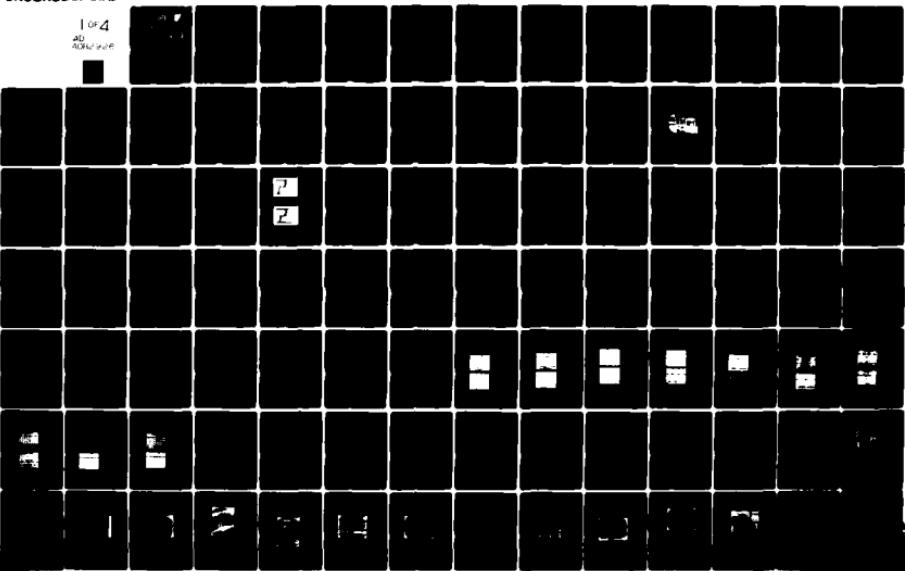


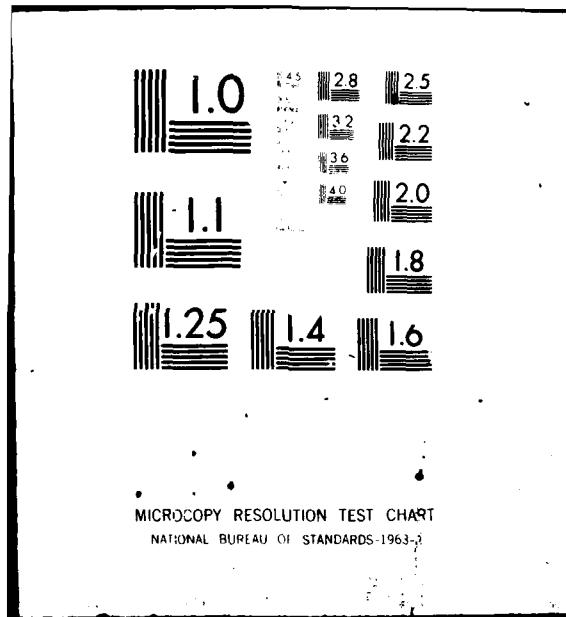
AD-AB82 926

RAYTHEON CO BEDFORD MA MISSILE SYSTEMS DIV  
RELIABILITY EVALUATION OF LOW POWER SCHOTTKY CLAMPED MICROCIRCUIT--ETC(U)  
FEB 80 K B LASCH, D BARTELS, J J SPINALE F30602-77-C-0186  
RADC-TR-80-5 NL

UNCLASSIFIED

1 of 4  
AD-AB82 926





ADA 082926

RADC-TR-80-5  
Final Technical Report  
February 1980

LEVEL



**RELIABILITY EVALUATION OF  
LOW POWER SCHOTTKY CLAMPED  
MICROCIRCUITS**

Raytheon Company

K. B. Lasch  
D. Bartels  
J. J. Spinalle  
P. H. Ackroyd

DTIC  
SELECTED  
APR 10 1980  
S D C

APPROVED FOR PUBLIC RELEASE; DISTRIBUTION UNLIMITED

**ROME AIR DEVELOPMENT CENTER  
Air Force Systems Command  
Griffiss Air Force Base, New York 13441**

DDC FILE COPY

80-1-10000

This report has been reviewed by the RADC Public Affairs Office (PA) and is releasable to the National Technical Information Service (NTIS). At NTIS it will be releasable to the general public, including foreign nations.

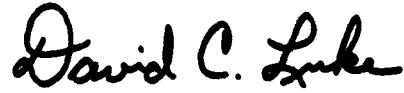
RADC-TR-80-5 has been reviewed and is approved for publication.

APPROVED:



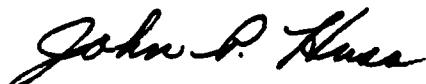
JOHN R. HABERER  
Project Engineer

APPROVED:



DAVID C. LUKE, Lt Col, USAF  
Chief, Reliability & Compatibility Division

FOR THE COMMANDER:



JOHN P. HUSS  
Acting Chief, Plans Office

If your address has changed or if you wish to be removed from the RADC mailing list, or if the addressee is no longer employed by your organization, please notify RADC (RBRP), Griffiss AFB NY 13441. This will assist us in maintaining a current mailing list.

Do not return this copy. Retain or destroy.

## UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

19) REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER RADC-TR-80-5	2. GOVT ACCESSION NO.	3. RECIPIENT'S CATALOG NUMBER
4. TITLE / SUBTITLE RELIABILITY EVALUATION OF LOW POWER SCHOTTKY CLAMPED MICROCIRCUITS.		5. TIME OF REPORT PERIOD COVERED Final Technical Report. September 77 - October 79
6. AUTHOR(s) K. B. Lasch D. Bartels J. J. Spinale		7. CONTRACT OR GRANT NUMBER(s) F30602-77-C-0186
8. PERFORMING ORGANIZATION NAME AND ADDRESS Raytheon Company/Missile System Division Hartwell Road Bedford MA 01730		9. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS 62702F 23380131
10. CONTROLLING OFFICE NAME AND ADDRESS Rome Air Development Center (RBRP) Griffiss AFB NY 13441		11. REPORT DATE February 1980
12. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office) Same		13. NUMBER OF PAGES 363
14. SECURITY CLASS. (of this report) UNCLASSIFIED		15a. DECLASSIFICATION DOWNGRADING SCHEDULE N/A
16. DISTRIBUTION STATEMENT (of this Report) Approved for public release; distribution unlimited.		
17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report) Same		
18. SUPPLEMENTARY NOTES RADC Project Engineer: John R. Haberer (RBRP)		
19. KEY WORDS (Continue on reverse side if necessary and identify by block number) Reliability Test and Failure Analysis Integrated Circuits Schottky Barrier Diode Microcircuits Microelectronics Circuits		
20. ABSTRACT (Continue on reverse side if necessary and identify by block number) An evaluation study has been completed on T <sup>2</sup> L Schottky integrated circuits of medium to large scale integration. The study consisted of electrical and physical characterization, step stress and accelerated long term testing, failure analysis and failure rate determination. The objective of this study was to verify the suitability of these devices for incorporation in advanced high speed digital military systems.		

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

111680

## UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE(When Data Entered)

Five device types were selected and each was procured from two manufacturers. Device selection was based upon the availability of the MIL-M-38510 slash sheet at the time of selection, and manufacturer selection was based upon his offering the greatest number of the devices selected. In all, in excess of 1000 devices from four different manufacturers were included in the study.

Electrical characterization was accomplished on computer-based test systems augmented by bench testing of transfer characteristics and thermal resistance.

Physical analysis revealed the following technological features to be represented:

- o single layer (Al only) and multilayer (Al/Ti-W/PtSi) metallization
- o single level and two level metallization
- o surface glassivation both doped with phosphorus and undoped.

Exploratory bench testing and step stress testing was utilized to determine the following temperature for use in the accelerated life test portion of this study:

hot storage life: 275°C, 300°C, 325°C  
operating life: 200°C, 225°C, 250°C

The hot storage accelerated life test was terminated after 4000h, and analysis of the results indicated a failure rate of less than .001 failures per 10<sup>6</sup> hours at 150°C ambient, evaluated at 10<sup>5</sup> hours.

The operating accelerated life test was terminated after 4000h of the 200°C group and after 3000h of the 225°C and 250°C groups. Analysis of the results indicated a failure rate of less than .001 failures per 10<sup>6</sup> at 125°C ambient, evaluated at 10<sup>5</sup> hours.

These figures are considerably better than the constant failure rates obtained from prediction methods of MIL-HDBK-217B.

The highlights of this study are:

- o The devices evaluated represent a mature, reliable technology suitable for military systems.
- o The prediction methods of MIL-HDBK-217B are too pessimistic.
- o Operating accelerated life test for the purpose of failure rate determination of some of these devices is virtually impossible because latch-up occurs at approximately 200°C ambient. This introduces electromigration at temperatures above 200°C, while testing below this temperature dilates test times to an unacceptable extent.
- o The Al/Ti-W/PtSi metallization system is more reliable than just aluminum.
- o Two electrical device behavior anomalies were identified and promulgated by means of GIDEP alerts.

## EVALUATION

This effort has successfully contributed toward the achievement of several specific goals identified in RADC TPO R5B, "Solid State Device Reliability." The primary objective of this study was to evaluate the reliability characteristics of complex low power Schottky diode clamped microcircuits using several representative test vehicles selected from devices for which MIL-M-38510 specifications had been recently developed. This reliability evaluation was one part in the continuing effort to identify potential life-limiting failure mechanisms associated with new microcircuit technologies prior to their full scale commitment to military electronic systems.

In particular, through the use of physical and electrical construction analysis techniques, specific design application, and specification weaknesses were identified. Corrective actions such as the issuance of GIDEP Alerts, recommendations for changes to MIL-M-38510, and direct communication with the microcircuit vendors have all been taken to ensure that identified problems do not adversely affect the design and development of costly electronic systems.

Accelerated life testing techniques were then evaluated and applied to all test vehicles. This phase of the study provided both an assessment of the relatively new concept of accelerated life testing and an evaluation of the long term reliability characteristics of the low power Schottky microcircuits. As a result of this study, specific suggestions were made regarding the implementation of accelerated testing. These recommendations will ensure that accelerated testing, as prescribed by MIL-STD-883, will yield valid data on microcircuit reliability and,

when used as a 100% screen, will not induce potentially dangerous latent failure mechanisms. Also, results of the long term life tests have indicated that the most common low power Schottky fabrication process in use today is a mature technology exhibiting very good reliability characteristics.

These findings are consistent with the rapidly increasing use of low power Schottky clamped microcircuits as evidenced both by the high production volume going to advanced electronic systems and by expanding list of QPL part types available to full MIL-M-38510 requirements. Although no life limiting reliability problems have been found to exist with the generic low power Schottky technology, it has been observed that some specific part types may exhibit design weaknesses that could affect system performance under worst case operation. Since all individual device designs cannot be evaluated in the depth that devices were studied under this effort, and since even an excellent specification cannot screen for every possible worst case application characteristic, it is therefore extremely important that any system design be thoroughly evaluated to ensure that all required worst case characteristics are specifically included in the device specification procurement documentation.



JOHN R. HABERER  
Project Engineer

## TABLE OF CONTENTS

<u>Section No.</u>	<u>TITLE</u>	<u>Page</u>
I.	Introduction	7
II.	General Information	12
	A. Delivery Times	12
	B. Hermeticity	13
	C. Gold Plating	13
III.	Electrical	14
	A. Schottky Diode TTL Circuits	14
	B. Low Power Schottky Circuits	15
	C. Parametric, Functional and Dynamic Testing	17
	D. Discussion of Failures at Initial Test	19
	1. Vendor A 54LS181	19
	2. Vendor B 54LS181	20
	3. Vendor A 54LS191	21
	4. Vendor B 54LS191	21
	5. Vendor A 54LS251	22
	6. Vendor B 54LS251	22
	7. Vendor A 54LS283	23
	8. Vendor B 54LS283	23
	9. Vendor C RAM	26
	10. Vendor D RAM	27
	E. Input/Output Transfer Characteristics	28
	F. Thermal Resistance	32
IV.	Construction Analysis	36
V.	Life Testing	41
	A. Life Test Configuration	41
	B. High Temperature Device Performance	47
	C. Step Stress Test	66
	1. Storage Step Stress	66
	2. Operating Step Stress	66
	D. Long Term Life Tests	67
	1. Long Term Storage Life	67
	2. Operating Life Test	67
		70

ACCESSION FOR	<input checked="" type="checkbox"/> MILITARY <input type="checkbox"/> DDC TABS <input type="checkbox"/> UNANNOUNCED		
REF ID:	Justification		
BY	Distribution /		
TYPE OF PROPERTY CLASS	Available or Special		
Dist	A		

## TABLE OF CONTENTS

<u>Section No.</u>	<u>TITLE</u>	<u>Page</u>
VI.	Criteria for Failure and Results A. Failure Definition B. Major Failure Modes and Mechanisms 1. Electromigration 2. Chip Separation C. Failure Analysis Summary D. Discussion	73 73 73 73 89 92 99
VII.	Final Results A. Failure Rates B. Schottky Diode C. General Comments	100 100 100 103
VIII.	Observations	104
IX.	Recommendations	106
Appendix A	Construction Analysis of Vendor A 54LS181	
B	Construction Analysis of Vendor B 54LS181	
C	Construction Analysis of Vendor A 54LS251	
D	Construction Analysis of Vendor B 54LS251	
E	Construction Analysis of Vendor A 54LS283	
F	Construction Analysis of Vendor B 54LS283	
G	Construction Analysis of Vendor A 54LS191	
H	Construction Analysis of Vendor B 54LS191	
I	Construction Analysis of Vendor C RAM	
J	Construction Analysis of Vendor D RAM	
K	Histograms - Critical Parameters	
L	Histograms - IOS	
M	Transfer Characteristics	
N	Initial/Final Distributions	

## LIST OF FIGURES

<u>Figure No.</u>	<u>Title</u>	<u>Page</u>
1.	Baker Clamp	14
2.	Macrodata MD 501	17
3.	Output Characteristics Vendor B 54LS283 Pin 4	25
4.	Output Characteristics Vendor A 54LS283 Pin 4	25
5.	Thermal Resistance Test Circuit	34
6.	Burn-in Configuration: 54LS181	42
7.	Burn-in Configuration: 54LS191	43
8.	Burn-in Configuration: 54LS251	44
9.	Burn-in Configuration: 54LS283	45
10.	Burn-in Configuration: RAM	46
11.	RAMS: $I_{CC}$ Versus Temperature	49
12.	54LS283: $I_{CC}$ Versus Temperature	50
13.	54LS251: Vendor A: $I_{CC}$ Versus Temperature	51
14.	54LS251: Vendor B: $I_{CC}$ Versus Temperature	52
15.	54LS191: $I_{CC}$ Versus Temperature	53
16.	54LS181: $I_{CC}$ Versus Temperature	54
17.	High Temperature Response, Vendor A, 54LS181	56
18.	High Temperature Response, Vendor B, 54LS181	57
19.	High Temperature Response, Vendor A, 54LS191	58
20.	High Temperature Response, Vendor B, 54LS191	59
21.	High Temperature Response, Vendor A, 54LS251	60

LIST OF FIGURES (continued)

<u>Figure No.</u>	<u>Title</u>	<u>Page</u>
22.	High Temperature Response, Vendor B, 54LS251	61
23.	High Temperature Response, Vendor A, 54LS283	62
24.	High Temperature Response, Vendor B, 54LS283	63
25.	High Temperature Response, Vendor C, RAM	64
26.	High Temperature Response, Vendor D, RAM	65
27.	Vendor D's RAM S/N 106 dc 7626	75
28.	Vendor D's RAM S/N 106 dc 7626	76
29.	Vendor D's RAM S/N 106 dc 7626	77
30.	Vendor D's RAM S/N 106 dc 7626	78
31.	Vendor D's RAM S/N 106 dc 7626	79
32.	Vendor D's RAM S/N 106 dc 7626	80
33.	Vendor D's RAM S/N 86 dc 7626	81
34.	Vendor D's RAM S/N 86 dc 7626	82
35.	Vendor D's RAM S/N 86 dc 7626	83
36.	Vendor A's 54LS283 S/N 44 dc 7732	85
37.	Vendor A's 54LS283 S/N 44 dc 7732	86
38.	Vendor A's 54LS283 S/N 44 dc 7732	87
39.	Vendor A's 54LS283 S/N 44 dc 7732	88
40.	Vendor B's 54LS283 S/N 140 dc 7741	90
41.	Vendor B's 54LS283 S/N 140 dc 7741	91

LIST OF TABLES

<u>Table No.</u>	<u>Title</u>	<u>Page</u>
1.	Low Power Schottky Test Plan	10
2.	Calculated Junction Temperature	11
3.	Delivery Times	12
4.	Initial Test Failures - Vendor A 54LS181	19
5.	Initial Test Failures - Vendor B 54LS181	20
6.	Initial Test Failures - Vendor A 54LS191	21
7.	Initial Test Failures - Vendor B 54LS191	21
8.	Initial Test Failures - Vendor B 54LS251	23
9.	Initial Test Failures - Vendor A 54LS283	23
10.	Initial Test Failures - Vendor B 54LS283	24
11.	Initial Test Failures - Vendor C RAM	26
12.	Typical $V_{OH}$ and $V_{OL}$ Versus Supply Voltage	30
13.	Typical $V_{OH}$ and $V_{OL}$ Versus Temperature	31
14.	Thermal Resistance Results	35
15.	C/A Summary	38
16.	Device Latching Results	55
17.	High Temperature Storage Results	68
18.	Expected Device Performance at Chosen Ambient Environment	70
19.	High Temperature Dynamic Operation - Results	72
20.	Listing of Low Power Schottky TTL Rejects	93
21.	Key to Failure Modes and Mechanisms	98
22.	Initial/Final Parametric Distributions and Drift	101

## ABSTRACT

An evaluation study has been completed on <sup>2</sup>T<sub>1</sub>L Schottky integrated circuits of medium to large scale integration. The study consisted of electrical and physical characterization, step stress and accelerated long term testing, failure analysis and failure rate determination. The objective of this study was to verify the suitability of these devices for incorporation in advanced digital military systems.

Five device types were selected and each was procured from two manufacturers. Device selection was based upon the availability of the MIL-M-38510 slash sheet at the time of selection, and manufacturer selection was based upon his offering the greatest number of the devices selected. In all, in excess of 1000 devices from four different manufacturers were included in the study.

Electrical characterization was accomplished on computer-based test systems augmented by bench testing of transfer characteristics and thermal resistance.

Physical analysis revealed the following technological features to be represented:

- o single layer (Al only) and multilayer (Al/Ti-W/PtSi) metallization
- o single level and two level metallization
- o surface glassivation both doped with phosphorus and undoped.

Exploratory bench testing and step stress testing was utilized to determine the temperature for accelerated life test.

The hot storage accelerated life test was terminated after 4000h, and analysis of the results indicated a failure rate of less than .001 failures per 10<sup>6</sup> hours at 150°C ambient, evaluated at 10<sup>5</sup> hours.

The operating accelerated life test was terminated after 4000h of the 200°C group and after 3000h of the 225°C and 250°C groups. Analysis of the results indicated a failure rate of less than .001 failures per 10<sup>6</sup> hour at 125°C ambient, evaluated at 10<sup>5</sup> hours.

These figures are considerably better than the constant failure rates obtained from prediction methods of MIL-HDBK-217B.

The highlights of this study are:

- o The devices evaluated represent a mature, reliable technology suitable for military systems.
- o The prediction methods of MIL-HDBK-217B are too pessimistic.
- o Operating accelerated life test for the purpose of failure rate determination of some of these devices is virtually impossible because latch-up occurs at approximately 200°C ambient. This introduces electromigration at temperatures above 200°C, while testing below this temperature dilates test times to an unacceptable extent.
- o The Al/Ti-W/PtSi metallization system is more reliable than just aluminum.
- o Two electrical device behavior anomalies were identified and promulgated by means of GIDEP alerts.

## I. INTRODUCTION

The overall low power Schottky program contained a total of 1010 devices with date codes ranging from 7614 to 7811.

In order to accomplish a comparative analysis four device types (54LS181, 54LS191, 54LS251, and 54LS283) were each purchased from two vendors (A and B). Since neither of these vendors manufactured similar  $T^2L$  Schottky memories, 256 x 1 bit RAM's from two other vendors, (C and D) were purchased. This vendor/group combination will be referred to as ten "types" throughout the study.

With parts from four manufacturers included in the study comparisons between vendor processes was possible. Design differences could also be pointed out since identical types were included from two vendors.

Initially, all devices were checked for hermeticity and then tested on the Macrodata MD 501 to the full MIL-M-38510 slash sheet requirements at  $+25^{\circ}\text{C}$ . All types with the exception of vendor D's RAM were received with tin plated leads. The tin was removed and leads were gold plated to prevent melting and oxidation at higher temperatures.

Following the plating operation, all units again were checked for hermeticity followed by an electrical go-no go test on the Macrodata MD 501. The test program used for the complete electrical test was identical to conditions, limits and test sequence called for in the corresponding slash sheets. In case of the RAM slight modifications were necessary. The parts were grouped as shown in the test plan of Table 1.

Devices used in the long term testing of both high temperature storage and high temperature operating life were data logged fully at room ambient and temperature extremes.

In order to determine junction temperature for devices under power during operation life tests, thermal resistance measurements were required. Five devices of each type and each vendor were checked for junction to case and junction to ambient with stagnant air; some typical units were measured for junction to air thermal resistance  $\theta_{JAF}$  under actual oven environment. The junction temperature was then calculated using  $\theta_{JAF}$  and the typical power dissipation at that ambient

temperature. The junction temperatures at the indicated oven ambients are summarized in Table 2.

One typical device of each "type" was subjected to high temperature dynamic operation to determine the actual ambient temperature at which the device outputs latched and also to record  $I_{CC}$  versus temperature. When latching occurred various device excitations were evaluated, in an attempt to find a configuration which would permit non-latched operation at the highest possible temperature.

Input/output transfer characteristics were taken for all device types with varying  $V_{CC} = 5.0V$ ;  $4.5V$  and  $5.5V$  at room ambient temperature and also at  $V_{CC} = 5.0V$  and ambient temperatures of  $-55^{\circ}C$ ,  $+25^{\circ}C$  and  $+125^{\circ}C$ . Under a nominal supply voltage of  $+5.0V$  and  $+25^{\circ}C$  the supply current was plotted during I/O transitions.

Propagation delay measurements were made using special bench tests to verify the results from the automatic MD 501 test system and also where device test results exceeded limits specified in the corresponding slash sheets.

The life test portion of the program consisted of two parts: step stress testing and long term life testing.

Step stress of both storage and high temperature dynamic operation was performed on all types. The step stress testing for dynamic high temperature operation was terminated at an upper temperature of  $+290^{\circ}C$ .

During the performance of the long term high temperature storage a representative sample of ten devices each of one type from each of the four vendors was subjected to three different ambient temperature environment.

Samples of all device types underwent high temperature dynamic operation. In the previous test, four of the ten types were already established to be latched-up at one or two of the high ambient temperatures. These were nevertheless included to study the effects of latched versus operational mode during accelerated life testing.

In the course of life testing failures were encountered only among the latched-up devices. For all normally operating devices, virtually no failures occurred. In order to calculate

median time to failure MTTF, standard deviations and activation energies  $E_a$  had to be assumed. Failure rates were then calculated at the maximum usage operating temperatures.

A detailed construction analysis was performed on all device types including mapping of the topology and verification of electrical schematics.

Failure analysis consisted of grouping of failure modes and the detailed determination of failure mechanisms on a sample for each group. During failure analysis, extensive use was made of the scanning electron microscope and micro-sectioning.

Table 1. Low Power Schottky Test Plan

DEVICE TYPE	VENDOR	CONTROL	INITIAL CHARACTERIZATION	STEP STRESS	LONG TERM			OPERATING			$\Sigma$	
					STORAGE	275°C	300°C	325°C	T <sub>A1</sub>	T <sub>A2</sub>	T <sub>A3</sub>	
54LS181	A	5	2	3	5	5			10	10	10	55
54LS251	A	5	2	3	5	5			10	10	10	55
54LS283	A	5	2	3	10	10	10		10	35	35	170
54LS191	A	5	2	3	5	5			10	10	10	55
256 BIT RAM	C	5	2	3	10	10	10	10	35	35	35	170
54LS181	B	5	2	3	5	5			10	10	10	55
54LS251	B	5	2	3	5	5			10	10	10	55
54LS283	B	5	2	3	10	10	10	10	10	35	35	170
54LS191	B	5	2	3	5	5			10	10	10	55
256 BIT RAM	D	5	2	3	10	10	10	10	35	35	35	170
												TOTAL 1010

Table 2. Calculated Junction Temperatures

Vendor	Device Type	Ambient Temperature			$T_J ({}^\circ C)$
		$T_{A1} = 200 {}^\circ C$	$T_{A2} = 225 {}^\circ C$	$T_{A3} = 250 {}^\circ C$	
A	54LS181	202	227	252	$T_J ({}^\circ C)$
A	54LS251	201	226	251	$T_J ({}^\circ C)$
A	54LS283	205	220	*	$T_J ({}^\circ C)$
A	54LS191	202	227	253	$T_J ({}^\circ C)$
A	RAM	209	234	*	$T_J ({}^\circ C)$
C	54LS181	203	228	253	$T_J ({}^\circ C)$
B	54LS251	201	226	252	$T_J ({}^\circ C)$
B	54LS283	209	*	*	$T_J ({}^\circ C)$
B	54LS191	203	228	254	$T_J ({}^\circ C)$
D	RAM	213	*	*	$T_J ({}^\circ C)$

\*Note: Junction temperatures can not be stated since devices were latched and power dissipation varied from unit to unit.

## II. GENERAL INFORMATION

### A. Delivery Times

The proposal included devices from four vendors and were originally quoted as off the shelf items with typically 4-6 weeks delivery. Worst case shipments, however, were promised within a 12 week time period at the time of order. Three conditions were imposed on the purchase orders: Uniform date codes for each device lot, units to be from recent production, and devices to be screened to MIL-STD-883B. Table 3 shows actual delivery times for all parts included in the study.

Table 3. Delivery Times

Vendor	Type	Ordered	Delivery Time in Weeks	Date Code
A	54LS181	11/3	5	7710
A	54SL251	11/3	31	7811
A	54LS283	11/3	4	7732
A	54LS191	11/3	4	7737
B	54LS181	11/3	3	7614/7630
B	54LS251	11/3	3	7711/7712
B	54LS283	11/3	9	7741
B	54LS191	11/3	2	7726
C	RAM	11/3	6	7744
D	RAM	11/22	10	7626

Through construction analysis and results from initial electrical test it was determined that no noticeable process or design differences existed in vendor B's devices of split date codes.

### B. Hermeticity Testing

All devices used in the study were initially tested for hermeticity. The fine leak test was performed by the use of a Norton Mass Spectrometer Leak Detector and a limit of  $5 \times 10^{-8}$  atm cc/sec was used as the acceptance limit.

Gross leak testing was done using the "Fluorocarbon gross leak method" specified in MIL-STD-883B, Method 1014.2, test condition C.

### C. Gold Plating

It was anticipated that with tin plated external leads at the proposed high operating and storage temperature well over  $+200^{\circ}\text{C}$  the tin would melt and oxidize during electrical and operating life testing. In order to prevent these problems from occurring, all device leads were tin stripped and nickel plated followed by gold plating. The detailed procedure was published in Appendix K of RADC TR-76-193 Final Technical Report, June 1976 entitled: "Reliability Evaluation of ECL Micro-circuits."

To verify the integrity of all units following the strip and plating process all devices were hermetically and electrically retested.

### III. ELECTRICAL

#### A. Schottky Diode TTL Circuits

A significant feature of the Schottky clamped circuit over the standard TTL is the use of a base-collector diode clamp: The Baker clamp.

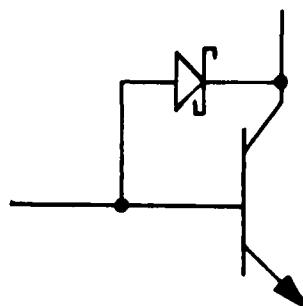


Figure 1. Baker Clamp

The clamp between base and collector of the transistor consists of a Schottky barrier diode which prevents the transistor from deep saturation by bypassing excess base drive. Since the transistor is almost out of saturation no excess base charge is stored and, therefore, the storage time is eliminated. When this structure is incorporated in TTL circuits, a marked reduction in propagation delay is realized.

An effective clamping diode requires a forward voltage characteristic lower than the base to collector junction forward voltage drop. The Schottky barrier diode, a metal to semiconductor junction has these characteristics and in addition due to the fact that it is a majority carrier device it will have negligible stored charge itself. The switching time of these diodes is very much faster than those of equivalent PN junctions. By incorporating the Schottky clamp, the need for gold doping used in regular TTL is no longer required.

## B. Low Power Schottky Circuits

Low Power Schottky circuits, contrary to standard Schottky TTL circuits, most often do not utilize the multiple emitter input scheme. In its place, Schottky diode input circuitry is used with individual inputs.

Input clamping is implemented also using Schottky barrier diodes to reduce negative-going excursions on the inputs. Because of the fast recovery time and its lower forward voltage drop, the Schottky input diode provides a significant improvement in clamping action over a conventional PN junction diode.

All transistors with the exception of the upper transistor in the totem pole of the output stages, which is in the Darlington configuration, have Schottky diode clamps. A Schottky clamp for this transistor is not required since the driving transistor does not permit the driven transistor to go into saturation.

The other main feature of the low power TTL Schottky device is that the circuit resistor values are approximately a factor of 10 larger than the standard Schottky devices. Hence, reduced power consumption is realized also resulting in lower operating junction temperatures. This in turn enhances the reliability and increases the MTTF. In addition as a result of lower internal currents, current densities are expected to be lower.

The devices included in the study are of medium to large scale integration and perform the outlined logic functions:

### Arithmetic Logic Unit, 4-Bit MIL-M-38510/308-01

This circuit performs 16 binary arithmetic operations on two 4-bit words. The device incorporates full internal carry look ahead and provides for either ripple carry between devices or for carry look ahead between packages.

The device has a complexity of 75 equivalent gates. The commercial device type number is 54LS181.

Multiplexer MIL-M-38510/309-05

This circuit is a high speed eight input digital multiplexer incorporating on-chip binary decoding to select one of eight data sources and features a strobe controlled tri-state output.

The device complexity is 15 equivalent gates. The commercial device type number is 54LS251.

4-Bit Binary Up/Down Counter MIL-M-38510/315-09

This circuit is a synchronous up/down, modulo 16 binary counter. State changes of the counters are synchronous with the low to high transition of the clock pulse input.

The device complexity is 58 equivalent gates and the commercial device type is 54LS191.

4-Bit Adder MIL-M-38510/312-02

This circuit is a high speed 4-bit binary full adder with internal carry look ahead. It accepts two 4-bit binary words and a carry input, and generates the binary sum outputs and the carry output from the most significant bit.

The device complexity is 36 equivalent gates and the commercial device type number is 54LS283.

256-Bit RAM MIL-M-38510/230 (format only)

This device is a fully decoded 256-bit random access memory organized as a 256-word by 1-bit array with an 8-bit address field and separate data in and data out lines. The device has three active low chip select inputs and a three state output.

### C. Parametric, Functional and Dynamic Testing

Electrical testing was performed at various times throughout the study, before and after gold plating, initial baseline at  $-55^{\circ}\text{C}$ ,  $+25^{\circ}\text{C}$  and  $+125^{\circ}\text{C}$ , during step stress, long term, and final testing again at the three temperature extremes.

A Macrodata MD 501 computerized test system shown in Figure 2 was used for all device testing throughout the study.

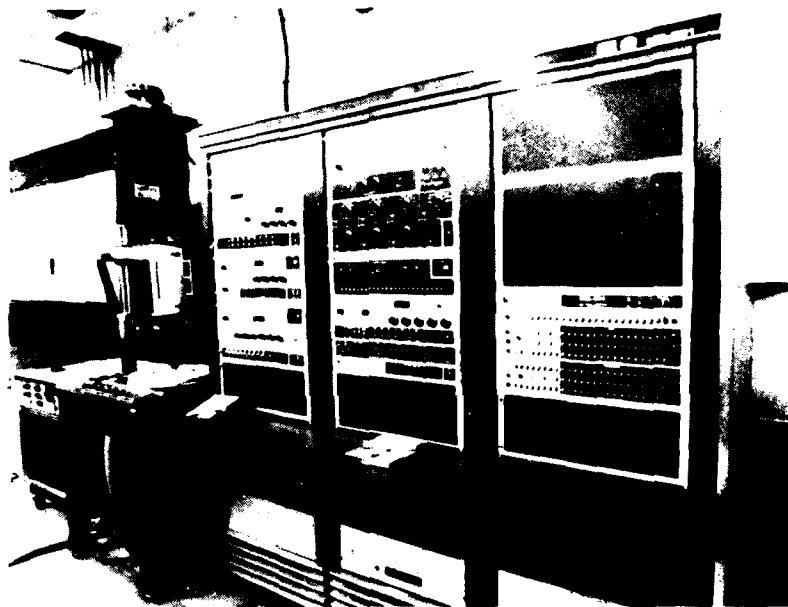


Figure 2

Macrodata MD 501

Individual test programs were generated for the parametric, functional and dynamic requirements to the governing slash sheet of MIL-M-38510 in the form available at that time:

54LS181	MIL-M-38510/308-01	Amendment 4 (8 Dec 77)
54LS251	MIL-M-38510/309-05	Amendment 1 (20 June 77)
54LS283	MIL-M-38510/312-02	Amendment 2 (8 Feb 78)
54LS191	MIL-M-38510/315-09	Proposed
256 Bit RAM	MIL-M-38510/230	Not released

The tests for each device type were in the exact order as documented in the respective slash sheet. Also device test conditions and limits were chosen to agree completely with the slash sheets for which released versions existed. Various corrections in test conditions were made during static and functional tests for the 54LS191 and RAM of both vendors. However, with the final release of MIL-M-38510/315 the mentioned corrections in test conditions have been included exactly or in an equivalent fashion.

The test program for the 256 bit RAM from both vendors follows the test sequence of the slash sheet, with test limits and conditions, however, according to vendors data sheets.

Functional testing consisted of three passes at +4.5V, 5.0V and 5.5V at 5MHz for all types with the exception of the RAM. Here the functional test frequency was 1MHz. Input levels during all functional testing were within limits of the governing slash or applicable data sheets; no worst case conditions were used. Output loading was as specified.

To guard against devices with low breakdown voltage of the lower output transistor, a collector-emitter breakdown test was performed at all device outputs and added to the automatic test program. The  $I_{CEX}$  current limit used was  $250\mu A$  when 5.5V were applied to the output terminal,  $Vcc = 5.5V$ .

To address the stability of the Schottky diodes additional forward voltage measurements at  $1.0\mu A$  and  $10.0\mu A$  of the input clamp diode was well as offset voltage measurements at all device outputs were included in all programs. The additional parametric testing followed the test sequence of the slash sheets and started with test number 501.

As previously mentioned all devices were tested on a go-no go basis initially and after gold plating. The initial data logging of device parameters on 9 track magnetic tape at room ambient and temperature extremes was performed only on those devices destined for long term high temperature storage and long term operational life test. All other units were data logged at  $+25^{\circ}C$  only.

A total of five control devices were data logged and hard copies of the results were obtained. Three units were used as controls for  $+25^{\circ}C$ , one device for  $+125^{\circ}C$  and one device for  $-55^{\circ}C$ . Prior to any testing, a corresponding control unit was data logged and its test results compared to the initial data.

#### D. Discussion of Failures at Initial Test

Parametric deviations from the specified limits for each "type" will be discussed. In cases where a significant number of devices failed a particular parameter a histogram showing the initial distribution for this parameter is included in Appendix K. Distributions for short circuit output current  $I_{OS}$  at  $+25^{\circ}\text{C}$  were plotted and are included in the Appendix L for all "types".

All histograms show normalized distributions regardless of lot size tested and quite frequently include multiples of identical tests per device. The scale indicated in the legend of each chart expressed in units refers to tests performed and not the number of devices. In cases where test limits vary such as where input pins drive more than one gate, the graphs reflect a fan-in of one equivalent.

In cases where devices failed to meet the ICEX test the failure tables do not reflect any deviation limits. The current in this case exceeded the programmed range when breakdown of less than 5.5V were encountered.

##### 1. Vendor A - 54LS181

The datalogged results refer to a total of 30 devices tested. The following failures were recorded at the temperatures indicated:

Table 4: Initial Test Failures - Vendor A 54LS181

Test Temperature	Number of Failed Devices	Parameter Failing	Deviation (less than)
$+125^{\circ}\text{C}$	14	$I_{IL}$	-10%
	10*	$V_{OH}$	

\*Due to automatic test system malfunction

The graph for input current  $I_{IL}$  shows a distribution (Appendix K-1) ranging from  $140\mu\text{A}$  to  $240\mu\text{A}$  at  $+125^{\circ}\text{C}$  with specified limits of  $160\mu\text{A}$  to  $400\mu\text{A}$ . These limits reflect one fan-in equivalent. Each of the indicated 14  $I_{IL}$  failures at  $+125^{\circ}\text{C}$  includes pin 8. Additional input low current failures of other input pins for these 14 recorded failures are of random nature.

The output voltage high  $V_{OH}$  failures of 10 devices at  $+125^{\circ}\text{C}$  in the table and also shown in the distribution (Appendix K-2) were a result of equipment problems. These units all failed output pin 16 on the Macrodata MD 501. The devices were bench tested and were well within specification limits.

## 2. Vendor B 54LS181

Thirty devices were tested with failures as shown:

Table 5: Initial Test Failures - Vendor B 54LS181

Test Temperature	Number of Failed Devices	Parameter Failing	Deviation (less than)
$-55^{\circ}\text{C}$	6	$I_{OS}$	-10%
	5	$I_{IL}$	-10%
$+25^{\circ}\text{C}$	1	$I_{CEX}$	
	12	$I_{OS}$	-10%
$+125^{\circ}\text{C}$	10	$I_{IH}$	+10%
	29	$I_{OS}$	-10%

The distribution for short circuit current  $I_{OS}$  at room temperature indicated a mean value just above the minimum specification value of  $+15\text{mA}$ . Since this limit applied also at  $+125^{\circ}\text{C}$  ambient temperature, almost all devices were below the minimum value specified.

The 10  $I_{IH}$  rejects consisted of devices whose  $I_{IH}$  on at best one input exceeded the maximum normalized limit of  $20\mu\text{A}$  for the input high level  $I_{IH}$ .

### 3. Vendor A 54LS191

The following non-conformance to specification were recorded for the 4 bit up/down counter.

Table 6: Initial Test Failures - Vendor A 54LS191

Test Temperature	Number of Failed Devices	Parameter Failing	Deviation (less than)
+25°C	1	$I_{CEX}$	
+125°C	26	$I_{IL}$	-10%

The input low current  $I_{IL}$  at +125°C originally tested to the limits of the proposed slash sheet from 180 $\mu$ A to 400 $\mu$ A, 26 of 30 devices failed. The released slash sheet modified the limits for  $I_{IL}$  from 100 $\mu$ A to 340 $\mu$ A for pin 11 and 160 $\mu$ A to 400 $\mu$ A for all others except pin 4 at an ambient temperature of +125°C. Based on the results shown in the distribution (Appendix K-5) only three devices fail this test, specifically at pin 14 to the new slash sheet limits.

### 4. Vendor B 54LS191

A total of 30 devices were initially characterized over temperature with the following failures.

Table 7: Initial Test Failures - Vendor B 54LS191

Test Temperature	Number of Failed Devices	Parameter Failing	Deviation (less than)
+25°C	2	$I_{IL}$	-20%
+125°C	30	$I_{IL}$	-20%

As shown in the Table all devices failed to meet the input low current  $I_{IL}$  limits of the proposed slash sheet of 180 $\mu$ A to

$400\mu A$  at  $+125^{\circ}C$ . In the released version the limits were changed to  $100\mu A$  to  $340\mu A$  for pin 11 and  $160\mu A$  to  $400\mu A$  for all others but pin 4. With these relaxed limits all devices pass the  $I_{IL}$  requirements. The histogram shown in Appendix K-6 clearly indicates two distributions; one at the lower end of the scale, the results for pin 11, the second at the higher end for all other inputs but pin 4 (not shown).

During propagation delay testing to the proposed slash sheet for test number 169 and 173 when the flip flops are loaded with one's and zero's and in either an "up" or "down" count mode, 17 out of 30 devices tested were found to be non-functioning. ( $t_{PHL}$  clock to output  $Q_D$  and  $t_{PLH}$  clock to output  $Q_D$ ). During these tests the clock pulse width specified was 25nsec and the ambient temperature was  $+125^{\circ}C$ . By widening the clock pulse width to greater than 40nsec or lowering the temperature below  $+90^{\circ}C$ , normal functional operation was resumed.

The released slash sheet inclusive of the latest amendment 2 (3 April 1979) will not catch this problem during any propagation delay tests since the clock pulse width has now been widened to a specified width of 500nsec. During the  $F_{max}$  test of the new specification this problem will not surface since only the QA output is tested. In circuit application at  $+125^{\circ}C$  ambient temperature, however, the maximum frequency essentially would be limited to approximately 12.5MHz and not detected by tests in the slash sheet. A GIDEP alert has been issued for vendor B's 54LS191 highlighting this problem. (GIDEP #K9-A-79-03)

#### 5. Vendor A 54LS251

All 30 units tested passed the requirements of the governing slash sheet at all three ambient temperature environments.

#### 6. Vendor B 54LS251

The list below shows parameters out of specification at the temperature indicated for a total of 30 units tested.

Table 8: Initial Test Failures - Vendor B 54LS251

Test Temperature	Number of Failed Devices	Parameter Failing	Deviation (less than)
-55°C	1	V <sub>OH</sub>	-10%
+125°C	9	I <sub>OS</sub>	-20%

As shown in the histogram (Appendix K-7) it is evident that the distribution for I<sub>OS</sub> centers around the minimum limit of 30mA. The specification range is 30mA to 100mA.

#### 7. Vendor A 54LS283

The following device failures were recorded during initial testing of 135 devices to MIL-M-38510/312 requirements:

Table 9: Initial Test Failures - Vendor A 54LS283

Test Temperature	Number Of Failed Devices	Parameter Failing	Deviation (Less Than)
+25°C	4	I <sub>CEX</sub>	
+125°C	2	I <sub>CC</sub>	+20%
	1	V <sub>OL</sub>	
	20	I <sub>IL</sub>	+10%

The distribution for I<sub>IL</sub> was normalized to a one fan-in equivalent and at an ambient temperature of +125°C centers around 170µA. With a minimum limit of 160µA some inputs are below the minimum requirement.

#### 8. Vendor B 54LS283

Initial testing of 135 devices at +25°C, -55°C, and +125°C to the governing slash sheet revealed the following device failures:

Table 10: Initial Test Failures - Vendor B 54LS283

Test Temperature	Number of Failed Devices	Parameter Failing	Deviation (less than)
-55°C	1	$I_{IL}$	+20%
	1	$I_{CC}$	
+25°C	7	$I_{CEX}$	-10%
	4	$V_{OH}$	
+125°C	3	$I_{OS}$	-10%

The indicated failures for  $I_{OS}$  shown in the Table were to limits of 30-130mA which now have been changed to 15-100mA in the latest version of MIL-M-38510/312. All devices passed the newly imposed limits for  $I_{OS}$ .

The initial testing at +125°C also revealed four device failures for  $V_{OH}$ . The output "high" voltage on these units was found to be below the minimum limit of 2.5V specified. A distribution of  $V_{OH}$  at maximum operating temperature for all outputs is shown in Appendix K-11 and can also be compared to the distribution of  $V_{OH}$  for Vendor A's equivalent device (Appendix K-8). Output pin 4 ( $\Sigma 1$ ) was separated out (Appendix K-12) as the lowest output high voltage  $V_{OH}$  and exhibited decreasing  $V_{OH}$  with increasing temperature.

This decrease of  $V_{OH}$  with temperature is not unique to the failed devices; in fact, every device of Vendor B's 54LS283 is affected. In the following brief evaluation, a device well within the specification limits was used for illustration purposes.

The output characteristics of pin 4 at room ambient temperature and +125°C is shown in Figure 3 and can be compared to Vendor A's equivalent device in Figure 4. In both cases an output "high" condition with respective inputs  $C_0$ ,  $A_1$  and  $B_1$  in a logic "1" state. Supply voltage  $V_{CC}$  was +5.0V. The curve tracer displays the output load characteristics and is offset such that the center of the graticule is at +5.0V.

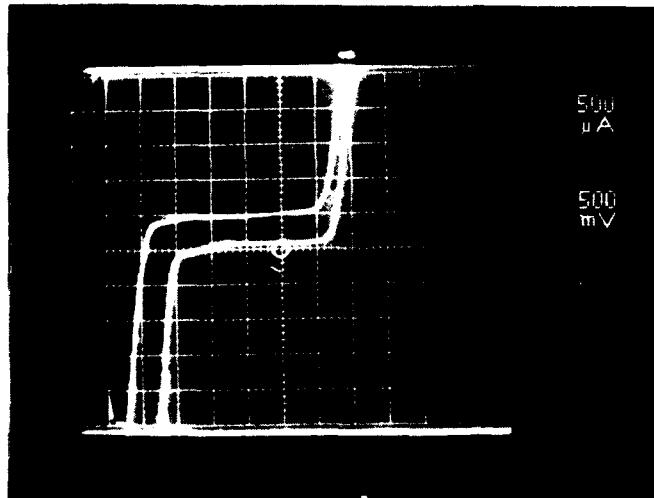


Figure 3.

Curve tracer display of Vendor B's output characteristics at pin 4. Lower curve was at 25°C; upper curve was at 125°C. Note 500 $\mu$ A leakage at 5V.

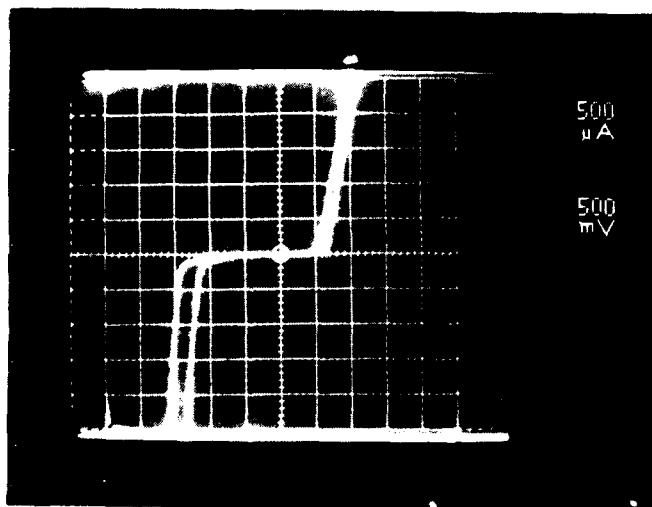


Figure 4.

Curve tracer display of Vendor A's output characteristics at pin 4. Outer curve was at 25°C; inner curve was at 125°C.

$V_{OH}$  for the 54LS283 is measured with an  $I_{OL}$  load current of  $-400\mu A$ . The comparison shows that  $V_{OH}$  for Vendor A's device shifted from 3.6 to 3.8V as temperature increased from  $25^{\circ}C$  to  $125^{\circ}C$ . The same temperature change produced a  $V_{OH}$  change from 3.4V to 3.0V for Vendor B's device.

Through internal probing, it was found that at room temperature the base of the phase splitting transistor Q4 (See Construction Analysis F-11) in the "off" state for Vendor B's 54LS283 is at a potential of +1.3V. In contrast in Vendor A's device, the base of the phase splitter was found to be at +1.0V. The potential of 1.3V measured at  $+25^{\circ}C$  could already be sufficient to start the partial turn on of the phase splitter Q4 and the lower output transistor Q<sub>8</sub>. As temperature increases, the two base-emitter junctions with their negative temperature coefficient will enhance the turn on. The partial turn on of the lower output transistor will result in a lower output voltage  $V_{OH}$ . This theory is supported by the fact that supply current  $I_{CC}$  increases were recorded for this device above  $+50^{\circ}C$ . (Figure 12). Also, when the base of Q4 was shunted to ground with a  $100\Omega$  resistor,  $V_{OH}$  assumed immediately a value consistent with expected levels of other low power Schottky devices.

When viewing the logic diagram of the construction analysis of Vendor B's 54LS283 (Appendix F-11) it can be seen that three logic paths exist through which the phase splitting transistor Q4 can be turned off. One of these paths through Q<sub>7</sub>, D<sub>7</sub> and Q<sub>10</sub> sets up the discussed 1.3 volt potential on the base of Q<sub>4</sub>. Probing at the emitter of Q<sub>8</sub>, a voltage of about 1.0V was recorded. This voltage was about .1V to .2V higher than, at equivalent locations of Q<sub>18</sub> or Q<sub>17</sub>. The exact cause of this higher voltage drop of the Schottky diode D<sub>7</sub> and transistor Q<sub>10</sub> combination was not determined.

A GIDEP Alert (GIDEP # K9-A-79-04) was issued for Vendor B's 54LS283.

#### 9. Vendor C's RAM

Initial test results from 135 devices tested showed the following results when tested to vendor data sheet limits.

Table 11: Initial Test Failures - Vendor C's RAM

Test Temperature	Number of Failed Devices	Parameter Failing	Deviation (Less Than)
$-55^{\circ}C$	6	$V_{OL}$	+10%
	3	$I_{OS}$	-10%

With the exception of one unit, all devices classified as  $V_{OL}$  rejects at  $-55^{\circ}\text{C}$  are exactly at the maximum limit of .4 volts. Three units rejected for  $I_{OS}$  at  $-55^{\circ}\text{C}$  were recorded with 1mA below the specification limit of 20mA.

#### 10. Vendor D's RAM

Initial testing of 135 devices following the guidelines of MIL-M-38510/230 proposed specification with vendor limits imposed. All devices passed the requirements at all three ambient temperatures.

## E. Input/Output Transfer Characteristics

Typical devices were selected from each vendor and type for input/output characterization plots.

Using an X-Y recorder (HP Mosley Model 7000A), the following graphs for input/output voltage or current characteristics were generated and are included in Appendix M.

- a) I/O for  $V_{CC} = 5V$ ,  $T = +25^{\circ}C$ ,  $T = +125^{\circ}C$  and  $T = -55^{\circ}C$
- b) I/O at  $T = 25^{\circ}C$  at  $V_{CC} = 4.5V$ ,  $5.0V$ ,  $5.5V$  and  $7.0V$
- c) I/O for  $V_{CC} = 4.5V$  at  $T = -55^{\circ}C$  and  $V_{CC} = 5.5V$  at  $T = +125^{\circ}C$
- d)  $I_{CC}/V_{IN}$  for  $V_{CC} = 5V$  at  $T = +25^{\circ}C$

For all the above conditions a particular defined path indicated on each graph was chosen and in all cases a standard specified load was used to simulate their respective driving requirements.

The output high level voltage  $V_{OH}$ , at specified load current is approximately:

$$V_{OH} \approx V_{CC} - 2V_{BE}$$

The output "high" voltage tracks almost directly any change in  $V_{CC}$  from  $+4.5$  to  $+5.5V$  at temperatures from  $-55^{\circ}C$  to  $+125^{\circ}C$  with the exception of vendors B's 54LS283 and the RAM's from both vendors.

In the case of vendor B's 54LS283 it was found that the output "1" voltage  $V_{OH}$  at  $+125^{\circ}C$  was lower than  $V_{OH}$  at  $+25^{\circ}C$ . A brief analysis performed at that time found that all outputs were affected to various degrees, however, output pin 4 most severely. It appears that the lower transistor in the totem pole output stage is partially turned on when that output is in a "1" state. This turn-on occurs only at elevated temperatures since the base of the phase splitting transistor is shunted to ground through two turned on transistors in series with one Schottky diode, and the created voltage drop on the base of the phase splitter is close to the sum of the  $V_{be}$ 's required to run on the phase splitter and output transistor.

All other transfer characteristics taken on this device were found to be normal.

For all devices, the output low voltages,  $V_{OL}$ , under maximum load conditions were within specified limits and varied less than 28mV per volt change of Vcc and its temperature coefficient ranges from  $-.12mV/^\circ C$  to  $-.31mV/^\circ C$ . (For details see Tables 12 and 13).

For typical devices operating under specified load conditions and a power supply voltage of 5.0V, delta  $V_{OH}$  values range from 2.9 to  $3.5mV/^\circ C$  for all low power Schottky devices in which the upper transistor of the output totem pole uses a base-emitter shunting resistor. When a bias resistor from the base of the upper output transistor to ground is used, such as in the RAMs of both vendors, the  $V_{OH}$  change with temperature ranges from 1.5 to  $1.7mV/^\circ C$ , which equals the temperature coefficient of one base to emitter junction. This design is not typical for low power Schottky devices. For power conservation, the base resistor of the upper output transistor is normally returned to the output terminal.

In both Tables 12 and 13 the abnormal  $V_{OH}$  behavior of vendor B's 54LS283 with Vcc and temperature change become evident.

For all devices except vendor B's 54LS283, the magnitude of  $V_{OL}$  change with temperature was typically about ten times smaller than the  $V_{OH}$  change with temperature. Their direction changes oppose each other, resulting in a larger output voltage swing at elevated temperatures under the same load conditions. Conversely, the lowest absolute output voltage swing is realized at the lowest operating temperature:  $V_{OL}$  is the highest while  $V_{OH}$  is lowest.

In Appendix M graphs showing supply current  $I_{CC}$  versus input voltage  $V_{IN}$  are included. The curves were taken with only one output loaded which also was the only output being exercised. One input was switched while all others were tied high or low. The  $I_{CC}$  current measured was the sum total of all currents within the device. The external load current of the output exercised was provided by a separate power supply and therefore was not included in the  $I_{CC}$  displayed. The current spike shown in these graphs was mainly due to the current contributions of totem pole transistor overlaps during transition periods. By viewing the individual graphs it can be seen that the current spike was dependent on the direction of the output transition. The magnitude of the current spike depended on the amount of overlaps and may be different for each type.

Table 12.  
Typical  $V_{OH}$  and  $V_{OL}$  Versus Supply Voltage

Type	Vendor	$V_{OH}/V_{CC}$ [mv/V]	$V_{OL}/V_{CC}$ [mv/V]
54LS181	A	1000	12.1
54LS251	A	990	17.0
54LS283	A	980	11.3
54LS191	A	980	9.9
RAM	C	430	19.9
54LS181	B	980	23.9
54LS251	B	1020	25.3
54LS283	B	*320	27.7
54LS191	B	960	26.5
RAM	D	500	23.7

\*Abnormal device behavior

Table 13.  
Typical  $V_{OH}$  and  $V_{OL}$  Versus Temperature

Type	Vendor	$V_{OH}/T$ [mv/ $^{\circ}C$ ]	$V_{OL}/T$ [mv/ $^{\circ}C$ ]
54LS181	A	3.5	-.21
54LS251	A	2.9	-.12
54LS283	A	3.4	-.22
54LS191	A	3.4	-.21
RAM	C	1.5	-.28
54LS181	B	3.3	-.29
54LS251	B	3.3	-.21
54LS283	B	*-4.9	-.27
54LS191	B	3.3	-.31
RAM	D	1.7	-.17

\* Abnormal device behavior

#### F. Thermal Resistance Measurements

For purposes of calculations of junction temperatures while dissipating power during limit and operational life testing the thermal resistance of all device types was measured. All measurements were made using the substrate diode junction as temperature reference. A constant current of 1mA was used for calibration and during measurements. (Discussion refers to Figure 5).

The device dissipation was accomplished by the use of one emitter follower circuit driven by a Data Pulse 110 generator. The repetition rate was such that the device under test was powered for better than 99.5%. For a period of 30 microseconds power was removed during which a measurement was made. To prevent possible overloading of the type W plug-in and achieve better accuracy a specially designed sampling network was employed.

Three measurements were made and the results shown in Table 14.

- $\theta_{JC}$  - Junction to case; utilizing FC 77 fluorocarbon liquid as heat sink.
- $\theta_{JA}$  - Junction to stagnant air at +25°C using an enclosure having a cavity of 1.5' x 1.5' x 1'.  
Sockets used were Robinson-Nugent; high temperature 16 pin IC-163-S2-HT for devices in 16 pin DIP packages. A Textool 24 pin Zip Dip socket 224-3344 was employed for all 54LS181 in the 24 pin DIP package.  
(Devices inserted not flush to socket).
- $\theta_{JAF}$  - Junction to air at +60°C in the life test oven environment and actual life test fixture. For this specific measurement only one selected typical device of each low power Schottky type was included.

Thermal resistance measurements  $\theta_{JC}$  and  $\theta_{JA}$  performed on five units per group and are for reference information only.

Results for thermal resistance  $\theta_{JAF}$  measured on one typical device per group were used to calculate junction temperature for both limit and long term life testing. Results ranged from 24°C/W to 49°C/W.

As indicated in Table 14, average values for junction to case measurements of all types and vendors tested ranged from 11°C/W to 28°C/W and therefore were well within the specified limits of vendor and military specification.

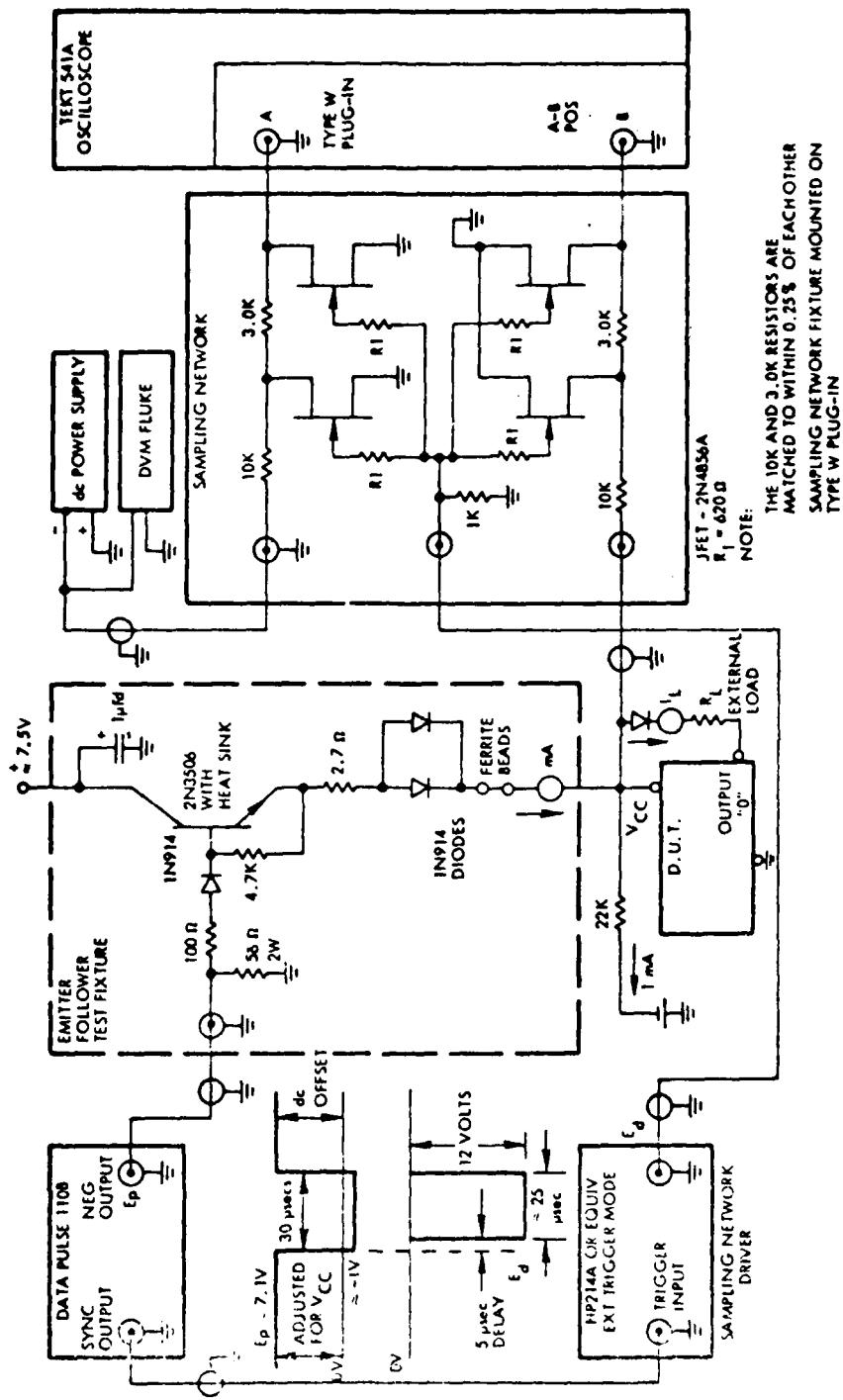


Figure 5. Thermal Resistance Test Circuit

Table 14. Thermal Resistance Results

		THERMAL RESISTANCE (stagnant air)							
VENDOR	DEVICE TYPE	$\theta_{JA}$ [ $^{\circ}\text{C}/\text{W}$ ]		$\theta_{JC}$ [ $^{\circ}\text{C}/\text{W}$ ]		$\theta_{JAF}$ [ $^{\circ}\text{C}/\text{W}$ ]		ONE DEVICE	
		LOW	MEAN	HIGH	LOW	MEAN	HIGH		
A	54LS181	64	73	80	13	14	15	24	
B	54LS181	54	61	70	15	16	18	30	
A	54LS191	105	114	124	12	13	14	31	
B	54LS191	109	123	131	17	19	21	38	
A	54LS251	92	107	129	16	21	23	40	
B	54LS251	133	145	160	24	28	36	41	
A	54LS283	111	118	124	14	18	21	49	
B	54LS283	119	122	124	16	19	23	45	
C	RAM	92	105	113	10	11	13	39	
D	RAM	102	106	112	10	11	12	40	

\* actual oven environment

#### IV. CONSTRUCTION ANALYSIS

The detailed construction analysis which includes verification of the electrical schematic by chip mapping, detailed identification of components of interest and of metallization systems, and sketches of important cross-sections, are shown in individual report in Appendices A-J as follows:

Vendor A:	54LS181	Appendix A
Vendor B:	54LS181	Appendix B
Vendor A:	54LS251	Appendix C
Vendor B:	54LS251	Appendix D
Vendor A:	54LS283	Appendix E
Vendor B:	54LS283	Appendix F
Vendor A:	54LS191	Appendix G
Vendor B:	54LS191	Appendix H
Vendor C:	RAM	Appendix I
Vendor D:	RAM	Appendix J

All devices with the exception of the 54LS181 from vendor A and B are in 16 lead ceramic dual-in-line packages. The 54LS181 are packaged in 24 lead ceramic dual-in-line.

All device "types" have glassivation covering the entire chip exposing the bonding pads only. A single level metallization is used for all types, with diffused underpasses where required. The only exception is vendor C's RAM where a two level metallization is employed. This device makes use of emitter coupled logic (ECL) for the internal circuitry with TTL Schottky input and output stages and therefore has access times 2 to 2½ times less than vendor D's version.

A trimetal system containing titanium-tungsten as a barrier and aluminum as the primary conductor was used by nine of the ten types. Platinum silicide in contact areas of highly doped N+ regions result in ohmic contacts while platinum silicide in areas of low doping materials forms the Schottky barrier diodes. The chip aluminum metallization in all cases is 99.9% pure, bond wires are 99% aluminum and 1% silicon. Vendor D's RAM, however, uses aluminum metallization without barrier metal and also aluminum Schottky diodes. An additional unique

feature of vendor D's RAM was the absence of phosphorus dopant in the surface glassivation, typically used for thermal expansion purposes. Furthermore, vendor D's external leads were gold plated without nickel underplate. All other devices were received with tin plated leads. Vendor D's RAM also was the only device packaged in a DIP using Au/Ni/Mo for the die attach area; all others used a thick film Au paste.

To prevent degradation of reverse leakage characteristics of the Schottky input clamp diode an annular diffused junction diode of higher breakdown voltage than the Schottky diode was used by all vendors. This "guard ring" allows the actual Schottky diode to avalanche when forced into breakdown.

The calculated cross-sections of the device metallization was the result of measurement on two devices per type. These metallization cross-sections were used to calculate current densities. The worst case current density was found to be vendor C's RAM with  $1.1 \times 10^5$  A/cm<sup>2</sup>.

The current densities were typical values and do not reflect current density increases over oxide steps. Even where thinning of the metallization occurs the maximum resulting current densities were below the maximum level of  $5 \times 10^5$  A/cm<sup>2</sup> specified in MIL-M-38510.

Transistor input structures used for both vendor A and B's 54LS181 do not allow input interfacing with C-MOS devices. All other types with input diode structures can directly be driven from C-MOS units. However, a redesign of vendor A's 54SL181 to diode input circuitry in late 1977 eliminates this shortcoming on devices date coded 7801 or later.

Table 15 lists important features and basic differences between all device types included in the study as they relate to different vendors.

TABLE 15: C/A SUMMARY

Vendor	Device Type	Epitaxial Thickness ( $\mu\text{m}$ )	Metallization Used	Barrier Metal Thickness Å	Contact	Glassivation Thickness ( $\mu\text{m}$ )	$\text{SiO}_2$ Dopants
A	54LS181	3.2	Ti-W-Al	4000	Pt. Silicide	1.5	Phosphorus
B	54LS181	3.8	Ti-W-Al	5000	Pt. Silicide	2.5	Phosphorus
A	54LS251	2.8	Ti-W-Al	2600	Pt. Silicide	1.3	Phosphorus
B	54LS251	3.5	Ti-W-Al	2500	Pt. Silicide	2.4	Phosphorus
A	54LS283	3.3	Ti-W-Al	3200	Pt. Silicide	1.6	Phosphorus
B	54LS283	4.1	Ti-W-Al	4000	Pt. Silicide	1.9	Phosphorus
A	54LS191	3.6	Ti-W-Al	3000	Pt. Silicide	1.6	Phosphorus
B	54LS191	5.1	Ti-W-Al	4000	Pt. Silicide	2.0	Phosphorus
C	RAM	4.0	Ti-W-Al	4000	Pt. Silicide	1.1	Phosphorus
D	RAM	5.0	Al		Al	2.5	None

TABLE 15: C/A SUMMARY

(Continued)

Vendor	Device Type	Thermal Oxide Present	Metallization In Die Attach Area	Lead Plating Material Thickness (μm)	Metallization Width (μm)	Metallization Thickness (μm)
A	54LS181	Yes	Au	Sn (8.75)	1.8	1.5
B	54LS181	Yes	Au	Sn (5.0)	20.7	2.4
A	54LS251	Yes	Au	Sn (6.25)	9.2	1.3
B	54LS251	Yes	Au	Sn (7.5)	1.1	2.4
A	54LS283	Yes	Au	Sn (5.0)	5.65	1.6
B	54LS283	Yes	Au	Sn (8.75)	7.8	1.9
A	54LS191	Yes	Au	Sn (4.4)	20	1.6
B	54LS191	Yes	Au	Sn (6.25)	21.3	2.1
C	RAM	Yes	Au	Sn (8.75)	9.8	1.5
D	RAM	Yes	Au/Ni/Mo	Au (2.5)	2.3	1.3

TABLE 15 : C/A SUMMARY  
 (Continued)

Vendor	Device Type	Cross-Sectional Area (cm <sup>2</sup> )	Maximum Current (mA)	Maximum Current Density (A/cm <sup>2</sup> )*
A	54LS181	2.7 x 10 <sup>-7</sup>	4.6	1.7 x 10 <sup>4</sup>
B	54LS181	5 x 10 <sup>-7</sup>	4.8	9.6 x 10 <sup>3</sup>
A	54LS251	1.2 x 10 <sup>-7</sup>	4.6	3.8 x 10 <sup>4</sup>
B	54LS251	2.64 x 10 <sup>-7</sup>	1.6	6.1 x 10 <sup>3</sup>
A	54LS283	9.04 x 10 <sup>-8</sup>	1.6	1.77 x 10 <sup>4</sup>
B	54LS283	1.5 x 10 <sup>-7</sup>	1.5	1.01 x 10 <sup>4</sup>
A	54LS191	3.2 x 10 <sup>-7</sup>	4.8	1.5 x 10 <sup>4</sup>
B	54LS191	4.48 x 10 <sup>-7</sup>	4.3	9.6 x 10 <sup>3</sup>
C	RAM	1.47 x 10 <sup>-7</sup>	16	1.1 x 10 <sup>5</sup>
D	RAM	6.9 x 10 <sup>-7</sup>	12	4.0 x 10 <sup>4</sup>

\* These are typical values and do not reflect current density increases over oxide steps.

## V. LIFE TESTING

### A. Life Test Configurations

All device "types" included in the study were subjected to a dynamic operational life test. The configurations used were identical to those suggested in the governing slash sheets (issues identified on page 17, under III C). Only one modification was made: in the case of the 54LS191 the load input pin was grounded. With this modification the ambient temperature at which latching occurred was raised from +185°C to 265°C for devices from both vendors. All device outputs were loaded to sink the maximum specified load current  $I_{OL}$ . Individual limiting resistors were used in the Vcc line for every burn-in position. The value of the resistors (5 or 10 ohms) were as specified in the burn-in configurations of the slash sheets. Vcc lines for the RAM burn-in positions were individually fused with a  $\frac{1}{2}$ A 250V "LITTELFUSE" (312-3AG).

The supply voltage was adjusted such that for typical devices, non latched, 5V was measured at the Vcc terminal. Applied input signals were digitally generated with a 50% duty cycle and with a high frequency of 100KHz. ( $A_0 = 100\text{KHz}$ ,  $A_2 = 25\text{KHz}$ , etc.). Input voltage amplitudes were 3V TTL levels.

1) Arithmetic Logic Unit - 54LS181

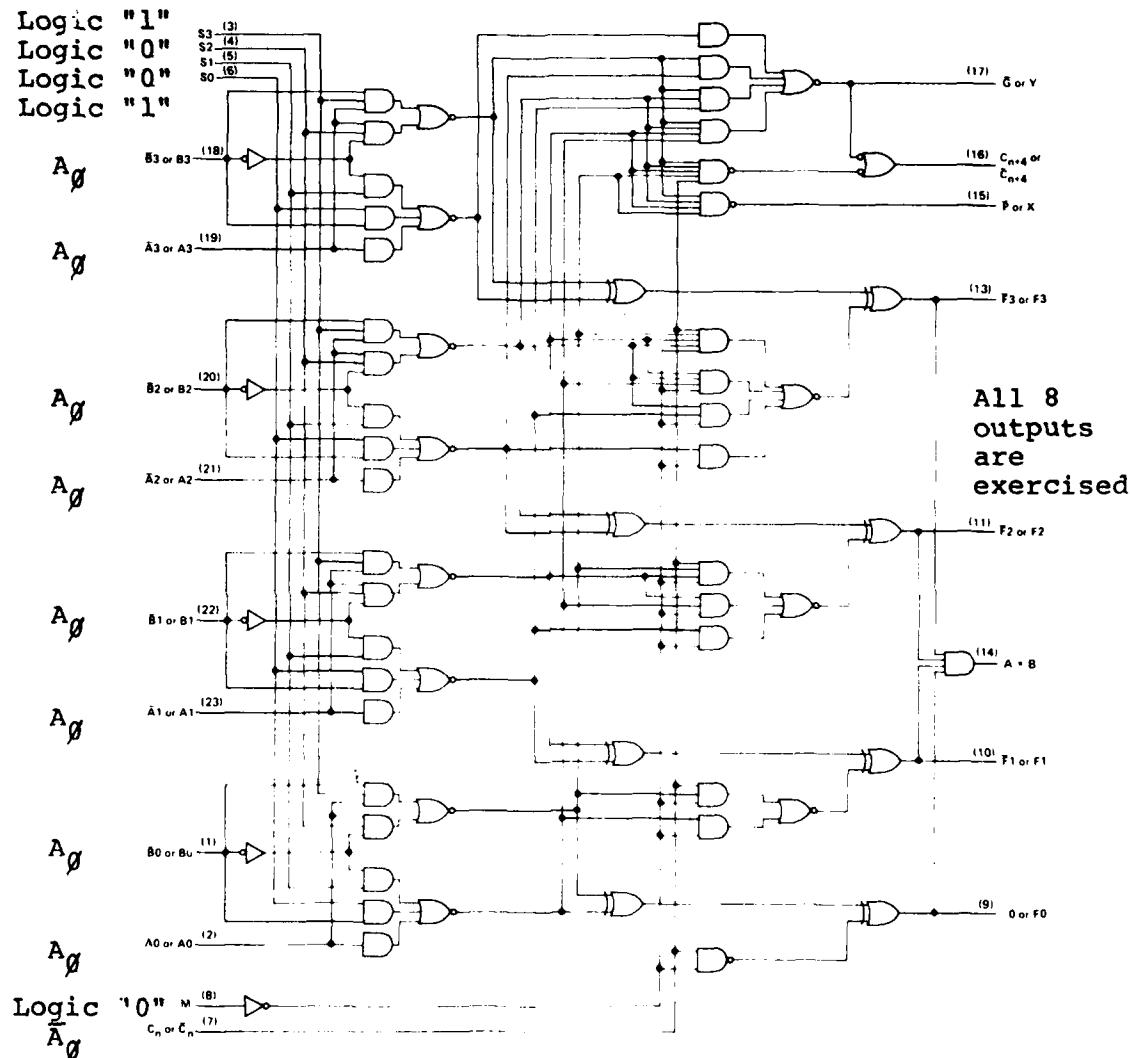


Figure 6

Burn-in Configuration: 54LS181

Nine of the inputs are dynamically addressed which results in 70 out of 79 gates and all eight outputs being exercised.

4) Synchronous Counter - 54LS191

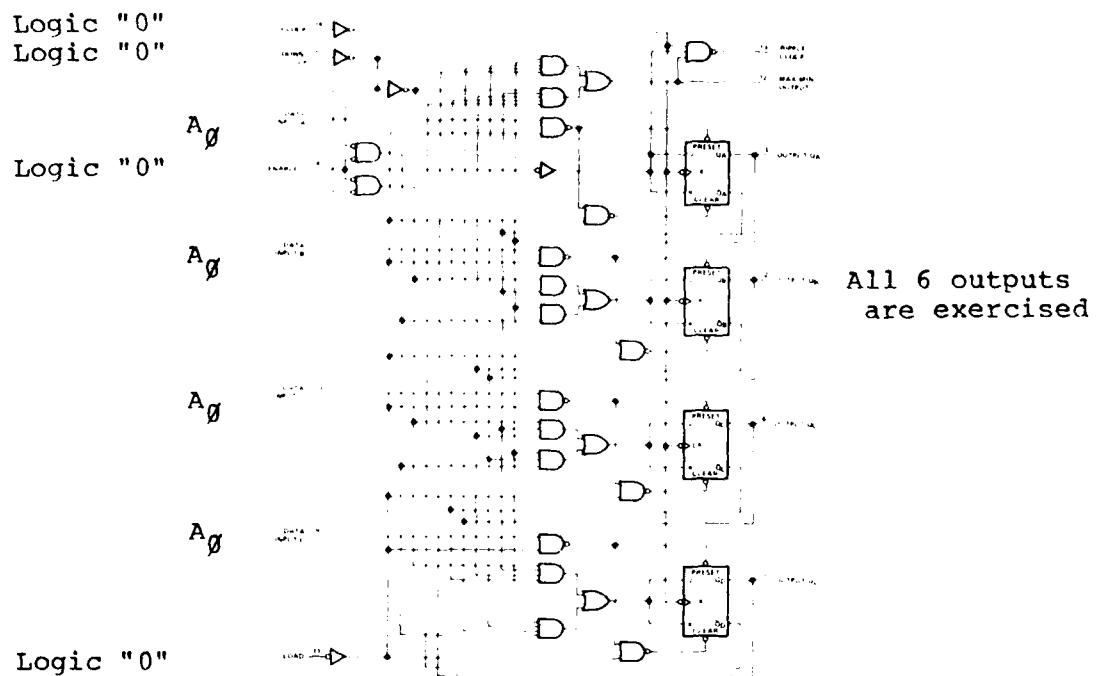


Figure 7  
Burn-in Configuration: 54LS191

The four data inputs are exercised while the load input is grounded continually loading the output flip-flops. All six outputs are exercised.

2) Data Selector/Multiplexer - 54LS251

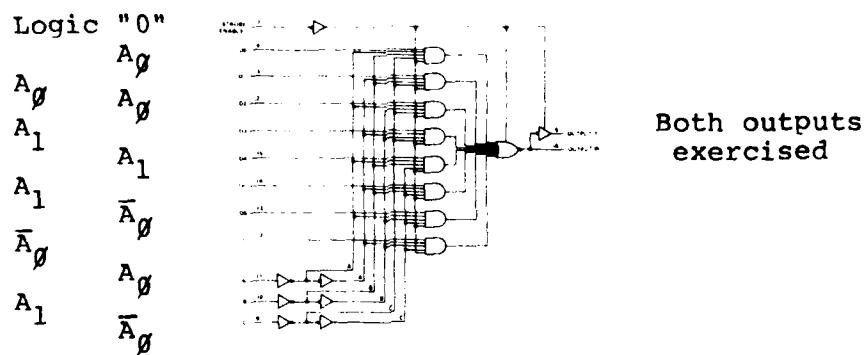


Figure 8

Burn-in Configuration: 54LS251

All inputs except the "strobe" input are exercised resulting in all but one gate and therefore both outputs being operated in this combinational circuit.

3) Four Bit Adder - 54LS283

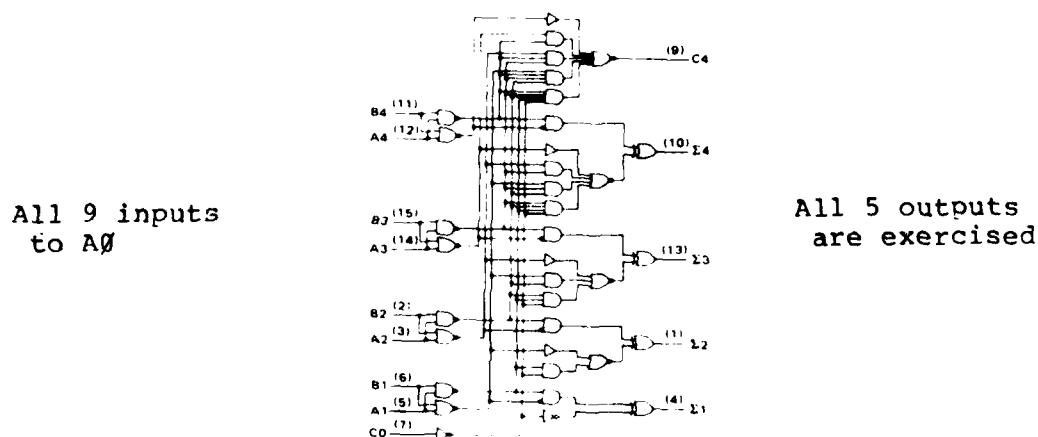


Figure 9

Burn-in Configuration: 54LS283

All inputs to the adder are exercised with the same 100KHz signal resulting in all gates and outputs being dynamically operated during burn-in.

5) 256 Bit RAM

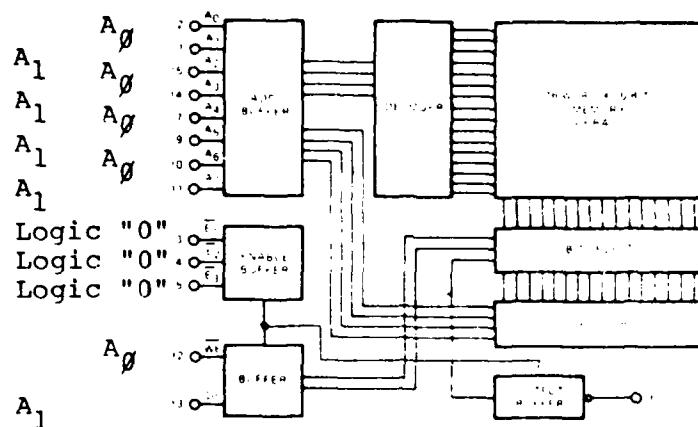


Figure 10

Burn-in Configuration: RAM

With the input stimuli shown, four memory locations are being addressed sequentially. Two are being written into and two are read.

## B. High Temperature Device Performance

Prior to subjecting all device "types" to step stress or long term dynamic testing, one unit from each vendor-type was checked for proper operation at elevated temperatures. In the dynamic latching test, the devices were exercised using a circuit and conditions specified by the governing slash sheets. In the actual chamber configured for long term dynamic operation one unit at a time was monitored for correct logic and output latching while the supply current was recorded up to the highest temperature possible. See Figures 11 to 16.

In all cases where device performance limited the operation to temperatures below +275°C extensive testing was done. This testing included variations in device excitation and also variations in input and supply voltage levels.

For all device types a static latching was additionally performed in which  $I_{CC}$  and combined input leakage currents were also recorded. The critical output as determined from the dynamic test was toggled to a "1" and then a "0" state.

Table 17 summarizes these discussed results. The temperature shown in the column "incorrect logic" is the ambient temperature at which either latching of the outputs or incorrect logic occurred. Photographs taken for the 54LS181, 54LS191, or 54LS251 from both vendors (Figure 17-22) are either directly or slightly below the latching ambient temperature indicated in the table to prove that correct logic was observed.

In the case of the 54LS283's and the RAM's, photographs (Figures 23-26) were taken at the indicated temperatures to prove that correct logic was not observed.

In all Figures 17-26 applied inputs and the expected output waveforms are drawn. Also shown are photographs of the most critical output at room temperature and the same output at elevated temperature. By lowering this ambient temperature by five degrees proper operation can be obtained.

This data indicates that both vendor A's and B's 54LS181 properly operate to +295°C.

The operation for both vendor A's and B's 54LS191 was limited to +185°C when using recommended burn-in circuit. The output Q<sub>B</sub> assumed a level between "1" and "0" at all times when the load command was in a "1" state. If, however, the load command remained at "0", proper operation of these devices was observed to +285°C and +265°C, respectively.

Vendor B's 54LS251 was operated satisfactorily to +300°C while vendor A's equivalent showed output pulse deterioration at output W. A supply current increase of about 30mA was observed to occur at +230°C.

Vendor A's 54LS283 was dynamically latched at +240°C, a severe step increase in supply current was recorded at +210°C.

Vendor B's equivalent unit was inoperative at +200°C due to the collapse of V<sub>OH</sub> at elevated temperatures. This problem was especially severe on output pin 4. A steady supply current increase starting at a temperature of +120°C was recorded to about +210°C when a major current step increase occurred.

Both vendor C's and D's RAM were considered latched at temperatures above 225°C and 250°C, respectively.

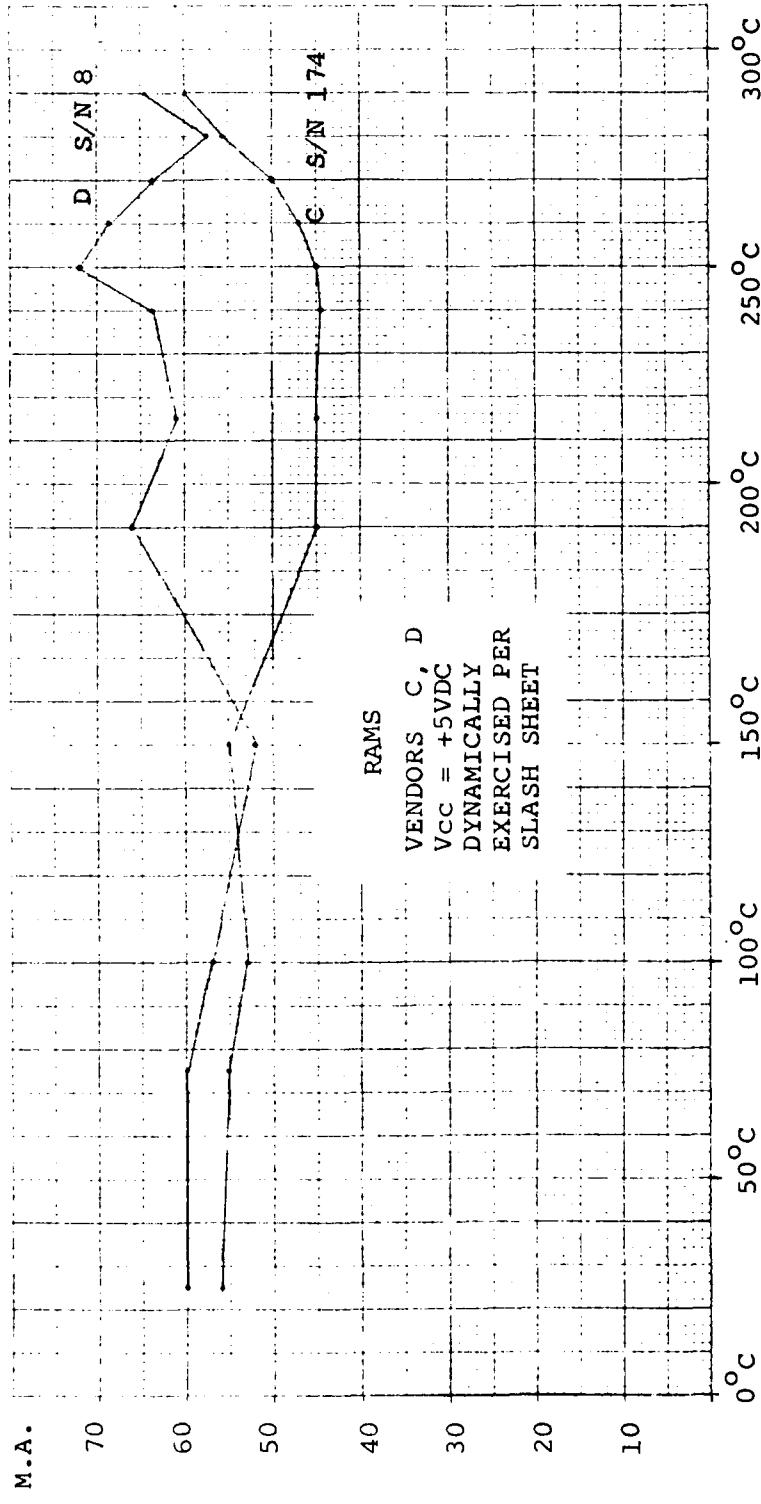


Figure 11: RAMS,  $I_{cc}$  vs. Temperature

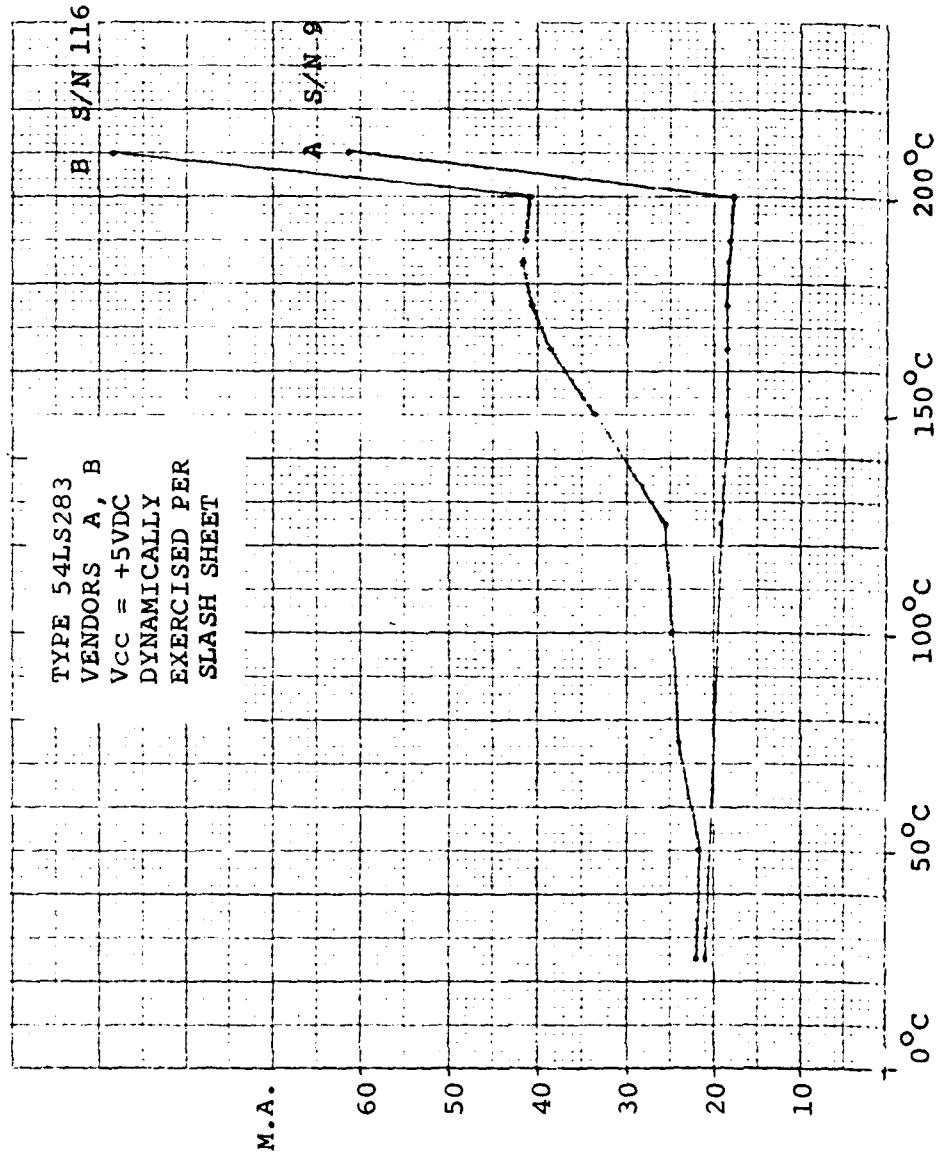


Figure 12: 54LS283, Icc vs. Temperature

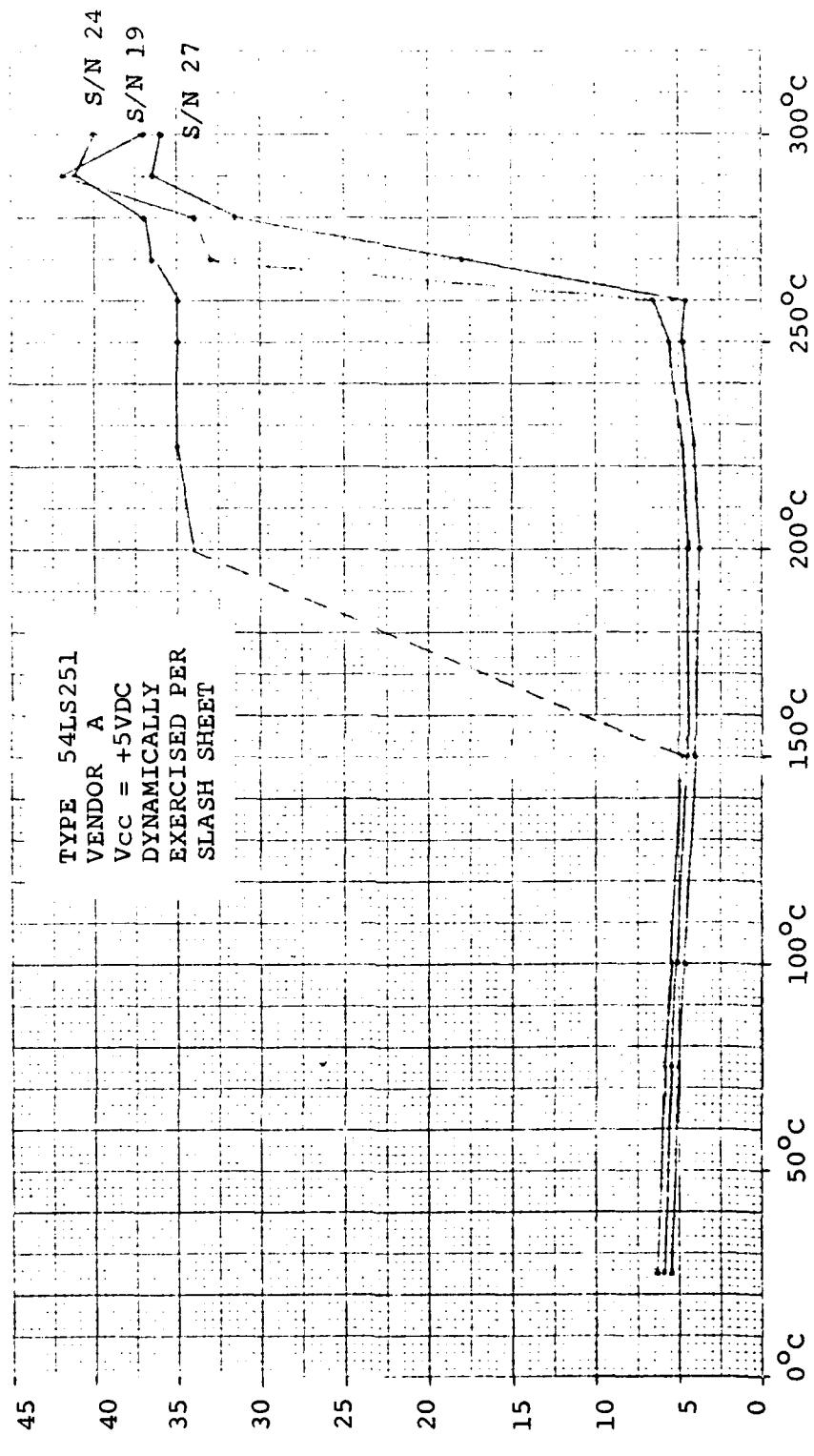


Figure 13 : 54LS251, Vendor A, Icc vs. Temperature

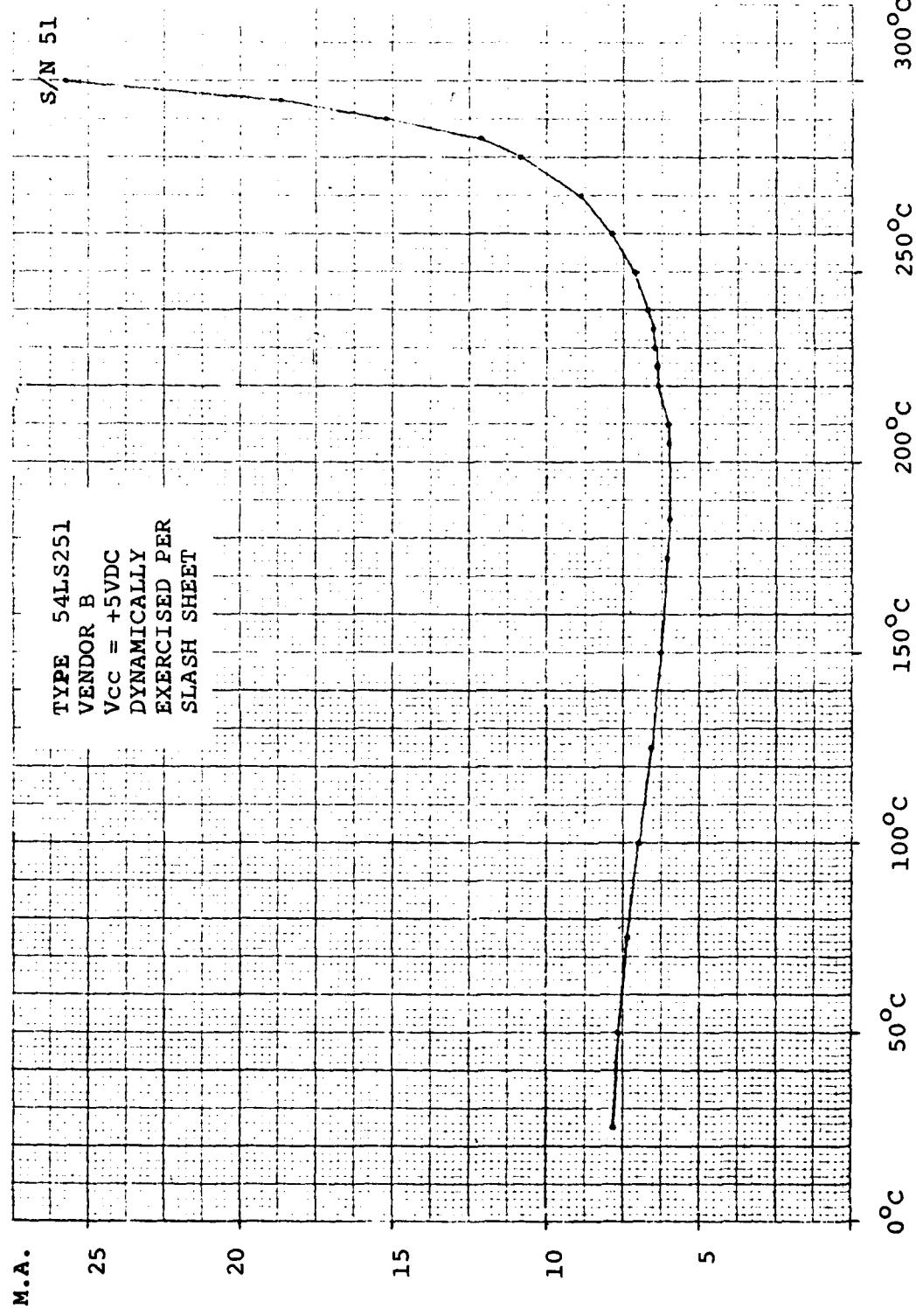


Figure 14 : 54LS251, Vendor B, I<sub>cc</sub> vs. Temperature

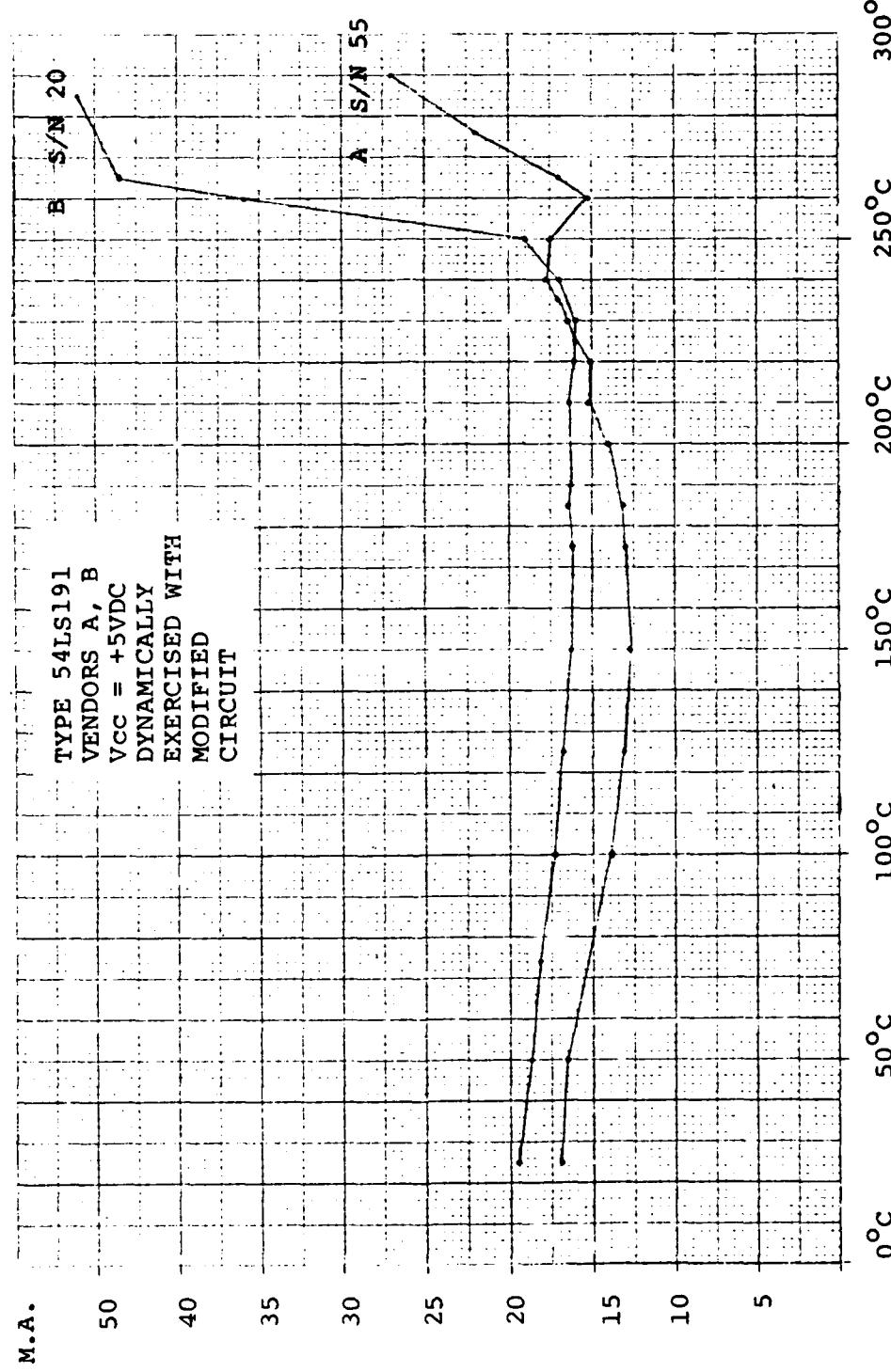


Figure 15: 54LS191, Icc vs. Temperature

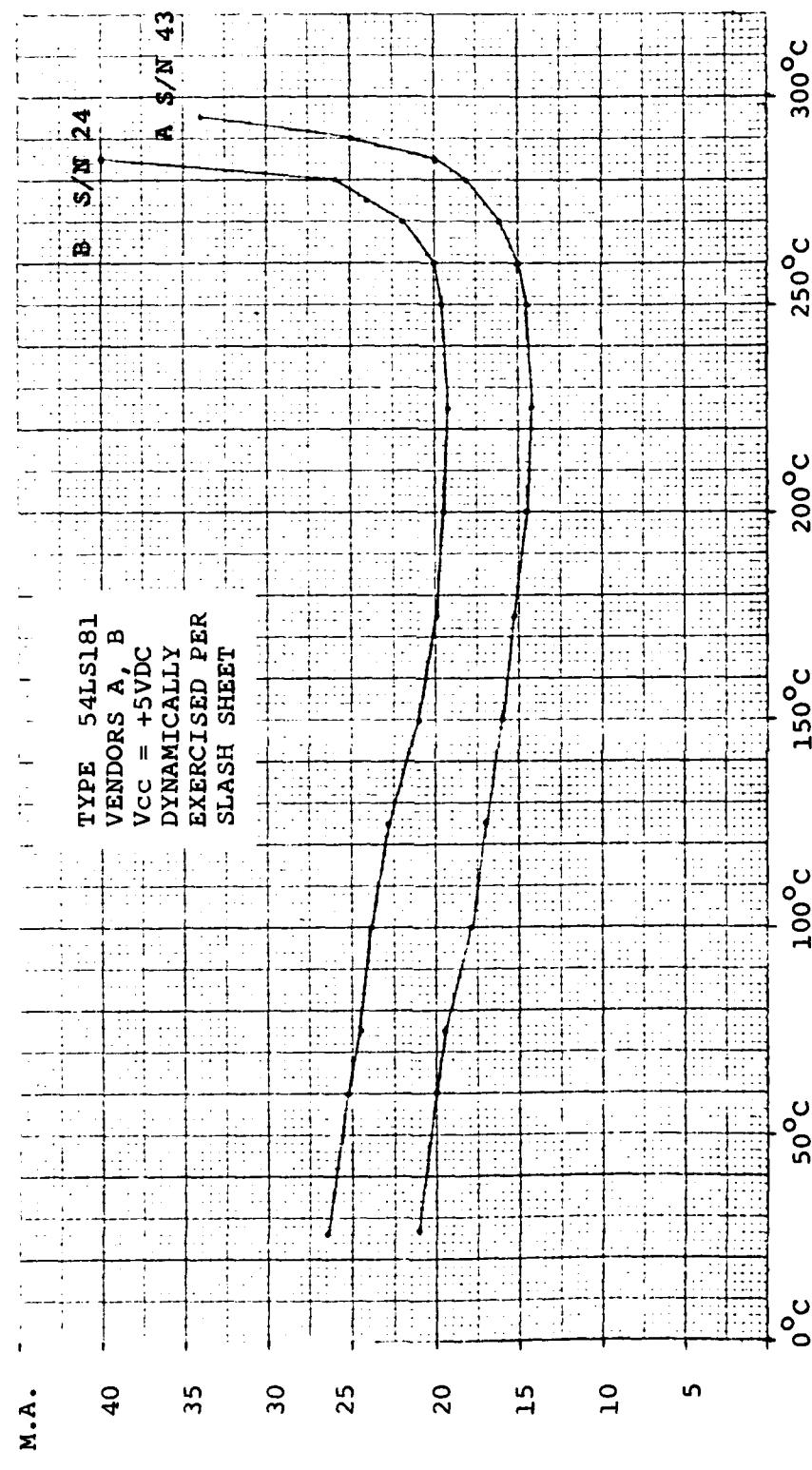


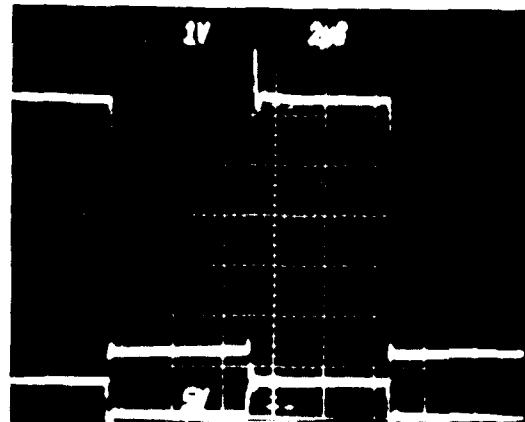
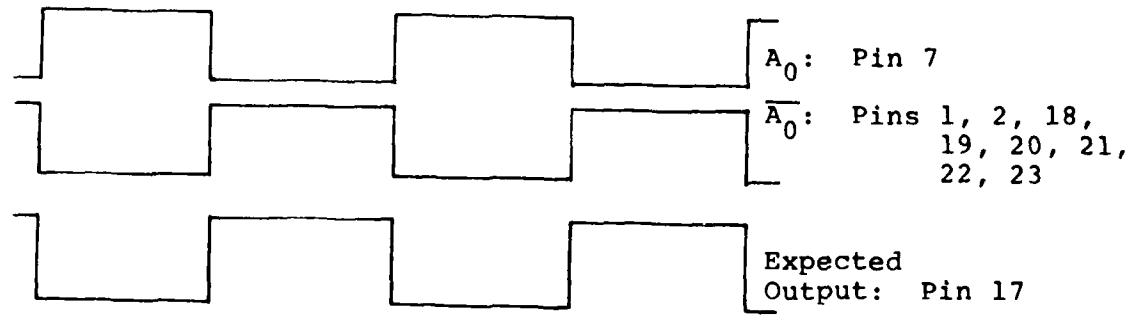
Figure 16: 54LS181, Icc vs. Temperature

Table 16. Device Latching Results

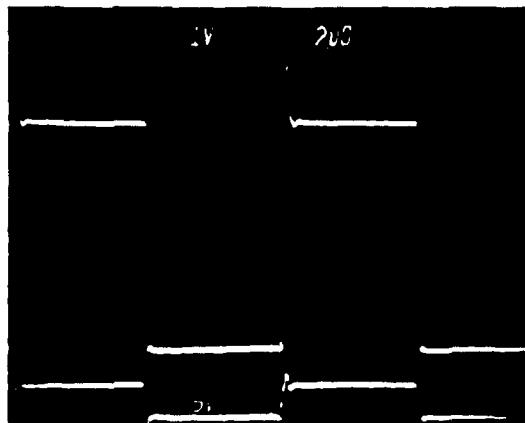
VENDOR/TYPE	TEMP IN °C TO RESULT IN:		
	INCORRECT LOGIC	I CC STEP INCREASE	OUTPUT LATCH
A LS181	+295	+295	+295
B LS181	+275	+285	+275
A LS191	+285*	+260	+260
B LS191	+265*	+260	+260
A LS251	+265	+230	+300
B LS251	+300	+300	+300
A LS283	+240	+210	+240
B LS283	+200	120**, +210	+225
D LSRAM	+225	None	+230
C LSRAM	+250	None	+255

\*modified circuit, \*\* gradual increase observed

Note:  $V_{CC} = +5V$



$+25^\circ\text{C}$



$+285^\circ\text{C}$

Figure 17: High Temperature Response, Vendor A, 54LS181

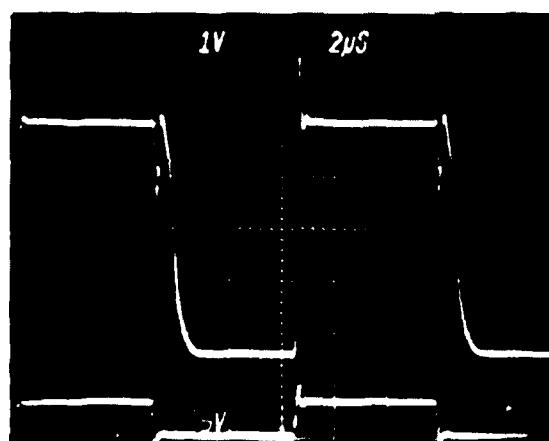
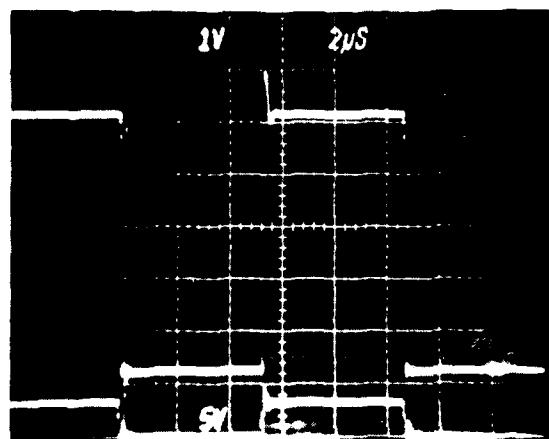
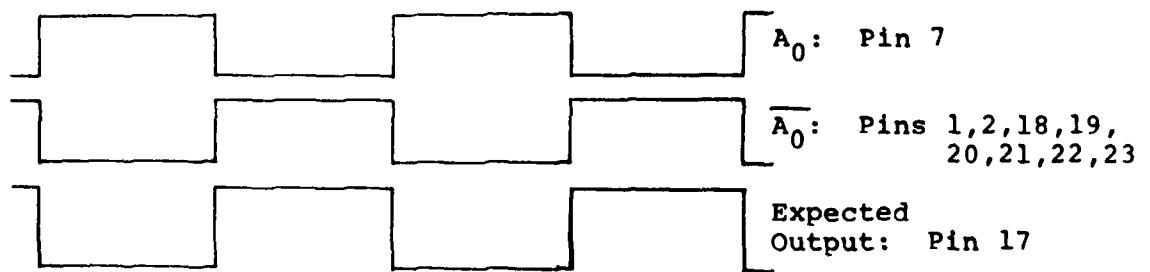
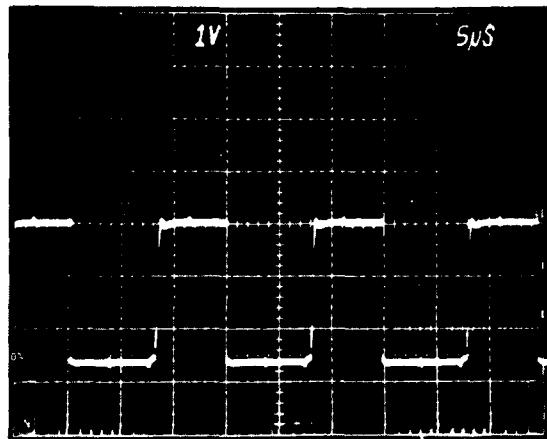
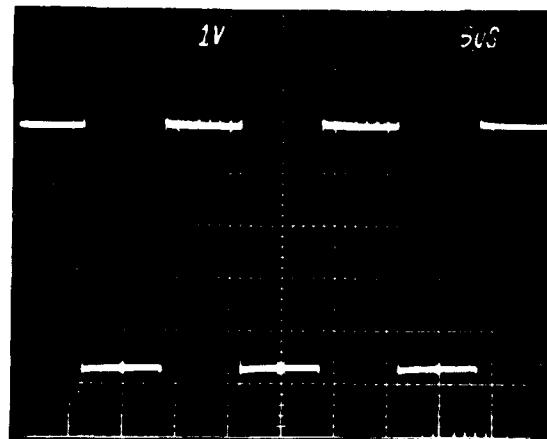
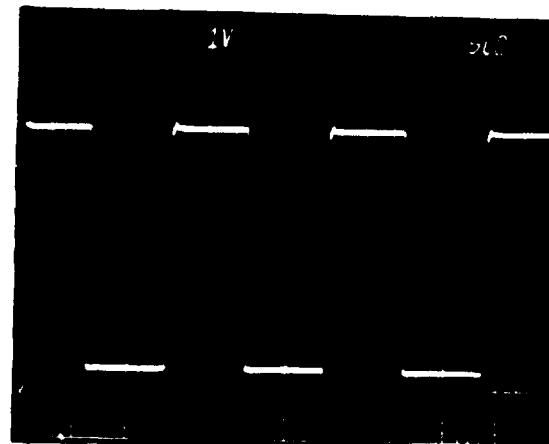
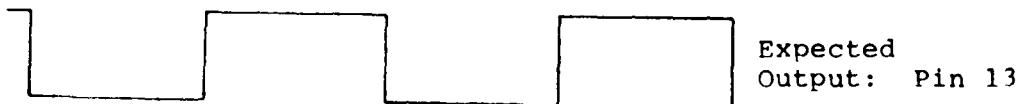


Figure 18: High Temperature Response, Vendor B, 54LS181

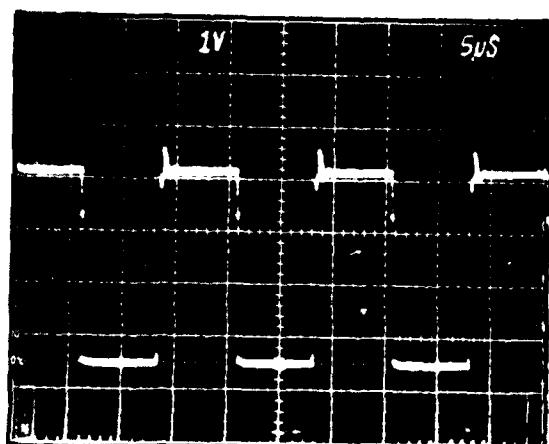


Note: Not exercised according to 38510 slash sheet, the difference being that the load pin is at ground. The worst output is shown and is still at acceptable logic levels at +285°C.

Figure 19: High Temperature Response, Vendor A, 54LS191



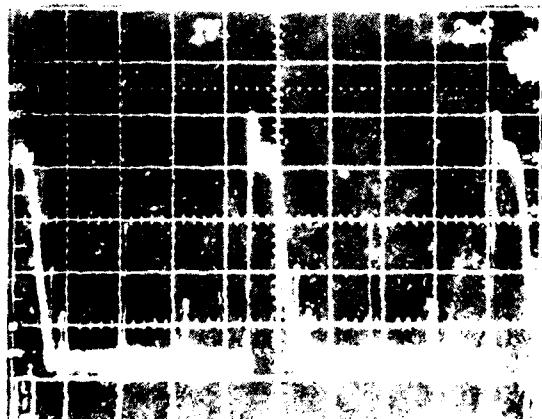
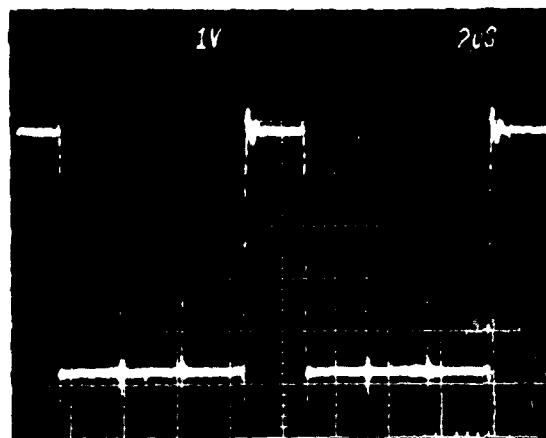
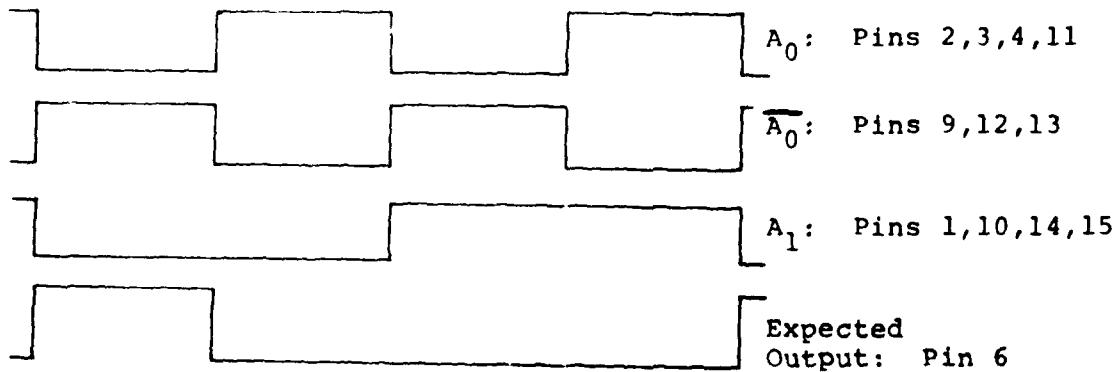
+25°C



+265°C

Note: Not exercised according to 38510 slash sheet, the difference being that the load pin is at ground. The worst output is shown and is still operating at acceptable logic levels at +265°C.

Figure 20: High Temperature Response, Vendor B, 54LS191



+265°C

Figure 21: High Temperature Response, Vendor A, 54LS251

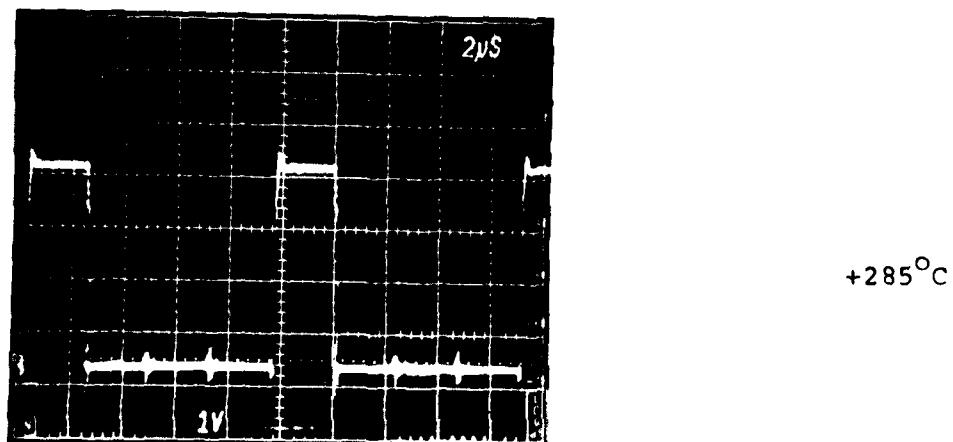
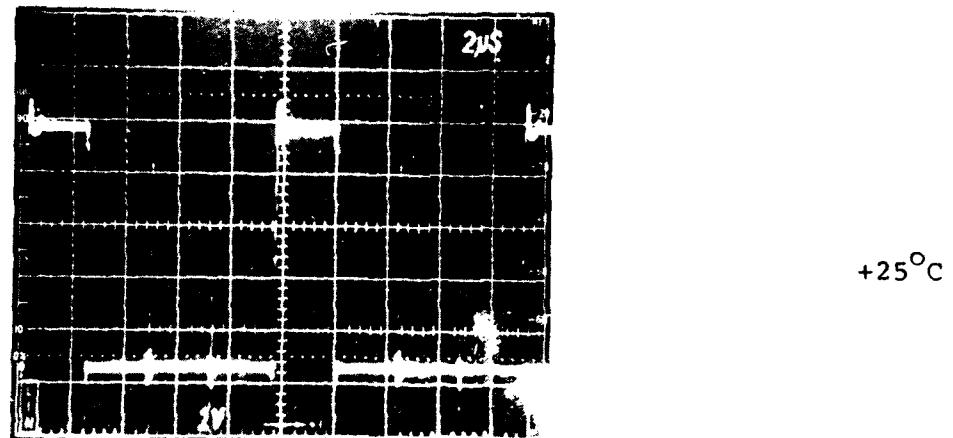
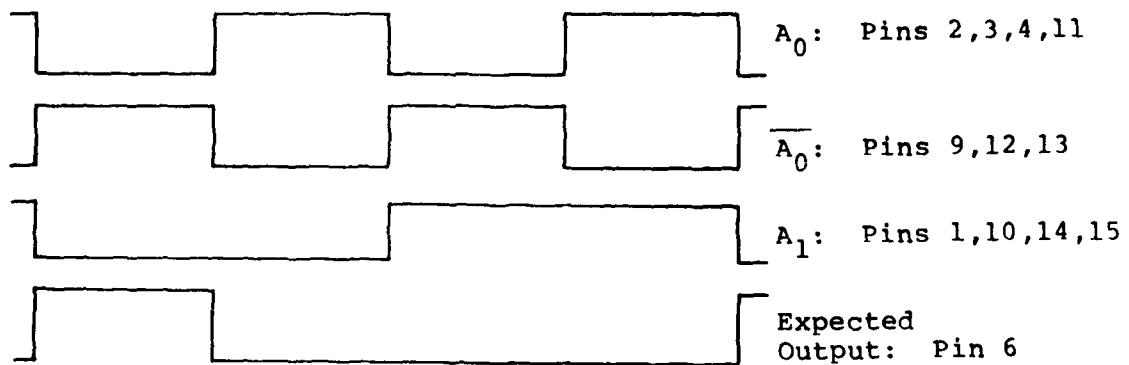
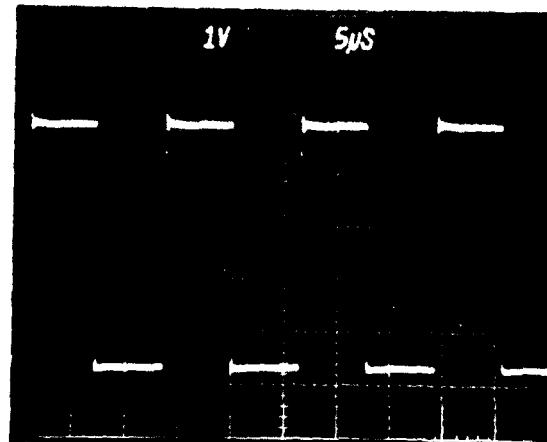
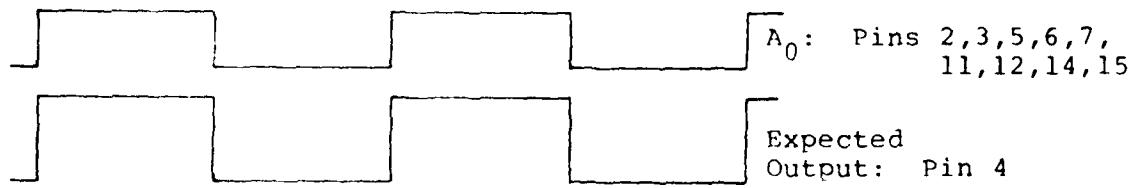
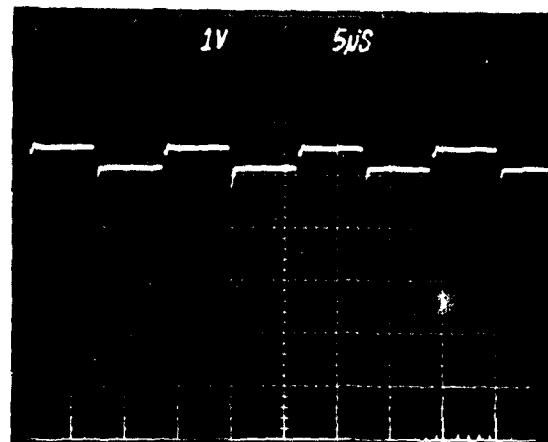


Figure 22: High Temperature Response, Vendor B, 54LS251

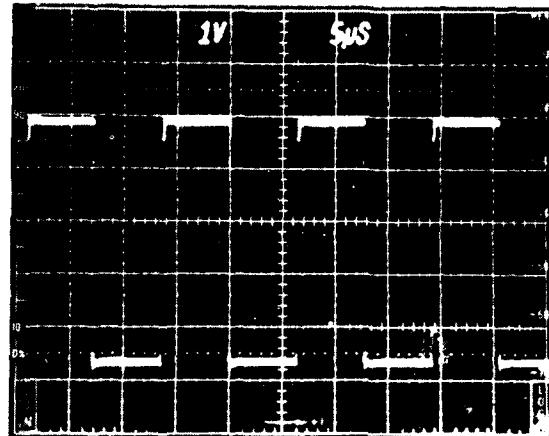
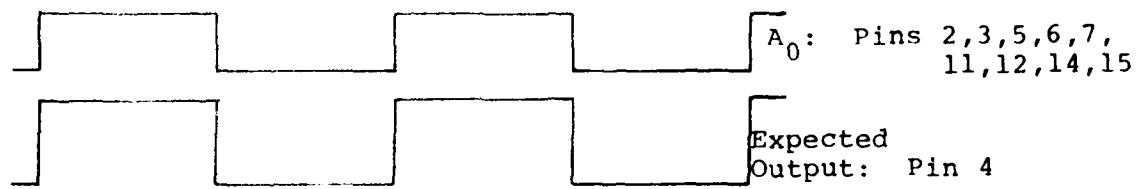


$+25^{\circ}\text{C}$

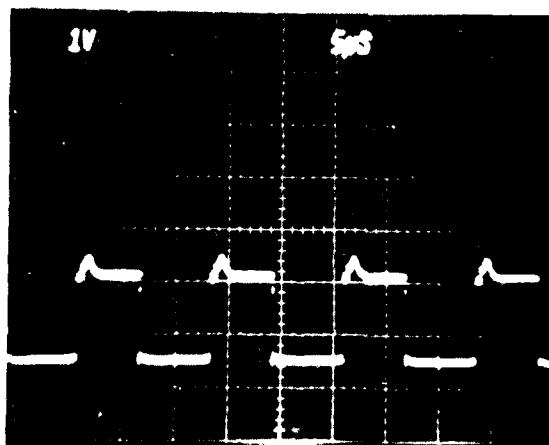


$+240^{\circ}\text{C}$

Figure 23: High Temperature Response, Vendor A 54LS283



+25°C



+200°C

Figure 24: High Temperature Response, Vendor B 54LS283

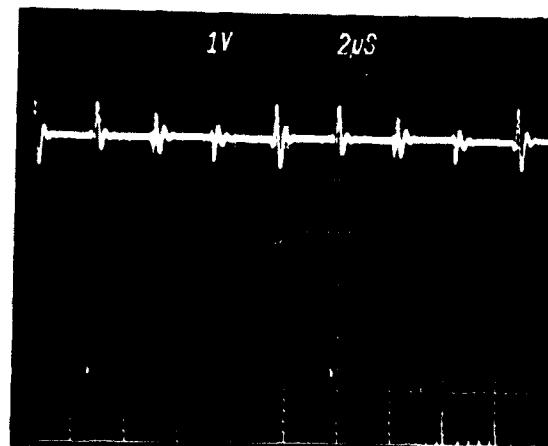
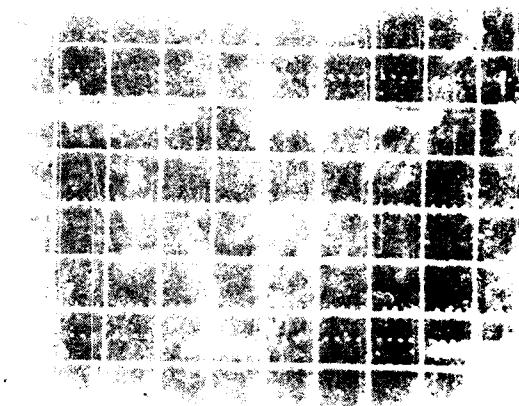
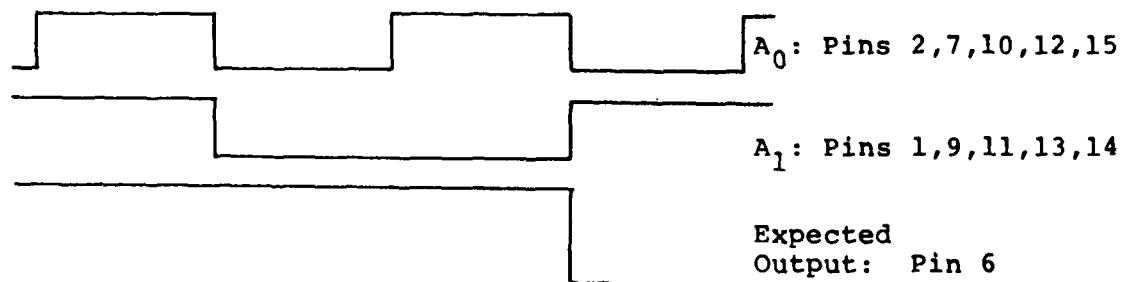


Figure 25: High Temperature Response, Vendor C's RAM.

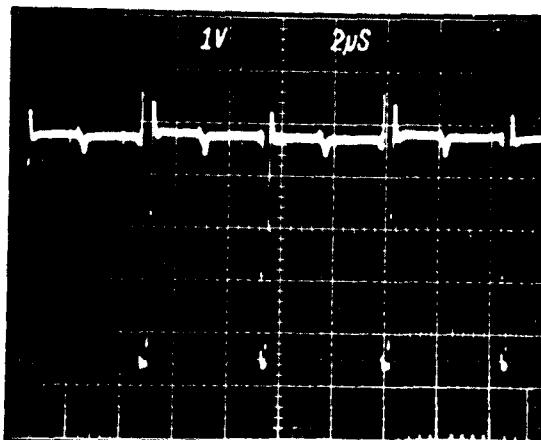
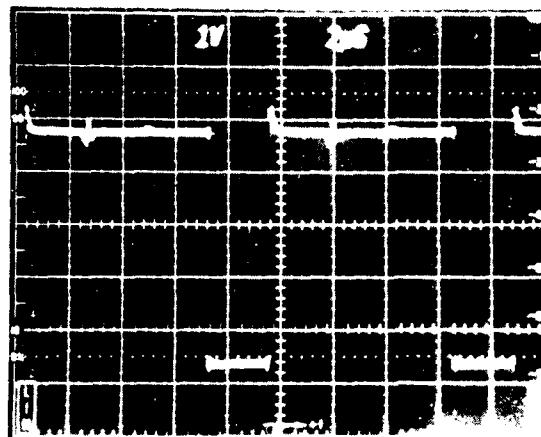
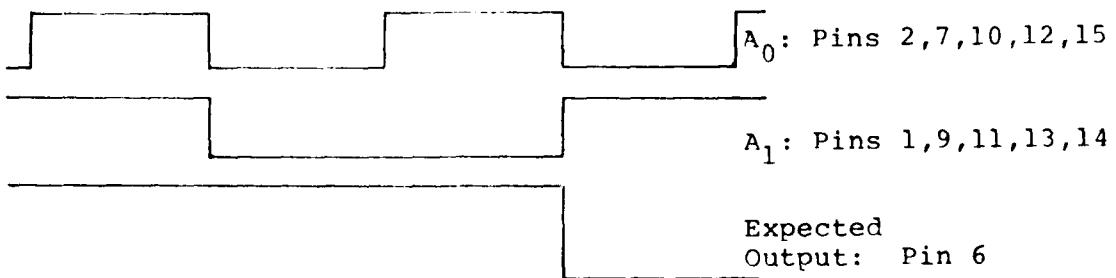


Figure 26: High Temperature Response, Vendor D's RAM.

### C. Step Stress Test

#### 1. Storage Step Stress

From both vendor types five devices each of the 54LS181, 54LS191, 54LS251 and ten units of the 54LS283 as well as the RAM's were subjected to high temperature storage step stress. The chosen starting temperature was +275°C and with 72 hour duration and 25°C increments the test was terminated at +350°C as the highest ambient temperature environment. All parts were initially data logged at +25°C and also at each high temperature storage end point. No failures were recorded during all end point testing.

Based on the obtained results, temperatures of +275°C, +300°C, and +325°C were set for long term high temperature storage.

#### 2. Operating Step Stress

The same number and types of devices as in the storage limit test above were subjected to dynamic operating step stress. The ambient environments for these tests were +225°C, +250°C, +275°C and +290°C to which the units were sequentially subjected for a duration of 72 hours each. Some of the devices already identified through the high temperature device performance tests were latched during the dynamic step stress and were drawing as much as five times the normal (room temperature) current at the highest temperature environment. All devices, however, passed every electrical end point measurement. From the results of the operational step stress, as well as the latching tests, temperatures of +200°C, +225°C and +250°C were chosen for the long term high temperature operational life test. Device types anticipated to be latched and/or in a higher current mode were included at the temperatures indicated above during the long term accelerated life test. It is to be pointed out that each burn-in position except those for the RAM's included a limiting resistor in its' Vcc line. RAM burn-in positions were fused with ½A fuses having a resistance of approximately 3 ohms.

The inclusion of these latched devices at these test temperatures was to compare the test results to those in a non-latched mode.

#### D. Long Term Life Test

##### 1. Storage Long Term Life

Long term storage life tests were conducted according to the test plan in Table 1. This shows that only one device type from each of the four vendors with ten units in each cell was included in the test, 54LS283 from vendors A and B and the RAM's from vendors C and D. The ambient environments of the storage life tests were +275°C, +300°C, and +325°C.

All devices were initially tested and parameters data logged at +25°C, -55°C and +125°C. Electrical end point tests of all device parameters again were data logged on magnetic tape (+25°C only) at accumulated times of 8, 32, 64, 128, 250, 500, 1000, 2000, 3000, and 4000 hours. Device failures during long term storage and detected at room ambient electrical test occurred on three device types only: Vendor A's 54LS283, Vendor B's 54LS283 and Vendor D's RAM. The detailed results are summarized in Table 17.

Table 17:  
High Temperature Storage Results

Accumulated Time (hrs)	Ambient Environment		
	325°C	300°C	275°C
4	*	*	*
8	0	0	0
16	*	*	*
32	0	0	0
64	0	0	0
128	0	0	0
250	1-283A	0	0
500	0	0	0
1000	0	0	0
2000	1-283A	0	0
3000	0	0	0
4000	2-283B 1-RAMD	0	0

Note: \* - No end point test performed  
 0 - Zero failures observed at end point

Temperature extreme testing at  $-55^{\circ}\text{C}$  and  $+125^{\circ}\text{C}$  after completion of high temperature long term storage revealed ten access time failures out of ten devices for Vendor C's RAM. These units were from the highest temperature environment. The failure mechanism was found to be lifting chips resulting from softening of the gold-silicon eutectic. Physical verification of all types subjected to the same ambient environment for the 4000 hour duration showed chip separation had occurred on all vendor types except for vendor D RAM. This is the only device making use of Au/Ni/Mo in the die-package interface.

Since this failure mechanism was only observed at devices in the  $+325^{\circ}\text{C}$  ambient environment and no evidence was found on units in the  $+275^{\circ}\text{C}$  and  $+300^{\circ}\text{C}$  temperature cells it was considered induced and excluded from any failure rate calculation. Failure rate calculations are based on extrapolated median lifetime at the life test temperature; then through a regression curve following an Arrhenius relationship median lifetimes at the maximum storage temperature were obtained. The failure rate calculations follow Bell Telephone (D.S. Peck) publications 1. Because of the lack of real time failures experienced during the test phase the following assumptions were made in order to perform failure rate calculations.

- a) A standard deviation of  $\sigma = 1.0$  typical for a matured and reliable product.
- b) An activation energy of  $E_a = 1.0\text{eV}$  was used for worst case calculations.
- c) One device failure was assumed at the end of the storage life test at the  $300^{\circ}\text{C}$  temperature environment and with the already assumed standard deviation of  $\sigma = 1.0$ , median times to failure were calculated.

Through extrapolation a median time to failure of  $1.45 \times 10^5$  hours at  $300^{\circ}\text{C}$  was calculated. At an ambient of  $+150^{\circ}\text{C}$  equal to the maximum storage temperature of these devices at  $10^5$  hours the anticipated failure rate would be less than .001 failure per  $10^6$  hours.

## 2. Operating Life Test

The long term operating life test was performed at three temperatures of +200°C, +225°C and +250°C with 35 devices per cell for both vendor A and B's 54LS283 as well as vendor C and D's RAM's; all other devices were represented with 10 devices each.

Table 18 shows the quantity of devices stressed and which devices were expected to be latched at the various temperatures based upon previous high temperature measurements.

Table 18  
Expected device performance at chosen ambient environment.

Vendor	Type	T <sub>1</sub> = 250°C	T <sub>2</sub> = 225°C	T <sub>3</sub> = 200°C
A	54LS181	10	10	10
B	54LS181	10	10	10
A	54LS191	10	10	10
B	54LS191	10	10	10
A	54LS251	10	10	10
B	54LS251	10	10	10
A	54LS283	(35)	35	35
B	54LS283	(35)	(35)	(35)
D	RAM	(35)	(35)	35
C	RAM	(35)	35	35

Note: X - device assumed operational, no excessive I<sub>CC</sub> expected

(X) - devices expected to be latched and possibly draw excessive current

For non-latched devices, junction temperatures were calculated for each ambient environment and are shown in Table 2. End point tests in which all electrical parameters were data logged on magnetic tape at +25°C commenced at 8, 16, 32, 64, 128, 250, 500, 1000, 2000, 3000 and only for the 200°C ambient environment also at 4000 hours.

The life test results are summarized in Table 19. This data basically shows device failures only for those types previously identified in a latched condition. The only other failure recorded at 8 hours in the +250°C environment (vendor A 54LS181) was considered an early life failure and therefore, not included in any failure rate prediction.

Meaningful predictions therefore are only possible for those six device types known to be operational during the accelerated life test. Also in the operating life test due to the absence of failures the following assumptions were made:

- a) a standard deviation of  $\sigma = 1.0$
- b) one device failure was assumed at the end of the highest (+250°C) operating life environment and with  $\sigma = 1.0$ , times to failure was obtained.
- c) an activation energy of  $E_a = 1.0\text{eV}$  for surface related problems was used for worst case calculations.

The resulting instantaneous failure rate for all of the following devices: 54LS181, 54LS191 and 54LS251 from both vendors A and B when calculated at  $10^5$  hours (11 years) can be stated as less than .001 failures per  $10^6$  hours. These figures are considerably better than the constant failure rates obtained from prediction methods in MIL-HDBK-217B.

Failure rates for those devices latched during the performance of the operating life test were not calculated since as a result of the latched condition high current densities at random device nodes induced electromigration damage of varying severity.

Table 19: High Temperature Dynamic Operation Results

Accumulated Time/Hrs	Ambient Environment		
	250°C	225°C	200°C
8	1-181A	0	0
16	0	*	*
32	2-RAMD	0	1-RAMD
	1-RAMC		
64	2-RAMD	1-RAMD	0
128	0	4-RAMD	0
250	0	1-RAMD	0
500	1-283A	1-RAMD	0
1000	1-RAMD	0	1-RAMD
2000	1-283; 4-283A; 5-RAMD	4-RAMD	1-RAMD
3000	4-283A; 8-RAMD	2-283A; 10-RAMD	0
4000	XX	XX	1-RAMD

Notes: \* - No end point test performed

0 - Zero failures observed at end point

XX - Operational life test concluded at 3000 hours

## VI. CRITERIA FOR FAILURE AND FAILURE ANALYSIS

### A. Failure Definition

Devices rejected during electrical room ambient end point testing at the Macrodata MD 501 from high temperature storage or high temperature operational life. The chosen failure criteria were non-conformance to the minimum and maximum limits of the tests identified in the appropriate slash sheets or vendor specifications as previously discussed, and parameter change of greater than 10% of the total range. A deviation from initial values of greater than 10% was also applied to devices originally outside the specified parameter limits.

Test system repeatability was verified through the use of control device printouts prior to the initiation of any end point testing. Units marginally exceeding the described rejection criteria were logged as failures at that end point but continued the long term accelerated testing. At the conclusion of the life testing the failed devices were grouped by similar failure symptoms, parameter failures verified by bench testing, and submitted to physical analysis.

### B. Major Failure Modes and Mechanisms

#### 1. Electromigration

The predominant failure mechanism for devices rejected during accelerated operational life test was found to be electromigration.

Electromigration is defined as mass transport of aluminum metal by momentum exchange between thermally activated aluminum ions and conducting electrons. The aluminum ions travel in the direction of electron flow resulting in hillock and void formation in the aluminum stripe. The net ionic flux,  $J_{ion}$  is given by

$$J_{ion} = (ND/kT) (Ze) \rho J,$$

after Huntington and Grone<sup>2</sup>, where

N = density of ions

D = D<sub>0</sub> exp (-Q/kT), the diffusion coefficient,  
where Q = the activation energy for diffusion

$k$  = Boltzmann's constant  
 $T$  = absolute temperature  
 $Ze$  = the effective electric charge of the migrating ion, and  
 $\rho$  = the resistivity of the conductor  
 $J$  = current density

This expression is applicable to bulk single crystals for which  $Q$  and  $D$  are well defined. However,  $Q$  and  $D$  are not as well defined for polycrystalline films.

Model calculations carried out by Black<sup>3</sup> and others<sup>4</sup> have determined mean time to failure (MTF) versus current density  $J$  and absolute temperature  $T$  to be expressible as:

$$MTF = A j^{-n} \exp (-Q/kT),$$

where:  $A$  = a constant dependent upon geometry and structure  
 $1.0 < n < 3.0$   
 $Q$  = the appropriate activation energy

Factors influencing MTF other than  $J$  and  $T$  include current density gradient, temperature gradient, grain size microstructure, geometry, and the presence and nature of a glass coating over the chip surface.

The failure modes associated with the observed electromigration included output voltage high  $V_{OH}$  failures, propagation delay  $t_p$  failures, input low current ( $I_{IL}$ ) failures, and supply current  $I_{CC}$  failures. All could be explained by voids in the aluminum metallization, often by voids seen in  $V_{CC}$  runs supplying current to critical places on the chip.

For example, S/N 106 of Vendor D's RAM failed  $V_{OH}$ ,  $V_{OL}$ , and  $I_{OS}$  (pin 6),  $I_{IL}$  (pins 7 and 9), and propagation delays (pins 6 and 12) after 2000 hours of life test at 225°C. Functional bench testing verified the failures, and when the device was opened, extensive, random electromigration was seen. Figure 1 shows a void in the  $V_{CC}$  run supplying the Q20's (see Appendix J, Figure 7), which resulted in  $V_{OH}$ ,  $V_{OL}$ , and  $I_{OS}$  failures, and also contributed to the propagation delay failures. Figure 2 is a dark field photograph showing the same

region after the glass was etched, and Figure 3 was taken subsequently using the scanning electron microscope (SEM). Similar damage was seen in the ground runs to the emitters of Q9 and Q<sub>12</sub> in the input structure associated with pin 7 and with the respective transistors in the input structure associated with pin 9. Opens or high emitter resistances due to voids in these ground runs accounted for the I<sub>IL</sub> failures at these pins. Figures 4, 5, and 6 show this damage.

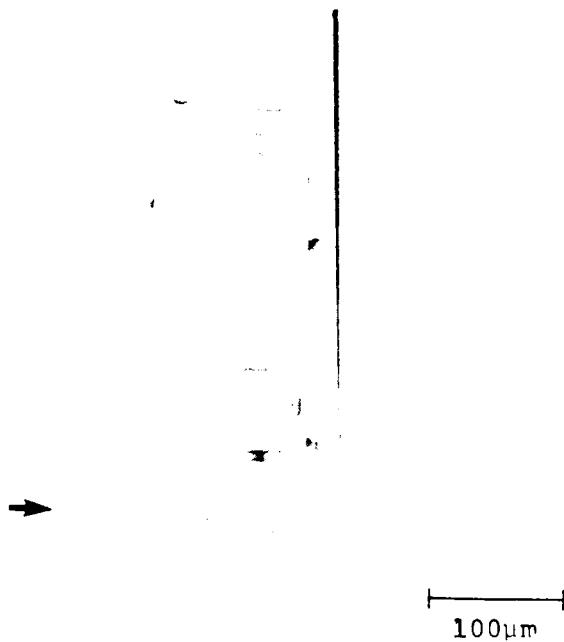


Figure 27. Void (arrow) in VCC run supplying the Q<sub>20</sub>'s on Vendor D's RAM, S/N 106, date code (dc) 7626, operating life failure after 2000 hours at 225°C. Void resulted in VOH, VOL, and IOS failures at pin 6. (reversed image).

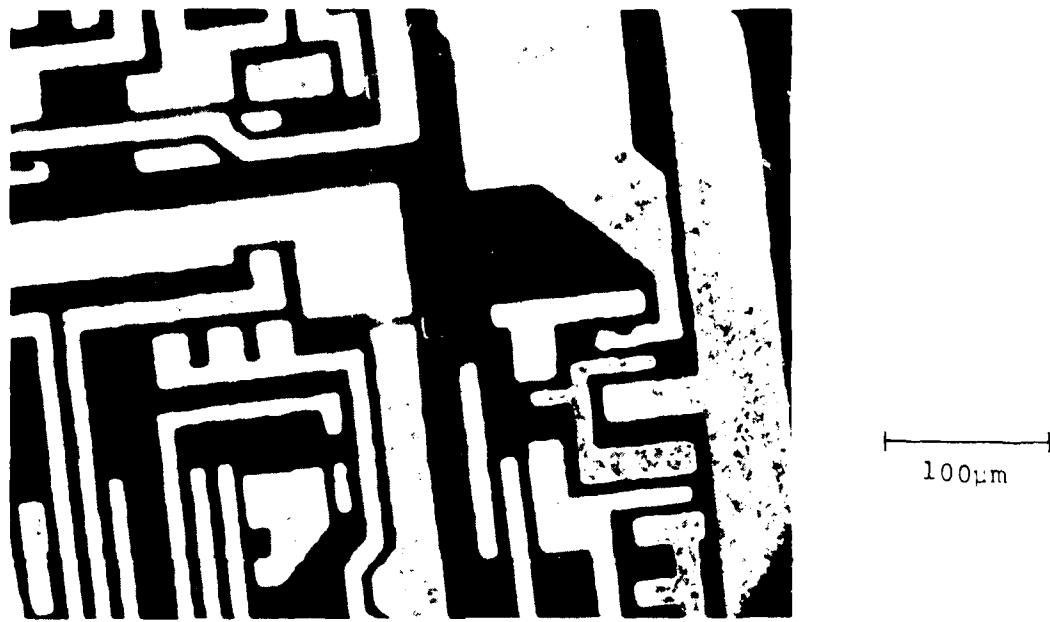


Figure 28. Vendor D's RAM, S/N 106, dc 7626, operating life, failed post 2000 hours at 225°C. Darkfield view of void shown in Figure 27 after glass etch.



Figure 29. Vendor D's RAM, S/N 106, dc 7626, operating life, failed post 2000 hours at 225°C.  
SEM photograph of void shown in Figures 27 and 28 after glass etch.

**Figure 30.** Vendor D's RAM, S/N 106, dc 7626, operating life, failed post 2000 hours at 225°C.  
Optical photomicrograph showing electromigration damage (arrow) in ground run associated with pin 9 input structure. (reversed image).



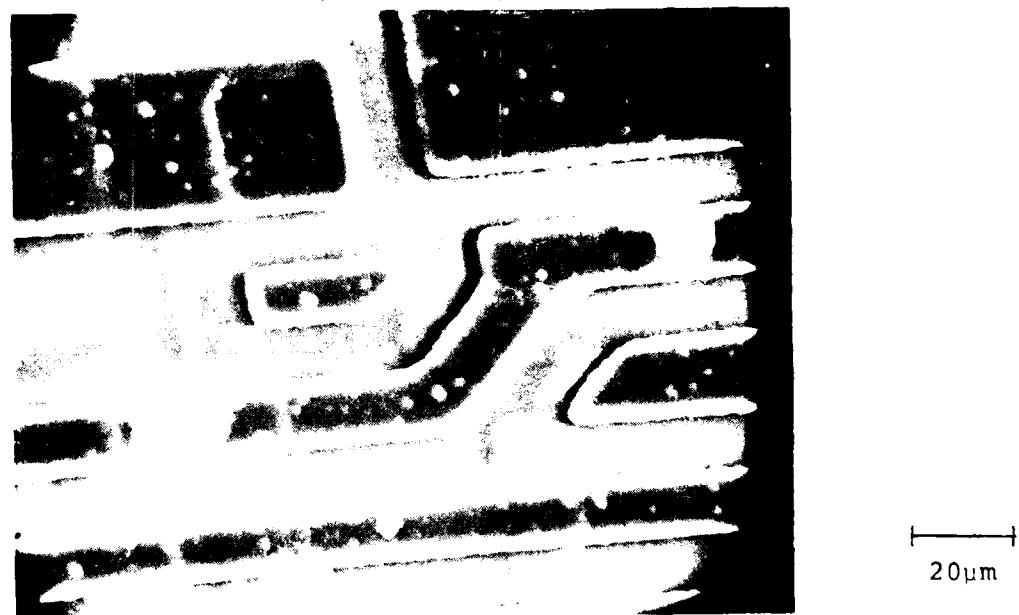


Figure 31. Vendor D's RAM, S/N 106, dc 7626, operating life,  
failed post 2000 hours at 225°C.  
SEM photograph of electromigration damage in ground  
run shown in Figure 30.

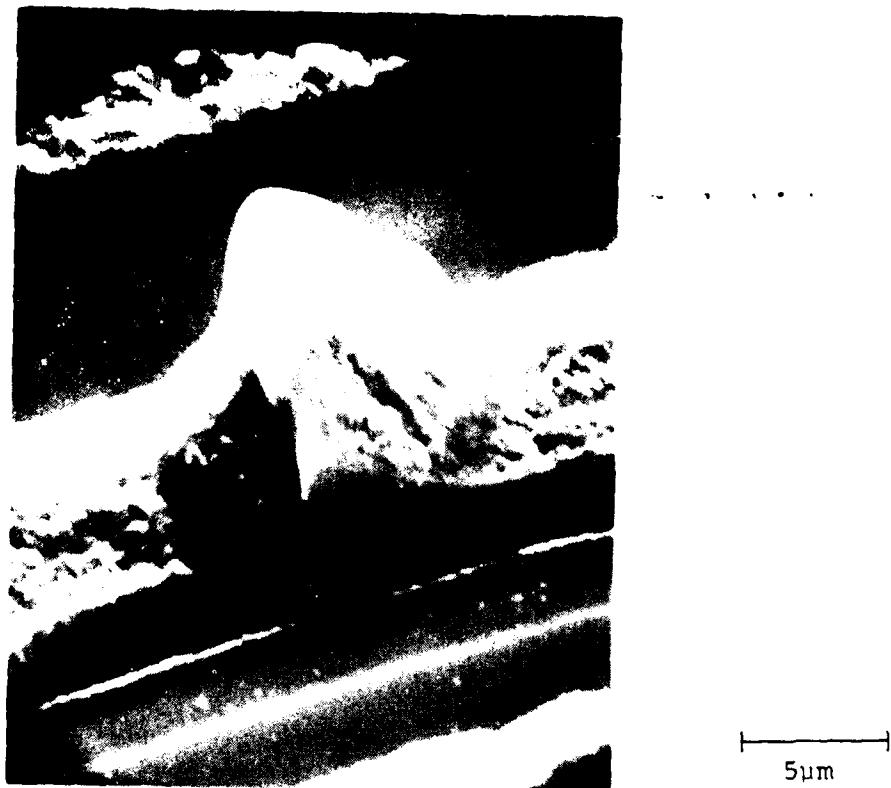


Figure 32. Vendor D's RAM, S/N 106, dc 7626, operating life, failed post 2000 hours at 225°C.  
SEM photograph of hillock caused by electromigration in ground run associated with pin 9 input structure taken after glass etch.

Similar damage was seen on all of vendor D's RAMs opened during the analysis. At least one failed device was opened from each failure group and each temperature environment. Extensive random electromigration was seen on all devices of this type whether the units were categorized as failures or actually still passed electrical end point specifications. An example of this was seen on S/N 86. Figure 7 shows electromigration damage which caused the input low current ( $I_{IL}$ ) failure at pin 7. Figures 8 and 9 show other electromigration damage which, although quite advanced, had not caused failure by the end of 3000 hours of life test at 225°C.

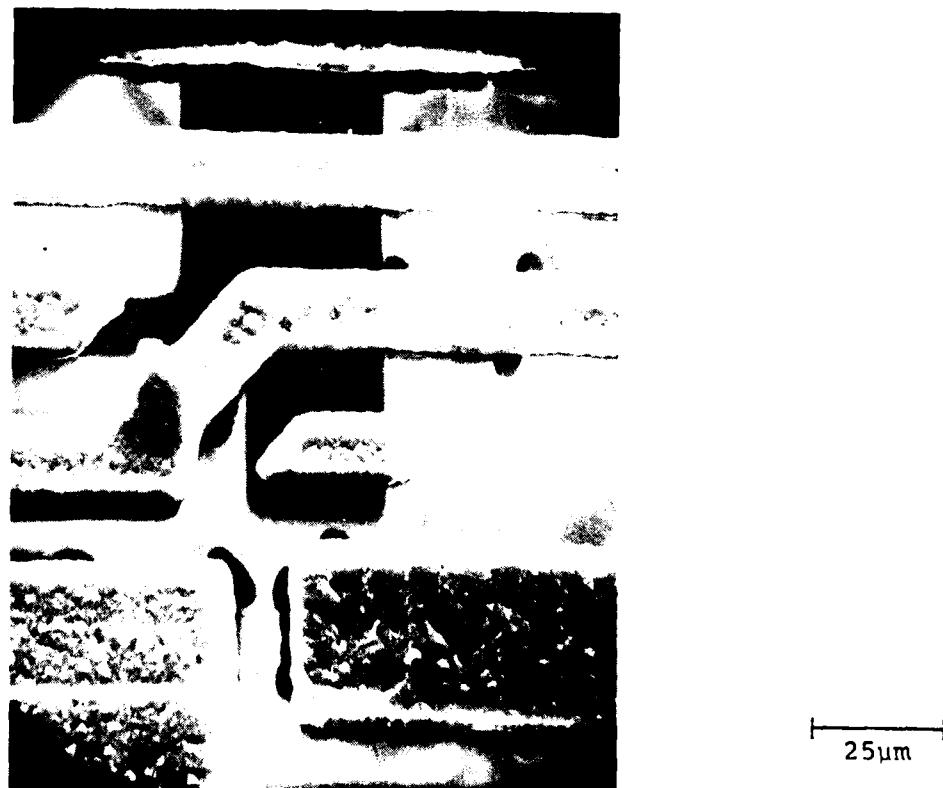


Figure 33. Vendor D's RAM, S/N 86, dc 7626, operating life, failed post 3000 hours at 225°C. SEM photograph of hillocks in ground metallization run associated with pin 7 input structure. Electromigration damage caused input low current failure.

THIS PAGE IS BEST QUALITY PRACTICABLE  
FROM COPY FROM 100% TO 95%



Figure 34. Vendor D's RAM, S/N 86, dc 7626, operating life, failed post 3000 hours at 225°C. SEM photograph of voids in V<sub>CC</sub> run which had not yet caused failure.

THIS PAGE IS DRAFT QUALITY PRACTICABLE  
FROM GSA FEDERAL PURCHASE CARD



Figure 35. Vendor D's RAM, S/N 86, dc 7626, operating life, failed post 3000 hours at  $225^{\circ}\text{C}$ . SEM photograph showing hillocks in emitter metallization of output had not yet caused failure after operating test at  $225^{\circ}\text{C}$  for 3000 hours.

No failure was recorded for vendor C's RAM with the exception of one unit considered an early life failure. It should be pointed out that these devices also were latched during operational life test. One of these, units, S/N 31 from the highest temperature environment after 3000 hours accelerated life test was opened for visual inspection . Electromigration of the aluminum was seen on this device as well. The lack of failures was attributed to the presence of the Ti-W barrier metallization, which preserved electrical continuity even after the aluminum had migrated.

For vendor A's 54LS283, random formation of voids and hillocks was observed also and occurred both in places where they were severe enough to cause device failure and other places where they did not. Several failure-inducing voids and hillocks in the VCC runs of S/N 44 were photographed and are shown in Figures 10 though 13. The damage shown is representative of that seen on other failed devices of this type. One device (S/N 27) of this type from the highest temperature/longest time ( $250^{\circ}\text{C}/3000$  hours) category which had not failed was opened. Inspection revealed that extensive, random, electromigration had occurred here also, but evidently not yet to the extent to cause failure.

THIS PAGE IS DRAFT QUALITY PRACTICABLE  
FROM CQI Y FOLIO 10000000000000000000000000000000

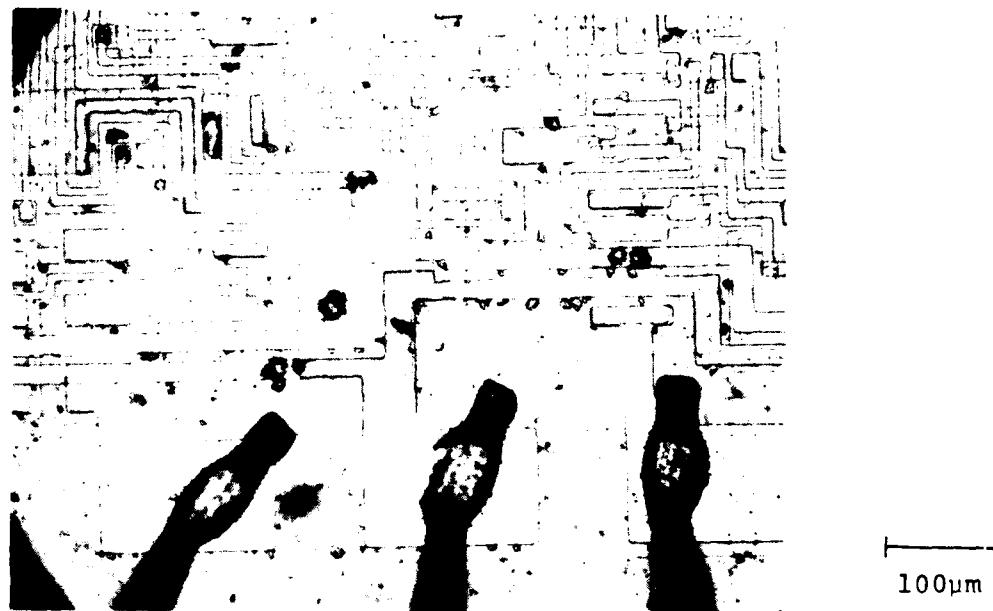


Figure 36. Photomicrograph showing electromigration damage to V<sub>CC</sub> run (arrow) on vendor A's 54LS283, S/N 44, dc 7732, operating life, failed after 2000 hours at 250°C. (reversed image).

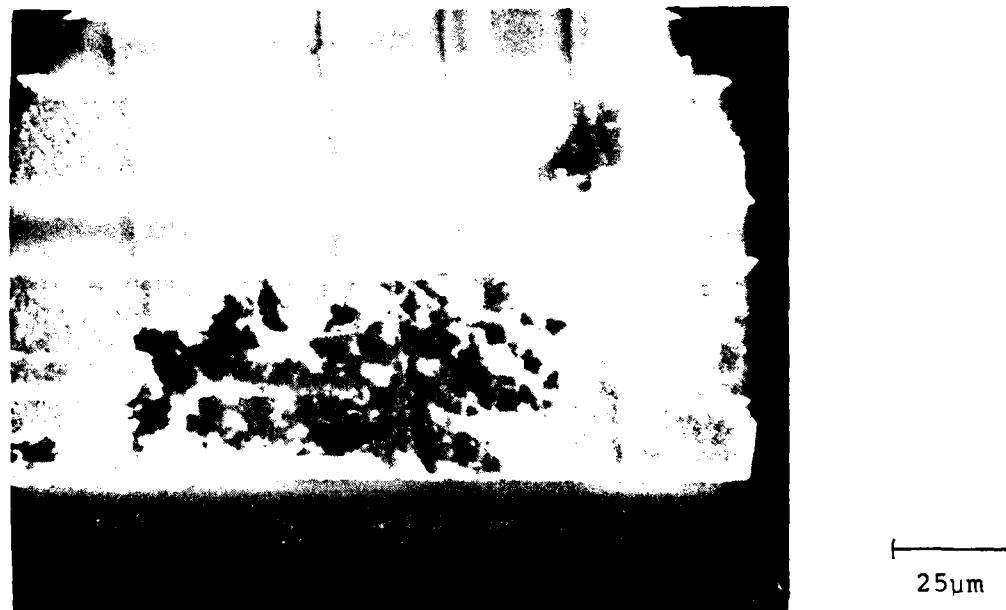


Figure 37. Vendor A's 54LS283, S/N 44, dg 7732, operating life, failed post 2000 hours at 250°C. SEM photograph of voids in VCC metallization run.



A horizontal scale bar consisting of a short vertical line at each end of a longer horizontal line, representing 50 micrometers.

50 $\mu$ m

Figure 38. Vendor A's 54LS283, S/N 44, dc 7732, operating life, failed post 2000 hours at 250°C.  
SEM photograph of hillocks in VCC run.



10 $\mu$ m

Figure 39. Vendor A's 54LS283, S/N 44, dg 7732, operating life, failed post 2000 hours at 250°C. SEM photograph of hillocks in V<sub>CC</sub> run.

One device of vendor B's 54LS283, S/N 55, failed after 2000 hours operating life test at 250°C. The failure mode (functional failure) and mechanism (electromigration) were identical to those seen in the eleven failures of vendor A's equivalent.

Since an equal number of devices from both vendors were on operating life test for equal times and temperature, the more frequent occurrence of failure of vendor A's unit was attributed to its thinner, narrower metallization. The cross-sectional area of vendor A's metallization was found to be  $9 \times 10^{-8} \text{ cm}^2$ , while that of vendor B's was  $15 \times 10^{-8} \text{ cm}^2$ . Hence the current density of vendor A's device would have been approximately 2/3 greater than that of vendor B's device given identical current distributions while latched.

One unit of vendor B's 54LS283, S/N 20, which had survived operating life test for 3000 hours at 250°C, was opened. Inspection revealed that extensive, random electromigration had occurred here also, but not yet to the extent of failure.

## 2. Chip Separation from Package

All 54LS283's of both vendors as well as vendor C's RAM which failed electrical end point test at room ambient or final electrical test at temperature extremes were from the highest (+325°C) storage environment. The recorded failures included output voltages, input leakage current, and  $I_{CC}$  failures. After verifying the failures on the bench, the devices were opened and the chip was found separated from the package. A SEM view of this is shown in Figure 40, with a detailed view of one corner of the chip shown in Figure 41.

Removal and cross-sectioning of the chip revealed two significant facts. Almost all of the gold had lifted from the package with the chip, and there were large glass particles in the gold. Once the chip was aloft, physical effects of handling and loss of heatsinking contributed to device failures.

It should be noted that several devices of types identified above from the same time/temperature environment which passed all electrical tests were also opened for examination. The chips were found separated on every unit inspected. Therefore it can be assumed that all 54LS283's of both vendors as well as vendor C's RAM exposed to +325°C storage for 4000 hours resulted in chip separation.



Figure 40. Vendor B 54LS283, S/N 140, dc 7741, +325°C storage,  
failed at post 4000 hours. SEM photograph showing  
separation of chip from package.

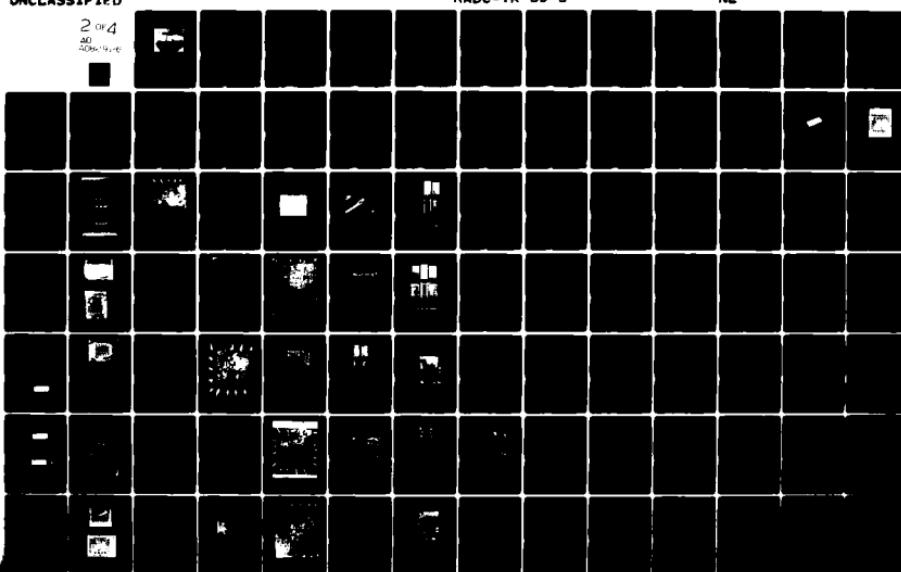
AD-A082 926 RAYTHEON CO BEDFORD MA MISSILE SYSTEMS DIV F/6 9/3  
RELIABILITY EVALUATION OF LOW POWER SCHOTTKY CLAMPED MICROCIRCUIT--ETC(U)  
FEB 80 K B LASCH, D BARTELS, J J SPINALE F30602-77-C-0186

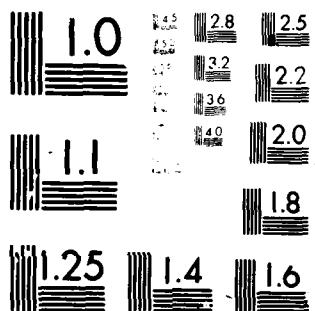
UNCLASSIFIED

RADC-TR-80-5

NL

2 or 4  
20  
400x14x6





MICROCOPY RESOLUTION TEST CHART  
NATIONAL BUREAU OF STANDARDS 1963?



200 $\mu$ m

Figure 41. Vendor B 54LS283, S/N 140, dc 7741, +325°C storage, failed at post 4000 hours. SEM photograph showing detailed view of one corner of chip separated from package.

Since all failures were the result of adhesive problems of the die attach it is appropriate to point out construction differences.

The chips were mounted using a silicon-gold eutectic, with a thick film gold paste providing the gold. This thick film gold paste contained minute glass particles which were fired into the ceramic at approximately 920°C, thus providing the adhesion to the ceramic substrate. This basic construction was used by vendors A, B and C, for which identical failures were observed. Vendor D used a different package metallization in the die attach area resulting in no failures of this nature. Here the metallization scheme was Au/Ni/Mo, with the molybdenum providing the adhesion to the ceramic substrate.

#### C. Failure Analysis Summary

Devices which failed during the performance of the study were grouped at the conclusion of accelerated testing by device type, environment and failure symptoms, and failure mechanisms were identified. All pertinent data is shown in Table 20.

TABLE 20: LISTING OF LOW POWER SCHOTTKY TTL REJECTS

Vendor	Device Type	Unit No.	Date Code	Life Test	$T_A$ ( $^{\circ}$ C)	Hours To Failure	Pin No. (s) Failed	Failure Mode	Failure Mechanism
D	RAM	38	7626	Operating	250	2000	6,12	E	EM
D	RAM	43	7626	Operating	250	32	6	A,D	EM*
D	RAM	47	7626	Operating	250	2000	6,12	E	EM
D	RAM	48	7626	Operating	250	3000	6,12	E	EM
D	RAM	49	7626	Operating	250	2000	6,7,9, 10,11,12	A,B,C, D,E	EM
D	RAM	50	7626	Operating	250	2000	6,12	E	EM
D	RAM	51	7626	Operating	250	64	16	F	EM*
D	RAM	52	7626	Operating	250	2000	6,7,9,12	A,B,C, D,E	EM
D	RAM	53	7626	Operating	250	3000	6,12	E	EM
D	RAM	54	7626	Operating	250	3000	6,12	E	EM
D	RAM	55	7626	Operating	250	128	6,12	E	EM*
D	RAM	56	7626	Operating	250	3000	6	A,D	EM
D	RAM	58	7626	Operating	250	3000	A11	B,G,H	EM
D	RAM	59	7626	Operating	250	1000	6	A,D	EM
D	RAM	60	7626	Operating	250	3000	6	A,D	EM
D	RAM	63	7626	Operating	250	64	2-7,9,11, 13-15	A,B,C	EM*
D	RAM	67	7626	Operating	250	3000	A11	A,B,C, D,E,G	EM
D	RAM	68	7626	Operating	250	3000	6,7,9,12	A,B,C, D,E	EM
D	RAM	69	7626	Operating	225	3000	6,12	E	

TABLE 2C LISTING OF LOW POWER SCHOTTKY TTL REJECTS  
(Continued)

Vendor	Device Type	Unit No.	Date Code	Life Test	T <sub>A</sub> (°C)	Hours To Failure	Pin No. (s) Failed	Failure Mode	Failure Mechanism
D	RAM	70	7626	Operating	225	3000	6,7,9,12	A,B,C, D,E	EM
D	RAM	73	7626	Operating	225	3000	6,7,9,12	A,B,C, D,E	EM
D	RAM	74	7626	Operating	225	3000	6,12	A,B,D,E	EM
D	RAM	75	7626	Operating	225	3000	6,12	A,B,D, E,H	EM
D	RAM	79	7626	Operating	225	3000	6,7,9,12	A,B,C, D,E	EM
D	RAM	80	7626	Operating	225	500	6,12	E	EM*
D	RAM	82	7626	Operating	225	3000	6,12	D	EM
D	RAM	83	7626	Operating	225	128	1,6,12	E,I	EM*
D	RAM	86	7626	Operating	225	3000	7	C,I,J	EM
D	RAM	87	7626	Operating	225	128	6,12,15	C,E,I	EM*
D	RAM	92	7626	Operating	225	250	6,12	E	EM*
D	RAM	93	7626	Operating	225	3000	6	A	EM
D	RAM	94	7626	Operating	225	3000	6	A,D	EM
D	RAM	99	7626	Operating	225	3000	6,7,9,12	A,B,C, D,E	EM
D	RAM	101	7626	Operating	225	64	6,12	E	EM*
D	RAM	102	7626	Operating	225	128	6,12	E	EM*
D	RAM	104	7626	Operating	225	128	4,6,12	C,E,I,J	EM*
D	RAM	105	7626	Operating	225	2000	6,7,9,12	A,B,C, D,E	EM

TABLE 20: LISTING OF LOW POWER SCHOTTKY TTL REJECTS

(Continued)

Vendor	Device Type	Unit No.	Date Code	Life Test	T <sub>A</sub> (°C)	Hours To Failure	Pin No. (s) Failed	Failure Mode	Failure Mechanism
D	RAM	106	7626	Operating	225	2000	6,7,9,12	A,B,C, D,E	EM
D	RAM	107	7626	Operating	225	2000	6,12	E	EM
D	RAM	118	7626	Operating	200	2000	6,12	E	EM
D	RAM	133	7626	Operating	200	32	13	C,I,J	EM*
D	RAM	134	7626	Operating	200	1000	6,12	E	EM
D	RAM	140	7626	Operating	200	4000	6,12	E	EM
A	54LS181	20	7710	Operating	250	8	23	C	C
A	54LS283	12	7732	Operating	250	500	1,13	D,K	EM
A	54LS283	43	7732	Operating	250	3000	N/A	K	EM
A	54LS283	44	7732	Operating	250	2000	N/A	K	EM
A	54LS283	48	7732	Operating	250	2000	1,4,7,9, 10,13	A,C,D	EM
A	54LS283	50	7732	Operating	250	2000	N/A	K	EM
A	54LS283	51	7732	Operating	250	2000	N/A	K	EM
A	54LS283	55	7732	Operating	250	2000	N/A	K	EM
A	54LS283	58	7732	Operating	250	3000	N/A	K	EM
A	54LS283	62	7732	Operating	250	3000	N/A	K	EM
A	54LS283	76	7732	Operating	225	3000	N/A	K	EM
A	54LS283	84	7732	Operating	225	3000	N/A	K	EM
B	54LS283	55	7741	Operating	250	2000	N/A	K	EM
C	RAM	32	7744	Operating	250	32	6,12	E	C

TABLE 20: LISTING OF LOW POWER SCHOTTKY TTL REJECTS

(Continued)

Vendor	Device Type	Unit No.	Date Code	Life Test	T <sub>A</sub> (°C)	Hours To Failure	Pin No.(s) Failed	Failure Mode	Failure Mechanism
C	RAM	136	7744	Storage	325	4000	N/A	L	Chip Lifted
C	RAM	137	7744	Storage	325	4000	6,12	E	Chip Lifted
C	RAM	138	7744	Storage	325	4000	6,12	E	Chip Lifted
C	RAM	139	7744	Storage	325	4000	6,12	E	Chip Lifted
C	RAM	140	7744	Storage	325	4000	6,12	E	Chip Lifted
C	RAM	141	7744	Storage	325	4000	6,12	E	Chip Lifted
C	RAM	142	7744	Storage	325	4000	6,12	E	Chip Lifted
C	RAM	143	7744	Storage	325	4000	6,12	E	Chip Lifted
C	RAM	144	7744	Storage	325	4000	6,12	E	Chip Lifted
C	RAM	145	7744	Storage	325	4000	6,12	E	Chip Lifted
D	RAM	151	7626	Storage	325	4000	14	I	Not Confirmed
A	54LS283	145	7732	Storage	325	2000	1,2,3,5,6, 7,14,15	A,B,C	Chip Lifted
A	54LS283	149	7732	Storage	325	250	1,3,5,6, 7,13	A,B,C, D	Chip Lifted

TABLE 20: LISTING OF LOW POWER SCHOTTKY TTL REJECTS

(continued)

Vendor	Device Type	Unit No.	Date Code	Life Test	$T_A$ ( $^{\circ}$ C)	Hours to Failure Failed	Pin No. (s) Failed	Failure Mode	Failure Mechanism
A	54LS283	150	7732	Storage	325	4000	1,4,7,9,10, 13,14,15,16	C,D,F, J	Chip Lifted
B	54LS283	140	7741	Storage	325	4000	All inout, 16	C,F,I, J	Chip Lifted
B	54LS283	142	7741	Storage	325	4000	4,16	A, F	Chip Lifted
B	54LS283	148	7741	Storage	325	4000	All inout	C,I,J	Chip Lifted

\*Device left on life test for entire 3000 hours, after which time electromigration was seen.

Table 21: Key to Failure Modes and Mechanisms

<u>Failure Modes</u>			
A	$V_{OH}$	G	$V_{IC}$
B	$V_{OL}$	H	$I_{ZL}$
C	$I_{IL}$	I	$I_{IH}$
D	$I_{OS}$	J	$B_{IIH}$
E	Propagation Delays or Access Times	K	Functional Contact
F	$I_{CC}$	L	

Failure Mechanisms

EM - Electromigration

C - Contamination

#### D. Discussion

The study revealed that electrical failures resulting from electromigration were restricted to those devices reported in a latched mode during the accelerated life test.

Some evidence of minor hillock formation also was noticed on one of vendor A's 54LS251 (S/N 3). This device showed excess current during life test. A second device S/N 2 which never was in a high current condition showed no evidence of electromigration.

One each of the following devices which passed life test at +250°C for 3000 hours was examined, and no evidence of electromigration was found:

Vendor B 54LS251, S/N 10; Vendor A 54LS181, S/N 27;  
Vendor B 54LS181, S/N 16; and Vendor B 54LS191, S/N 15.

Two of vendor A's 54LS191's were opened after life test at 250°C for 3000 hours. In both of these units evidence of electromigration in the form of minor hillock formation was found, despite the fact that these units had never drawn excessive current.

During the performance of the life test individual  $I_{CC}$  currents for each device were recorded at the start and the completion of every life test period. Similarly device outputs were checked for proper operation for those device types not considered latched both at the beginning and end of each life test period up to an accumulated time of 32 hours. Thereafter proper output operation only was verified at the beginning of each period.

Chip separation was restricted to those devices in the +325°C storage environment having gold-silicon eutectic without nickel-molybdenum underplate. None of the examined units from exposure to 4000 hours at +300°C which included samples of all four vendors, even after additional thermal shock were found with chip/package separation. RAM's from both vendors subjected to storage step stress at 275°C, 300°C, 325°C for 72 hours each did not display this failure mechanism.

## VII. FINAL RESULTS

### A. Failure Rates

During the long term operational life test, no failures were recorded for the 54LS181, 54LS191, and 54LS251 from vendors A and B, with one exception; 54LS181 from vendor A identified at 8 hours. This unit was catagorized as early life failure and therefore excluded from the main population.

In order to calculate failure rates, the following assumptions were made; one single failure at the end of 3000 hours for the highest temperature environment; a distribution  $\sigma = 1.0$  and an activation energy  $E_a = 1.0\text{eV}$ .

The resulting instantaneous failure rate at  $10^5$  hours at maximum operating ambient temperature in application of  $+125^\circ\text{C}$  was calculated to be less than .001 failures per  $10^6$  hours.

With identical assumptions and one device failure at the end of the  $300^\circ\text{C}$  high temperature storage environment, failure rates of less than .001 failure per  $10^6$  hours were calculated for a maximum storage temperature of  $150^\circ\text{C}$ .

### B. Schottky Diodes

Distributions of offset voltage and input clamp forward voltage at different current levels for many types were plotted to demonstrate possible differences in Schottky stabilities between vendor processes. The offset voltage measured as  $V_{OL}$  without external load and equating to  $V_{BE} - V_{FS}$  was used to access the voltage  $V_{FS}$  stability of the Schottky diode used in the Baker clamp configuration. Should the forward voltage of this diode increase,  $V_{OL}$  would decrease and the output transistor therefore be forced deeper into saturation. As the device is forced deeper into saturation, storage time increases and the overall device propagation delay increases. Each graph of offset voltage or input clamp forward voltage compares initial versus final normalized parameter distribution from devices included in the operational life test. For those types which failed end point or final test resulting in severe electromigration damage, the generation of parameter distributions was limited to the forward voltage  $V_F$  of the input clamp diodes. Additionally, selected graphs of  $V_F$  of a particular input diode or offset voltage of a specific output was plotted versus time together with the identical parameter of a control device. The control devices referred to in the graph of Appendix N are identified with five digit serial numbers and have not undergone any stress testing nor electrical testing other than at the temperature indicated on the respective graphs. The possible variations of the control unit are due to test equipment drifts and minimum resolutions. Table 22 identifies the particular graphs generated for each device type.

Table 22: Initial/Final Parametric  
Distributions and Drift

Vendor	Type	Description of Graph	Appendix
A	54LS181	$\Delta V_F$ : All input clamp diodes, 18mA, 10 $\mu$ A, 1 $\mu$ A	N1-3
	"	$V_F$ /time: Input pin 1, 1 $\mu$ A	N4
B	54SL181	$\Delta V_F$ : All input clamp diodes, 18mA, 10 $\mu$ A, 1 $\mu$ A	N5-7
	"	$V_F$ /time: Input pin 1, 1 $\mu$ A	8
A	54LS191	$\Delta V_F$ : All input clamp diodes, 18mA, 10 $\mu$ A, 1 $\mu$ A	N9-11
	"	$\Delta V_{off}$ : All outputs	12
	"	$V_{off}$ /time: Output pin 2	13
B	54LS191	$\Delta V_F$ : All input clamp diodes, 18mA, 10 $\mu$ A, 1 $\mu$ A	N14-16
	"	$\Delta V_{off}$ : All outputs	17
	"	$V_{off}$ /time: Output pin 2	18
A	54LS251	$V_{off}$ /time: Output pin 5	19
B	54LS251	" " " "	20
A	54LS283	$\Delta V_F$ : All input clamp diodes, 18mA, 10 $\mu$ A,	N21-22
B	54LS283	$V_F$ : All input clamp diodes, 18mA, 10 $\mu$ A	N23-24
C	RAM	$V_F$ : All input clamp diodes, 18mA, 10 $\mu$ A, 1 $\mu$ A	N25-27
	"	$V_{off}$ : Output pin 6	26
	"	$V_{off}$ : Output pin 6	27

Table 22: (continued)

Vendor	Type	Description of Graph	Appendix
D	RAM	$\Delta V_F$ : All input clamp diodes, 18mA, 10 $\mu$ A, 1 $\mu$ A	N28-30
	"	$V_F$ /time: Input pin 2, 10 $\mu$ A	N31
	"	$V_F$ /time: Input pin 2, 1 $\mu$ A	N32

The data clearly demonstrates the stability of the platinum silicide Schottky process.

For vendor D employing aluminum for both ohmic and Schottky contacts distinct drifts of +30mV to +45mV in the forward voltage of the Schottky input diodes can be noticed.

### C. General Comments

Units of vendor B's 54LS191 earlier identified for non-performance during the  $F_{max}$  test (17 out of 30) at  $+125^{\circ}\text{C}$  are not considered a long term reliability problem.

The previously reported problem, that is the negative temperature coefficient for  $V_{OH}$  of vendor B's 54LS283 was totally masked by the severe deterioration of the devices due to electromigration so that its impact on reliability could not be assessed. The final measurements of access time for vendor D's RAM when compared to initial results increased by approximately 10%. These results were obtained as an average among six devices: three after completion of  $300^{\circ}\text{C}$  hot storage and three after completion of  $200^{\circ}\text{C}$  operational life test. Comparable units of vendor C's RAM, typically 2-2½ times faster by design, were basically stable and did not show a change in access time. This observed increase is possibly related to forward voltage drift of the aluminum Schottky diodes.

## VIII. OBSERVATIONS

The trimetal system consisting of titanium-tungsten as a barrier and aluminum as the main current carrying conductor is used by three of the four vendors. In these cases platinum-silicide is employed for ohmic contacts and Schottky barrier diodes. Results of the life test did not reveal any deterioration of the Schottky characteristics as evidenced in the stability of the input clamp diodes and offset voltage measurements. No penetration of aluminum or silicon through the barrier was noted indicating the effectiveness of the titanium-tungsten barrier.

Aluminum metallization without barrier metal and aluminum to semiconductor ohmic and Schottky contacts were employed by vendor D. The stability of these Schottky diodes as evidenced in the increase of forward voltage drop of the input clamps and also expressed in an increase of access time, is not as sound as the platinum-silicide equivalent.

The normalized current densities for the low power Schottky devices are well below the limit of  $5 \times 10^5$  A/cm<sup>2</sup> specified in MIL-M-38510 by one order of magnitude with the exception of vendor C's RAM with  $1.1 \times 10^5$  A/cm<sup>2</sup>.

C-MOS to low power Schottky interfacing is possible for all devices except the 54LS181 from both vendors.

The arithmetic logic units (54LS181) analyzed in this study from vendor A and vendor B make use of multi-emitter input structures.

Devices of vendor A's 54LS181 with date codes more recent than 7801 have been redesigned employing a diode input structure and now can also be driven by C-MOS devices.

In circuit application at maximum ambient temperature a large percentage (approximately 50%) of vendor B's 54LS191 will not perform at maximum frequency of 18MHz as specified. The value of approximately 50% is based on the test results of this study. Even when devices are fully tested to MIL-M-38510/315 this malfunction will not be screened out. A GIDEP report (GIDEP # K9-A-79-03) was issued.

A negative temperature coefficient for V<sub>OH</sub> above 25°C was discovered on all of vendor B's 54LS283 at output pin 4. Three percent of the devices failed to meet the minimum limit for V<sub>OH</sub> at +125°C. This phenomenon leads to a decreased noise immunity at higher temperatures. A GIDEP report (GIDEP # K9-A-79-04) was issued.

Severe random electromigration in the aluminum conductor runs was evidenced on all devices which were known to be in a latched condition during operational life test.

Instantaneous failure rates for the 54LS181, 54LS191, and 54LS251 from both vendors A and B which were not latched during operational life test, when calculated at 10<sup>5</sup> hours with previously discussed assumptions, was less than .001 failures per 10<sup>6</sup> hours. These figures are considerably better than the constant failure rates obtained from prediction methods in MIL-HDBK-217B.

## IX. RECOMMENDATIONS

An expansion of tests in MIL-M-38510/315 is recommended as a result of failures detected during the study. A large number of vendor B's 54LS191 failed to meet functional test at minimum clock pulse width at +125°C. The malfunction only affects the Q<sub>D</sub> output in either an "up" or "down" count mode. None of the tests in the present slash sheet will pick up this problem. The maximum frequency F<sub>max</sub> test only verifies operation of the Q<sub>A</sub> output. The recommended expansion of the F<sub>max</sub> test should include verification of Q<sub>B</sub>, Q<sub>C</sub>, and Q<sub>D</sub> at the specified clock frequency of 18MHz at room ambient and temperature extremes. Without this change devices could be accepted with a maximum frequency essentially limited to 12.5MHz when operated at +125°C.

If it is intended to perform burn-in at extremely accelerated conditions, then the burn-in configuration needs to be assessed in detail to achieve the highest possible temperature of operation without device latch up or significant increase in supply current I<sub>CC</sub>. A specific burn-in circuit proven for a particular type from one vendor may not necessarily prove to be the optimum for the same type from another vendor.

When devices are subjected to accelerated operational life test every device should be periodically checked for proper operation of the outputs and I<sub>CC</sub> verified.

It is also suggested to continue to include V<sub>CC</sub> line limiting resistors for all burn-in circuits in low power Schottky slash sheets to be released in the future.

References

1. D. S. Peck, "The Analysis of Data from Accelerated Stress Tests", B. T. L. Publications.
2. H. B. Huntington and A. R. Grone, J. Phys. Chem. Solids 20, 76 (1961)
3. J. R. Black, Proceedings of the 1967 Annual Symposium on Reliability Physics, 1967 (unpub.), Proc. IEEE 57, 1587 (1969).
4. D. S. Chhabra, N. G. Ainshie, and J. Jepsen, Electrochemical Soc. Meeting, Dallas, Texas, 1967 (unpub.).

APPENDIX A  
CONSTRUCTION ANALYSIS OF VENDOR A 54LS181  
STANDARD SCHOTTKY TTL INTEGRATED CIRCUIT IN CERAMIC DIP

Abstract

A Vendor A 4-bit arithmetic logic unit, 54LS181, was subjected to a detailed construction analysis. The circuit performs 16 binary arithmetic operations on two 4-bit words, incorporates full internal carry look ahead, and provides for either ripple carry between devices or for carry look ahead between packages. The device has a complexity of 75 equivalent gates, and low power Schottky technology is employed in the device fabrication.

Two devices were received packaged in standard 24 pin ceramic dual-in-line packages (CERDIP's) date coded 7710. The leads were tin plated Kovar; the internal wires were 1 mil aluminum, having better than adequate pull-strengths. The single level chip metallization was vapor deposited Al over sputtered Ti-W over  $Pt_xSi_y$  in the contact areas. The chip was entirely covered with vapor deposited PSG for scratch protection and passivation. One weakness in construction was noted. One wire bond did not align well with the bond pad, and the tail of the bond extended slightly over the Vcc metallization run, such that a weakness in the oxide layer there could result in a short.

Each input structure consisted of a Schottky diode to ground and an emitter-base junction of an npn Schottky transistor. This use of a transistor in place of the normally used second diode makes this device incompatible with CMOS devices. According to the vendor, a change in the input structure was made so that devices date coded 7801 and later do use the second diode.

No other weaknesses in construction or workmanship were noted.

Introduction

This analysis was performed as part of an evaluation of this device for Rome Air Development Center (RADC). The analysis was designed to document the construction details and materials used in these units and to identify shortcomings in the design or defects in workmanship, if any.

## Results

### The Package

The units were packaged in 24-lead ceramic dual-in-line packages (CERDIP). Both lid and base were of smooth alumina, with a fritted glass seal. The leads were embedded in the seal and consisted of tin plated Kovar. The thickness of the tin plating was measured to be  $8.8\mu\text{m}$  ( $350\mu\text{inches}$ ). The package dimensions were found to be within the limits specified in MIL-M-38510D and are shown in Figure 2; the case outline drawing and specification for dimensions are shown in Figure 1. The package markings were as shown in Figure 3.

The internal area of the lead frame which is used for bonding pads for the aluminum wires was clad with aluminum. This is rolled on prior to assembly of the package, and was measured to be  $3.8\mu\text{m}$  ( $152\mu\text{inches}$ ) thick.

### The Chip

The lid was removed by applying a mechanical stress to it and forcing a chisel edge into the seal in a controlled manner until the seal fractured. An overall view of the chip is shown in Figure 4. The chip was measured to be  $1.8 \times 2.2 \times 0.2 \text{ mm}$  ( $72 \times 88 \times 8.0 \text{ mils}$ ). The volume of the cavity was  $0.11 \text{ cm}^3$  including the recess in the package lid. The chip was mounted using a silicon-gold eutectic approximately  $10-20\mu\text{m}$  ( $0.39-0.79 \text{ mils}$ ) thick with a thick film gold paste providing the gold. This thick film gold paste also contains minute glass particles which are fired into the ceramic at  $920^\circ\text{C}$ , thus providing the adhesion to the ceramic substrate. Away from the chip the gold metallization which lined the bottom of the cavity was measured to be  $10-20\mu\text{m}$  ( $0.39-0.79 \text{ mils}$ ) thick. Thermal resistances were measured to be  $\theta_{\text{junction-to-air}} = 73.3 \text{ }^\circ\text{C/W}$  and  $\theta_{\text{junction-to-case}} = 13.6 \text{ }^\circ\text{C/W}$ .

The internal wires were ultrasonically bonded, 1 mil diameter aluminum. Microbond-pull testing of 9 of the 24 wires yielded a range in pull strength from 3.4 to 5.5 grams-force, with an average of 4.6. These wires exceed the minimum pull-strength of 2.0 gm-f specified in MIL-STD-883B, Method 2011.2. No bond defects were noted.

The chip metallization was a single level interconnection scheme which used aluminum  $1.5\mu\text{m}$  ( $59\mu\text{inches}$ ) thick over Ti-W approximately  $4,000 \text{ \AA}$  thick. The presence of the Ti-W layer provides good adhesion to the Si and  $\text{SiO}_2$  and is a diffusion barrier to the aluminum. The platinum-silicide in the contact areas gives good contact for base (P) and emitter (N+) diffusions and Schottky barrier contacts for

collectors (N). The above thicknesses were measured in an angle cross-section. The aluminum layer was vapor deposited and the Ti-W was sputter deposited in an undisclosed ratio. The  $Pt_xSi_y$  is formed in the contact areas, followed by blanket etching to remove the Pt elsewhere. A phosphosilicate glass layer about  $1.5\mu m$  ( $59\mu in$ ches) thick covered entire chip as passivation and protection against scratching during handling.

The highest current density was found to exist in the ground metallization run at Q86. Here the current is  $4.6mA$  maximum and the smallest metallization width is  $1.8 \times 10^{-3}cm$ . The metallization thickness of  $1.5 \times 10^{-4}cm$  results in a minimum cross-sectional area of  $2.7 \times 10^{-7}cm^2$ , which yields a maximum current density of  $1.7 \times 10^4 A/cm^2$ . Over an oxide step the current density could reach  $2.6 \times 10^4 A/cm^2$ , since the metallization thins to about 2/3 its thickness as it goes over an oxide step. This is within the specification of  $5 \times 10^5 A/cm^2$  found in MIL-M-38510 as a maximum current density for Al to avoid an unacceptable level of electromigration failures.

The chip was photographed and mapped to identify all the components. Figure 5 shows the logic layout of the device, and Figure 6 shows a detailed schematic of the device as related to the external pin connections and as it appears in the slash sheet, MIL-M-38510/308. Figure 7 shows the chip with all of the components labelled with the schematic symbol designations corresponding to those given in Figure 6. It was found that each input structure consisted of a Schottky diode to ground and an emitter-base junction of an npn Schottky transistor, this latter in place of the second diode shown in the circuit schematic in the slash sheet and in Figure 6. In some places multiple emitter transistors were used. In Figure 7, each such emitter is labelled  $D_{xy}$ , corresponding to  $Z_{xy}$  on Figure 6. An example of the circuit schematics for the input structure as shown in the slash sheet and as it was found to be on the chip is shown in Figure 8. Figure 9 shows a photomicrograph of the corresponding region of the chip. It should be noted that, according to the vendor, a change in the device construction was effective starting with devices date coded 7801, such that the schematic shown in the slash sheet became representative. Earlier devices, including those received for construction analysis, used a transistor input.

Visual inspection of the chip was performed using Method 2010.3 of MIL-STD-883B as a guide. The only workmanship weakness found consisted or poor alignment of one of the wire bonds (pin 22) to a chip pad. The tail of this bond extended slightly over the Vcc metallization run. If an oxide defect were present underneath the bond tail, a short could result between Vcc and pin 22 (an input). A photomicrograph of this bond is shown in Figure 10.

### The Components

The substrate was P-type. Subcollectors approximately  $7.9\mu\text{m}$  (0.31 mils) deep, consisting of low resistivity N-type diffusions, were made in positions corresponding to the transistors prior to the growth of the epitaxial layer. These provided high conductivity paths from the vicinity of the base-collector junctions to the collector contact diffusions. An N-type epitaxy about  $3.2\mu\text{m}$  (0.13 mils) thick was then grown.

After the growth of the epitaxial layer, P-type isolation diffusions approximately  $3.8\mu\text{m}$  (0.15 mils) deep were made, partitioning the epitaxial layer into individual collector regions and other components. The P-type base diffusion followed and the resistors were also made at this time. This diffusion was measured to be about  $1.8\mu\text{m}$  ( $71\mu\text{inches}$ ) deep. This also created the p-n junction guard rings for the input clamping diode to be discussed later. The N+ type diffusion, measured to be about  $1.1\mu\text{m}$  ( $3.3\mu\text{inches}$ ) deep, then created the emitters and the collector contact enhancement regions. This latter was necessary to achieve ohmic contact to the low-doped epitaxial layer.

### The Transistors

All but thirty-one of the transistors utilized the Schottky design. The base regions of these Schottky transistors were annular, having a rectangular "hole" within a rectangular shaped diffusion. Hence a portion of the epitaxial region at the surface was surrounded by this annular ring. The contact hole in the base oxide exposed both part of the base region and all of the epitaxial region which was surrounded by the base ring. This latter was part of the collector. When the metallization was deposited within the contact hole, it created the ohmic contact to the base region and also created the Schottky diode between base and collector. This occurred because of the relative doping level of the base region (high doping yields ohmic contact) versus that of the epitaxial (collector) region (low doping yields rectifying Schottky contact). The 31 transistors mentioned above as exceptions from this design were of standard bipolar construction.

### The Diodes

Each input had a Schottky barrier diode to ground to provide protection for the input against negative voltage spikes. The construction was quite similar to that in the transistor, forming what was actually a p-n junction - Schottky barrier hybrid diode. A cross-sectional diagram (not to scale) of the construction of the input structure is shown in Figure 11. References 1 and 2 describe the theory and advantages of such a structure.

### The Resistors

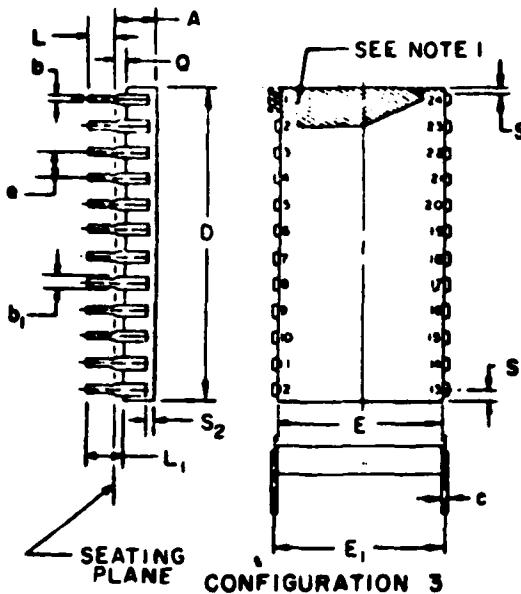
P-type base diffusion was used for all of the resistors. This diffusion had a resistivity of about  $1,000\Omega/\square$ . This sheet resistance was obtained by counting squares and comparing to values shown in the electrical schematic in Figure 6. The diffusion depth was measured to be about  $1.8\mu\text{m}$  ( $71\mu\text{inches}$ ).

### Conclusions and Recommendations

In performing a construction analysis of Vendor A's 54LS181, one potential reliability hazard was identified. One of the wire bonds was poorly aligned to the bond pad on the chip. It is recommended that the vendor's pre-cap visual inspection procedures be reviewed. Other than this defect, no weaknesses in construction or workmanship were noted.

### References

1. RADC-TR-76-292, Reliability Evaluation of Schottky Barrier Diode Microcircuits, Raytheon Company, Sept. 1976, Appendix B, P. 158.
2. R.A. Zettler and A.M. Cowley, "p-n Junction-Schottky Barrier Hybrid Diode" IEEE Transactions on E.D., Vol. ED-16, No. 1, January 1969.



SEATING PLANE CONFIGURATION 3

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		.221		.572	
b	.014	.023	.16	.58	1
b <sub>1</sub>	.030	.070	.76	1.98	2
c	.008	.015	.20	.38	3
D		1.290		32.77	4
E	.500	.710	12.73	15.49	4
F <sub>1</sub>	.500	.620	14.00	15.75	7
E <sub>2</sub>	.270		.680		
E <sub>3</sub>	.050		.127		
f	100	RSC	2.54 RSC	5.9	
L	.120	.200	.305	.508	
L <sub>1</sub>	.100		.381		
Q	.015	.075	.38	1.91	3
Q <sub>1</sub>	.020		.51		
S		.098		.240	6
S <sub>1</sub>	.005		.13		6
S <sub>2</sub>	.005		.13		
w	0°	15°	0°	15°	

NOTES:

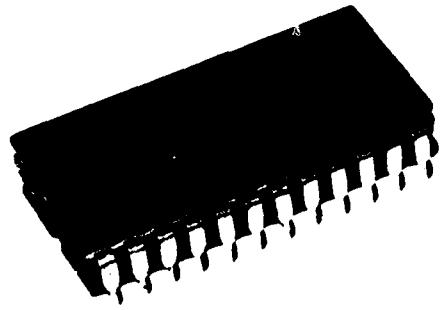
- Index area; a notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
- The minimum limit for dimension b<sub>1</sub> may be .020 (.51 mm) for leads number 1, 12, 13 and 24 only.
- Dimension Q shall be measured from the seating plane to the base plane.
- This dimension allows for off-center lid, meniscus and glass overrun.
- The basic pin spacing is .100 (2.54 mm) between centerlines. Each pin centerline shall be located within ±.010 (.25 mm) of its exact longitudinal position relative to pins 1 and 24.
- Applies to all four corners (leads number 1, 12, 13, and 24), and 40.5 shall apply.
- Lead center when a is 0. E<sub>1</sub> shall be measured at the centerline of the leads (see 40.4 of this appendix).
- All leads - Increase maximum limit by .003 (.08 mm) measured at the center of the flat, when lead finish A is applied.
- Twenty-two spaces.
- If this configuration is used, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.

Figure 1. Package outline and dimensions specified for 24-lead ceramic dual-in-line package (CERDIP).

Figure 2. Package Dimensions

<u>Designation</u>	<u>Measured Value</u>
A	3.7 (.148)
b	0.45 (.018)
b <sub>1</sub>	1.25 (.050)
c	0.25 (.010)
D	30.8 (1.230)
E	12.8 (.510)
E <sub>1</sub>	14.5 (.580)
E <sub>2</sub>	--
E <sub>3</sub>	--
e	2.5 (.100)
L	3.38 (.135)
L <sub>1</sub>	4.5 (.180)
Q	1.0 (.040)
Q <sub>1</sub>	--
S	1.8 (.070)
S <sub>1</sub>	1.0 (.040)
S <sub>2</sub>	1.38 (.055)

Note: Values outside parentheses are in millimeters.  
Values within parentheses are in inches.



**Figure 3. External view showing package markings of device as received. Magnification: 1.7X.**

THIS PAGE IS BEST QUALITY PRACTICABLE  
FROM COPY FROM SOURCE TO DDC

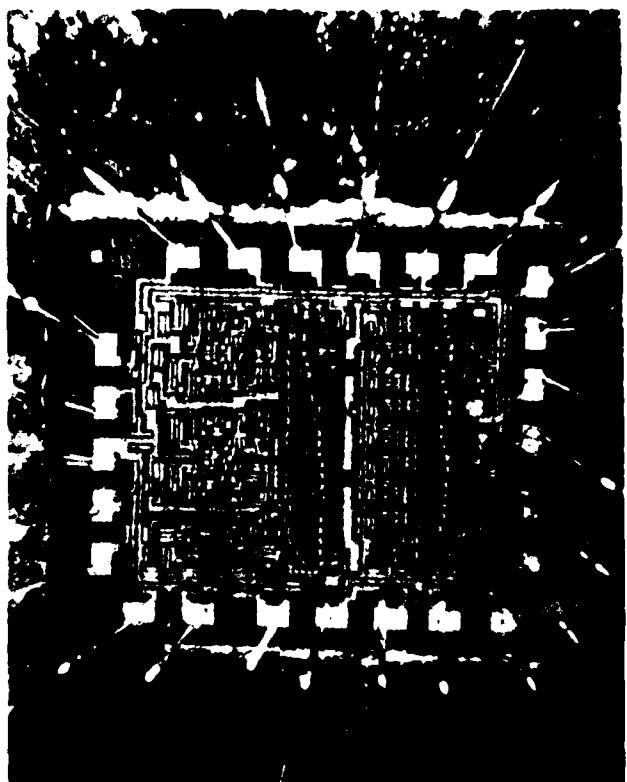


Figure 4. Interior view showing layout of chip.  
Magnification: 33X.

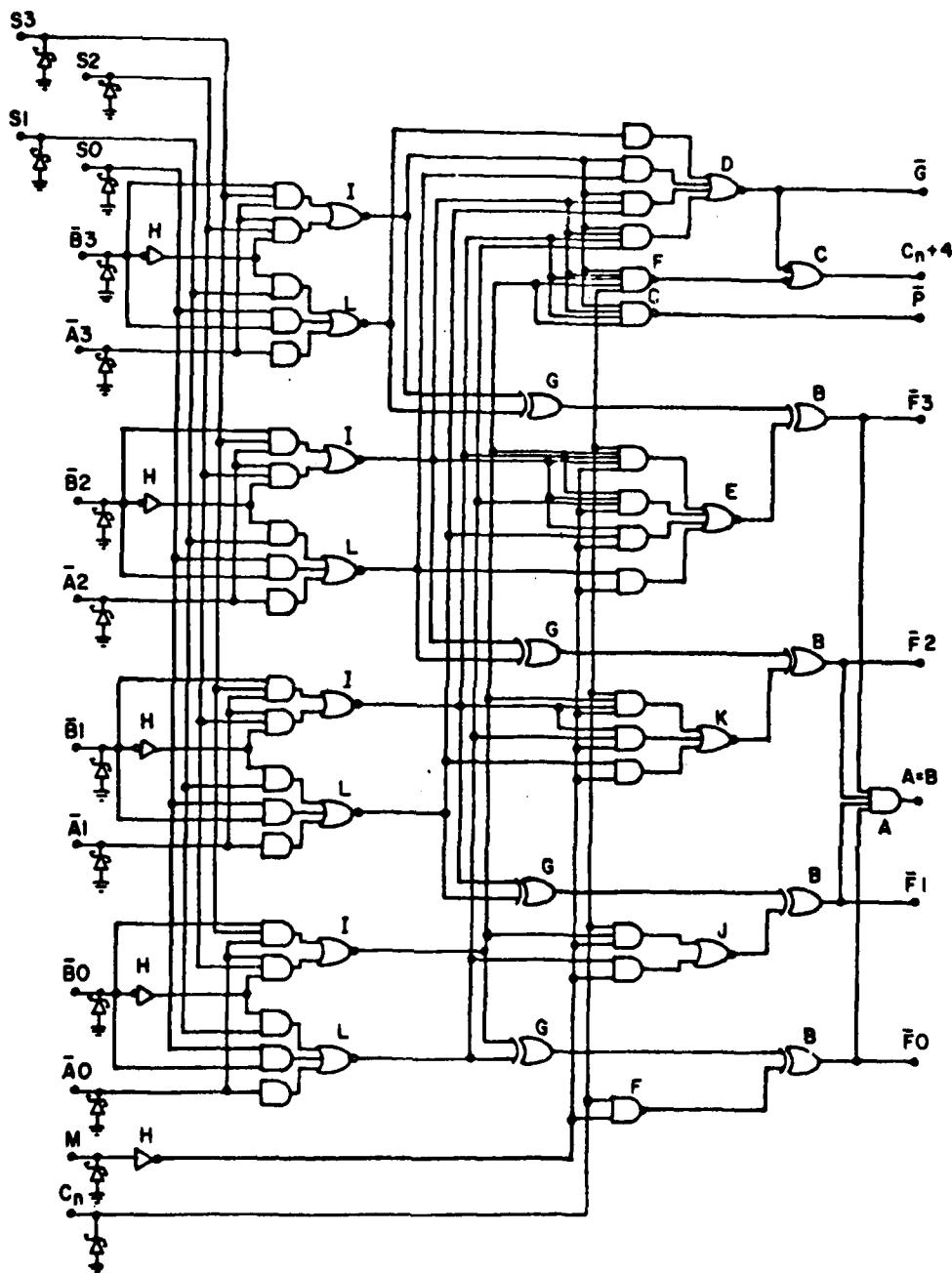


Figure 5. Logic diagram for the device.

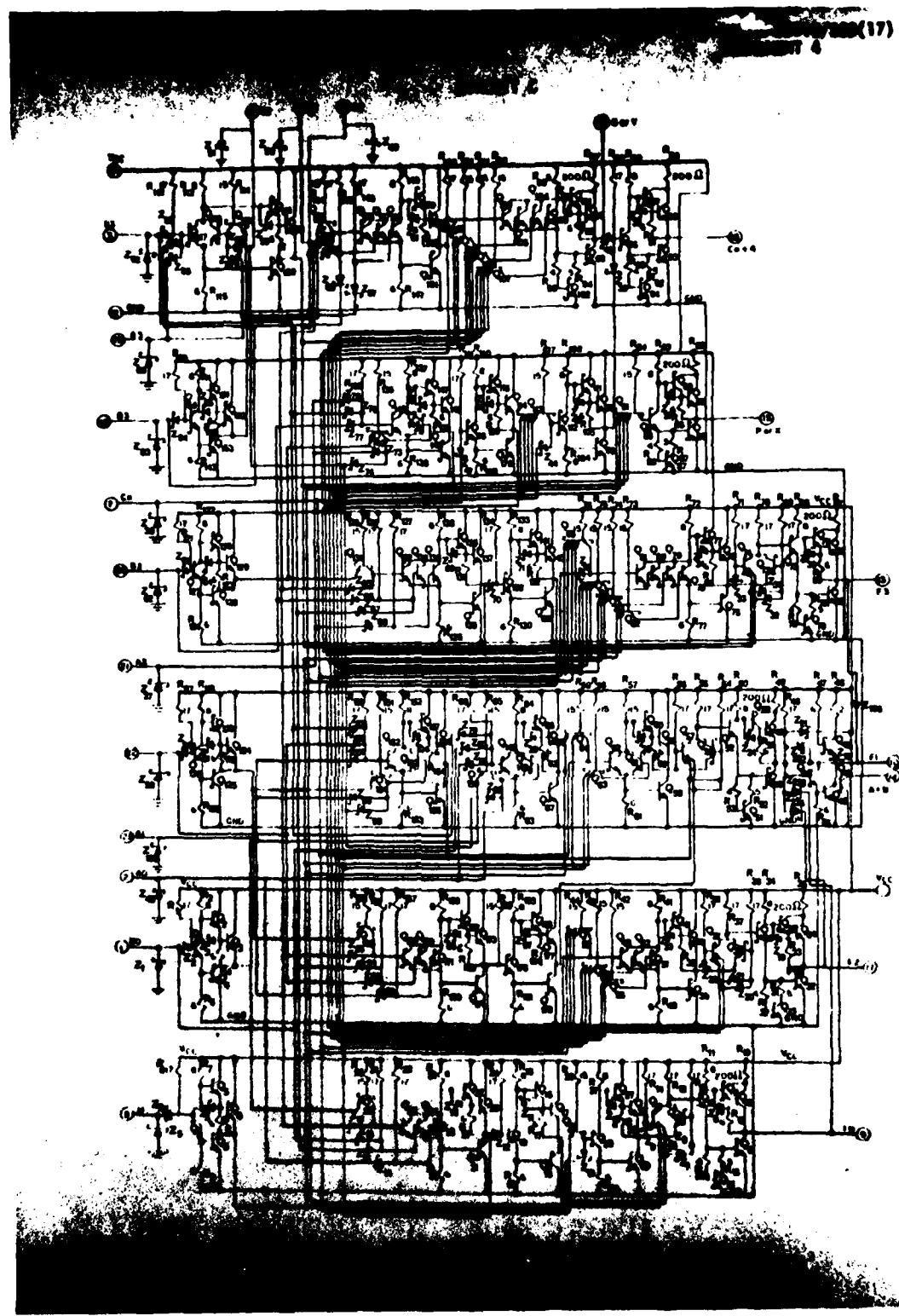


Figure 6. Detailed schematic of the device showing external pin connections.

A-11

THIS PAGE IS BEST QUALITY PRACTICABLE  
FROM COPY FURNISHED TO DDC

THIS PAGE IS BEST QUALITY PRACTICABLE  
FROM COPY MADE DIRECT TO DDC

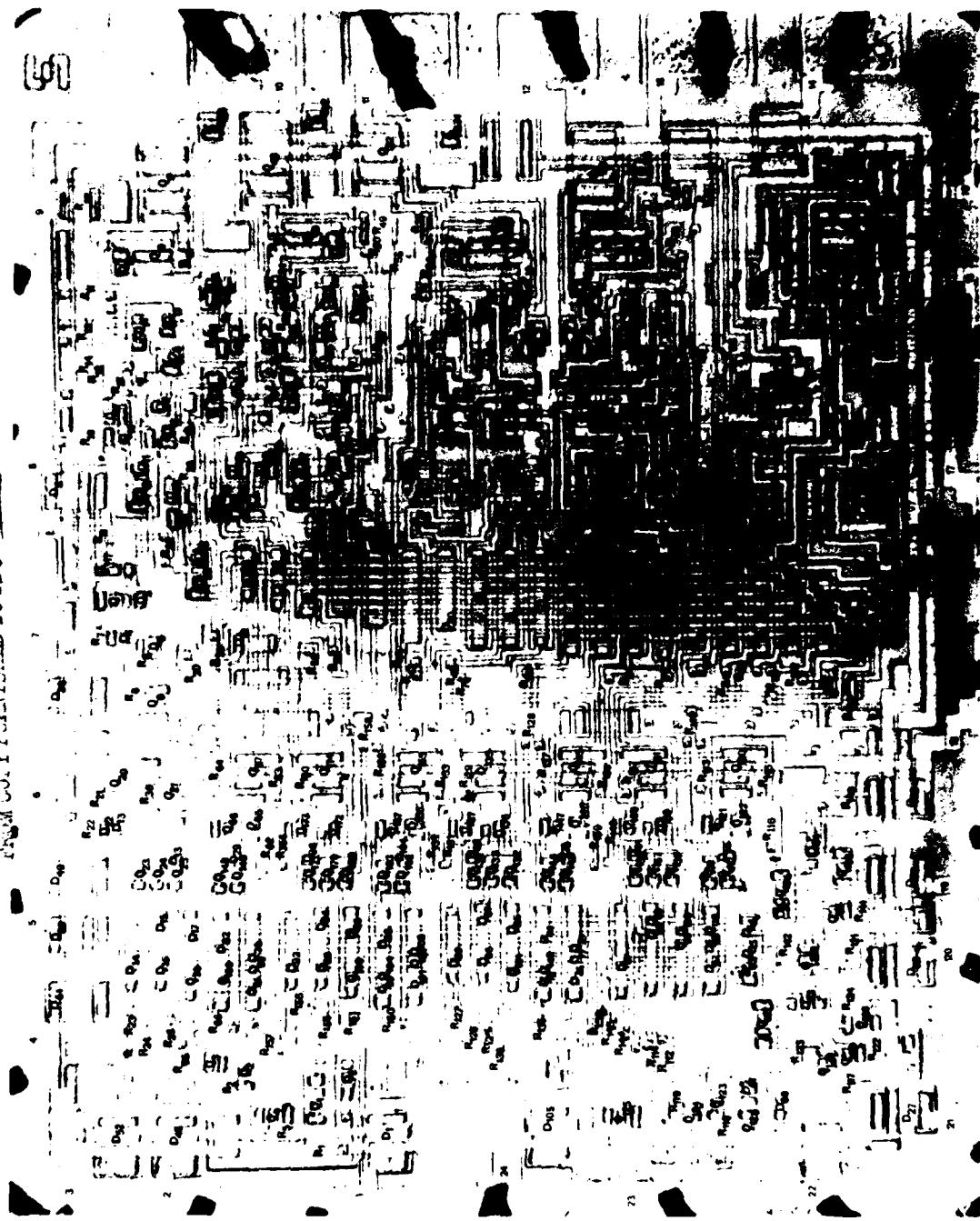


Figure 7. Detailed map of chip with device component designations corresponding to those in Figure 6. Note that the D's indicate emitter-base junctions of single or multiple emitter transistors used in input structures. (D<sub>xy</sub> corresponds to Z<sub>xy</sub> in Figure 6). Magnification: ~100X. (reversed image).

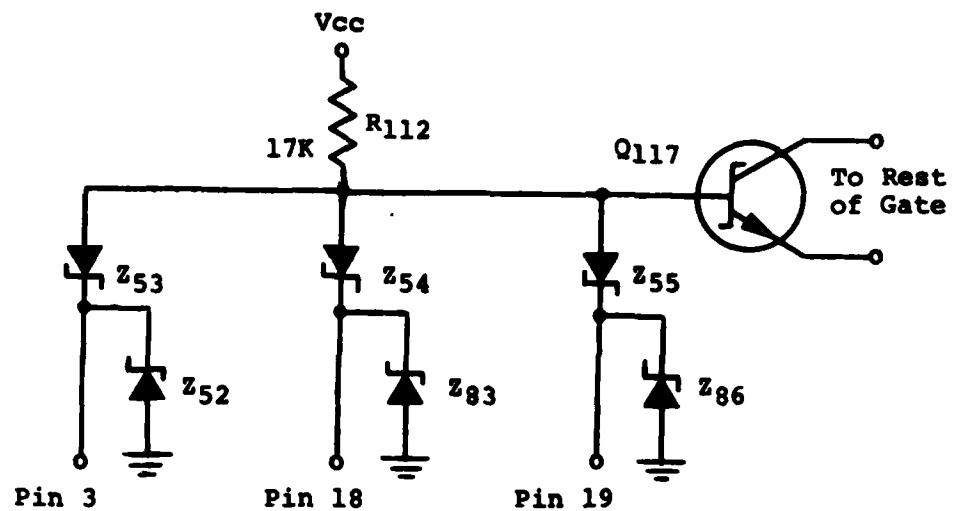


Figure 8a. Input structure as shown in slash sheet for input pins 3, 18, and 19.

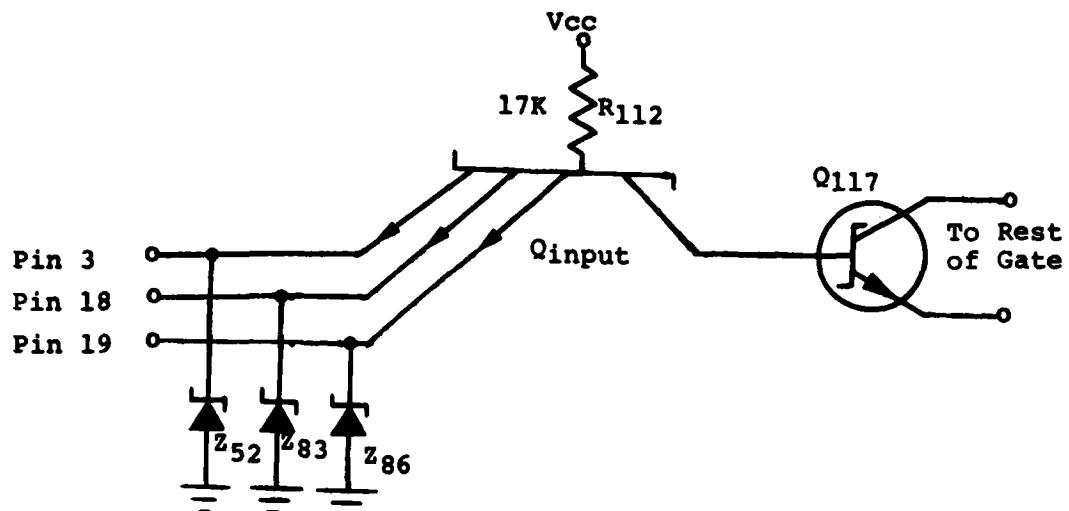
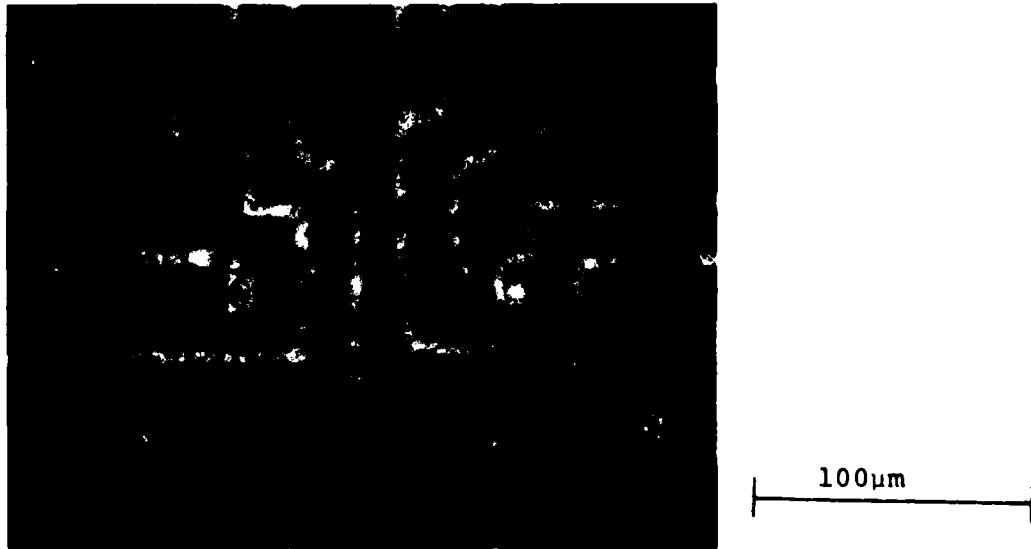


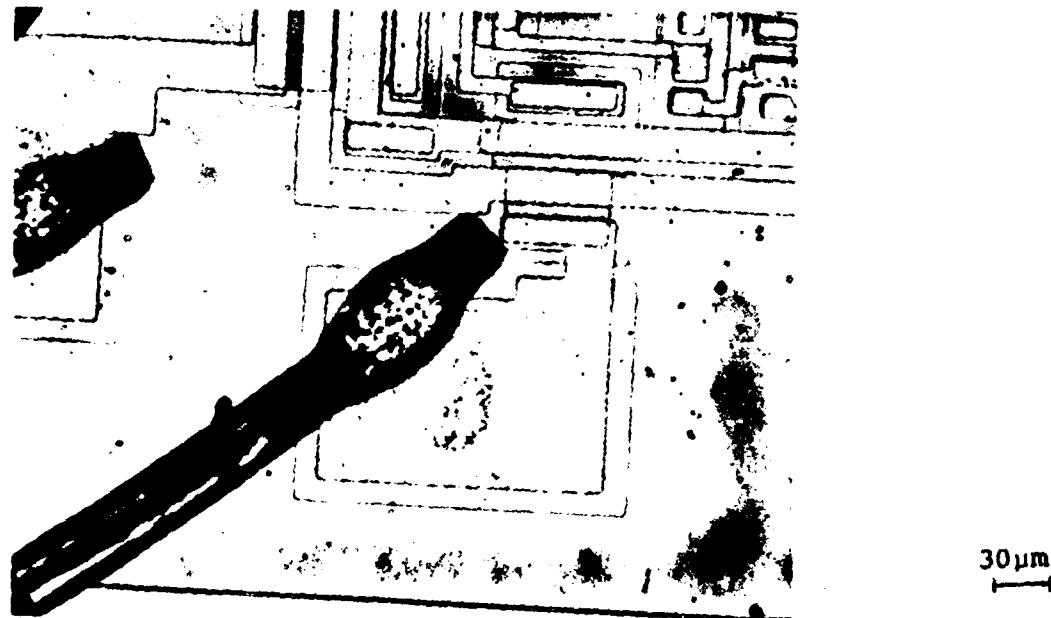
Figure 8b. Actual input structure using multiple emitters.

THIS PAGE IS SOIL QUALITY PRACTICABLE  
FROM COPY SOURCE



**Figure 9.** Photomicrograph showing input structure corresponding to that shown in Figure 8. C is the collector contact of the input transistor; B is the base contact; and  $\bar{D}_{xy}$  is the emitter contact corresponding to  $Z_{xy}$  in Figure 8a. Each such "diode" is actually an emitter-base junction.

THIS PAGE IS BEST QUALITY PRACTICABLE  
FROM COPY RECEIVED 10/20



**Figure 10.** Photomicrograph showing poor alignment of wire bond from device pin 22 at chip pad.

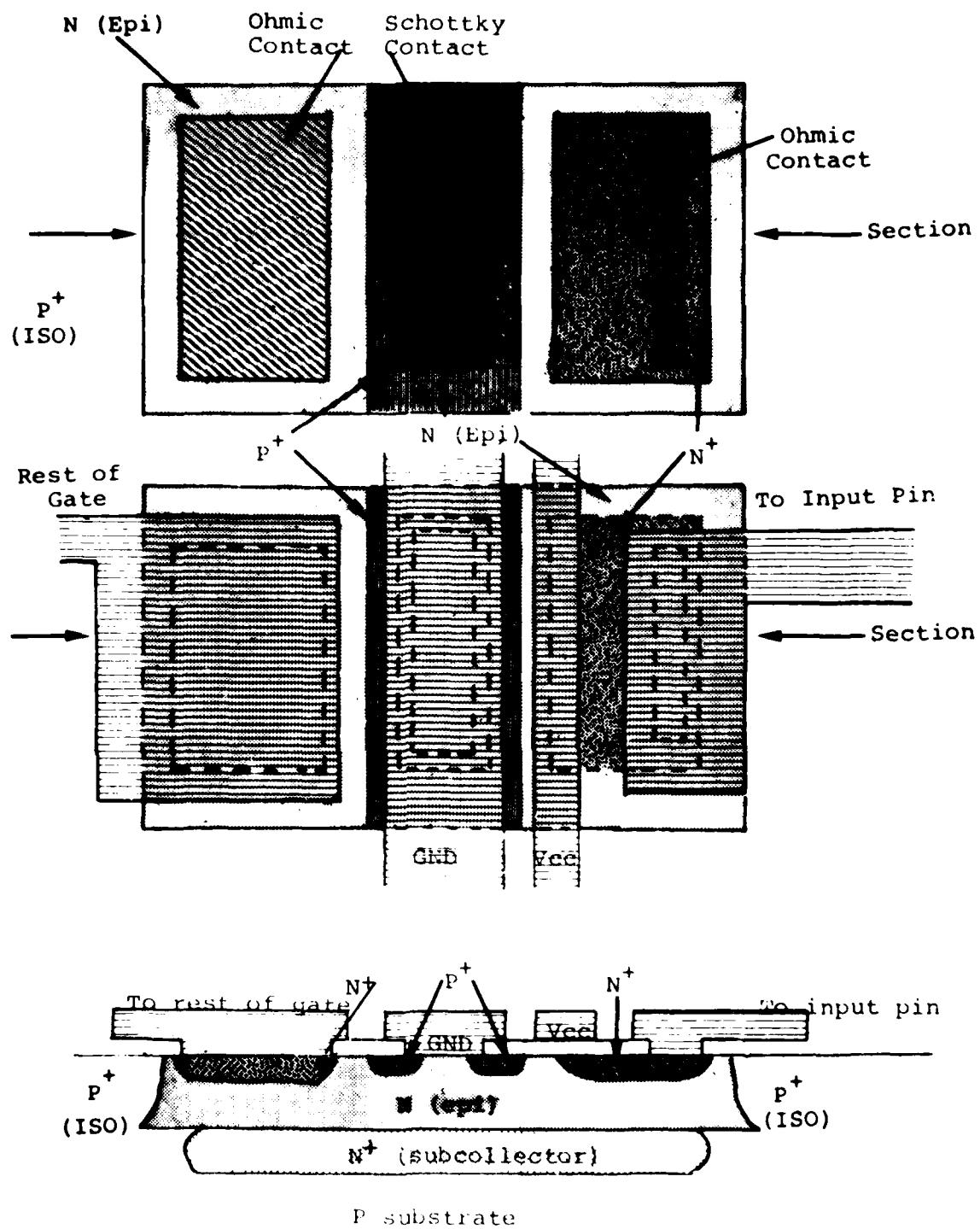


Figure 11. Schematic diagram showing cross-sectional view of input structure (not to scale).

APPENDIX B  
CONSTRUCTION ANALYSIS OF VENDOR B 54LS181  
STANDARD SCHOTTKY TTL INTEGRATED CIRCUIT IN CERAMIC DIP

Abstract

A Vendor B 4-bit arithmetic logic unit, 54LS181, was subjected to a detailed construction analysis. The circuit performs 16 binary arithmetic operations on two 4-bit words, incorporates full internal carry look ahead, and provides for either ripple carry between devices or for carry look ahead between packages. The device has a complexity of 75 equivalent gates, and low power Schottky technology is employed in the device fabrication.

Two devices were received packaged in standard 24 pin ceramic dual-in-line packages (CERDIP's) date coded 7614 and 7630. The leads were tin plated Kovar; the internal wires were 1 mil aluminum, having better than adequate pull-strengths. The single level chip metallization was vapor deposited Al over sputtered Ti-W over Pt<sub>x</sub>Si<sub>y</sub> in the contact areas. The chip was entirely covered with vapor deposited PSG for scratch protection and passivation. An oxide defect was seen near the ground metallization run, and a similar breakdown of the oxide elsewhere could result in a short.

Each input structure consisted of a Schottky diode to ground and an emitter-base junction of an npn Schottky transistor. This use of a transistor in place of the normally used second diode makes this device incompatible with CMOS devices.

No other weaknesses in construction or workmanship were noted.

## Introduction

This analysis was performed as part of an evaluation of this device for Rome Air Development Center (RADC). The analysis was designed to document the construction details and materials used in these units and to identify shortcomings in the design or defects in workmanship, if any.

## Results

### The Package

The units were packaged in 24-lead ceramic dual-in-line packages (CERDIP). Both lid and base were of smooth alumina, with a fritted glass seal. The leads were embedded in the seal and consisted of tin plated Kovar. The thickness of the tin plating was measured to be  $5.1\mu\text{m}$  ( $200\mu\text{inches}$ ). The package dimensions were found to be within the limits specified in MIL-M-38510D and are shown in Figure 2; the case outline drawing and specification for dimensions are shown in Figure 1. The package markings were as shown in Figure 3.

The internal area of the lead frame which is used for bonding pads for the aluminum wires was clad with aluminum. This is rolled on prior to assembly of the package, and was measured to be  $4.0\mu\text{m}$  ( $157\mu\text{inches}$ ) thick.

### The Chip

The lid was removed by applying a mechanical stress to it and forcing a chisel edge into the seal in a controlled manner until the seal fractured. An overall view of the chip is shown in Figure 4. The chips in the two units were compared, and no masking differences between these units of different date codes were found. The chip was measured to be  $1.84 \times 2.14 \times 0.19\text{mm}$  ( $77.4 \times 84.3 \times 7.5$  mils). The volume of the cavity was  $0.11\text{ cm}^3$  including the recess in the package lid. The chip was mounted using a silicon-gold eutectic approximately  $10-20\mu\text{m}$  ( $0.39-0.79$  mils) thick with a thick film gold paste providing the gold. This thick film gold paste also contains minute glass particles which are fired into the ceramic  $920^\circ\text{C}$ , thus providing the adhesion to the ceramic substrate. Away from the chip the gold metallization which lined the bottom of the cavity was measured to be  $12-24\mu\text{m}$  ( $0.47-0.94$  mils) thick. Thermal resistances were measured to be  $\theta_{\text{junction-to-air}} = 61.0^\circ\text{C/W}$  and  $\theta_{\text{junction-to-case}} = 16.4^\circ\text{C/W}$ .

The internal wires were ultrasonically bonded, 1 mil diameter aluminum. Microbond-pull testing of 8 of the 24 wires yielded a range in pull strength from 2.5 to 3.5 grams-force, with an average of 2.9. These wires exceed the minimum pull-strength of 2.0 gm-f specified in MIL-STD-883B, Method 2011.2, but by such a small amount that only slight weakening of the wires could result in failures at high levels of acceleration. No bond defects were noted.

The chip metallization was a single level interconnection scheme which used aluminum  $2.4\mu\text{m}$  ( $94\mu\text{inches}$ ) thick over Ti-W approximately  $5,000\text{ \AA}$  thick. The presence of the Ti-W layer provides good adhesion to the Si and  $\text{SiO}_2$  and is a diffusion barrier to the aluminum. The platinum-silicide in the contact areas gives good contact for base (P) and emitter (N+) diffusions and Schottky barrier contacts for collectors (N). The above thicknesses were measured in an angle cross-section. The aluminum layer was vapor deposited and the Ti-W was sputter deposited in an undisclosed ratio. The  $\text{Pt}_x\text{Si}_y$  is formed in the contact areas, followed by blanket etching to remove the Pt elsewhere. A phosphosilicate glass layer about  $2.5\mu\text{m}$  ( $98\mu\text{inches}$ ) thick covered the entire chip as passivation and protection against scratching during handling.

The highest current density was found to exist in the ground metallization run at Q45. Here the current is  $4.8\text{mA}$  maximum and the smallest metallization width is  $2.0 \times 10^{-3}\text{ cm}$ . The metallization thickness of  $2.4 \times 10^{-4}\text{ cm}$  results in a minimum cross-sectional area of  $5 \times 10^{-7}\text{ cm}^2$  which yields a maximum current density of  $9.6 \times 10^3\text{ A/cm}^2$ . Over an oxide step the current density could reach  $1.4 \times 10^4\text{ A/cm}^2$ , since the metallization thins to about  $2/3$  its thickness as it goes over an oxide step. This is within the specification of  $5 \times 10^5\text{ A/cm}^2$  found in MIL-M-38510 as a maximum current density for Al to avoid an unacceptable level of electromigration failures.

The chip was photographed and mapped to identify all the components. Figure 5 shows the logic layout of the device, and Figure 6 shows a detailed schematic of the device as related to the external pin connections. Figure 7 shows the chip with all of the components labelled with the schematic symbol designations corresponding to those given in Figure 6.

Visual inspection of the chip was performed using Method 2010.3 of MIL-STD-883B as a guide. The only workmanship weakness

found consisted of an oxide defect near the ground metallization run. While its location was not such as to raise great concern, similar oxide weaknesses occurring elsewhere might cause shorting.

#### The Components

The substrate was P-type. Subcollectors approximately  $15.5\mu\text{m}$  (0.61 mils) deep, consisting of low resistivity N-type diffusions, were made in positions corresponding to the transistors prior to the growth of the epitaxial layer. These provided high conductivity paths from the vicinity of the base-collector junctions to the collector contact diffusions. An N-type epitaxy about  $3.8\mu\text{m}$  (0.15 mils) thick was then grown.

After the growth of the epitaxial layer, P-type isolation diffusions approximately  $4.1\mu\text{m}$  (0.16 mils) deep were made, partitioning the epitaxial layer into individual collector regions and other components. The P-type base diffusion followed and the resistors were also made at this time. This diffusion was measured to be about  $1.8\mu\text{m}$  ( $71\mu\text{inches}$ ) deep. This also created the p-n junction guard rings for the input clamping diode to be discussed later. The  $\text{N}^+$  type diffusion, measured to be about  $1.0\mu\text{m}$  ( $39\mu\text{inches}$ ) deep, then created the emitters and the collector contact enhancement regions. This latter was necessary to achieve ohmic contact to the low-doped epitaxial layer.

#### The Transistors

All but sixteen of the transistors utilized the Schottky design. The base regions of these Skottky transistors were annular, having a rectangular "hole" within a rectangular shaped diffusion. Hence a portion of the epitaxial region at the surface was surrounded by this annular ring. The contact hole in the base oxide exposed both part of the base region and all of the epitaxial region which was surrounded by the base ring. This latter was part of the collector. When the metallization was deposited within the contact hole, it created the ohmic contact to the base region and also created the Schottky diode between base and collector. This occurred because of the relative doping level of the base region (high doping yields ohmic contact) versus that of the epitaxial (collector) region (low doping yields rectifying Schottky contact). The 16 transistors mentioned above as exceptions from this design were of standard bipolar construction.

Schottky transistors are used in the input structures, with the base-emitter (p-n) junctions taking the place of what is usually a diode between the input pin and the rest of the gate. This makes the device incompatible with CMOS devices as a result of the lower breakdown voltage of the junction. A top view of an input transistor is shown in Figure 8.

#### The Diodes

Each input had a Schottky barrier diode to ground to provide protection for the input against voltage spikes. The construction was quite similar to that in the transistors, forming what was actually a p-n junction - Schottky barrier hybrid diode. A cross-sectional diagram (not to scale) of the construction of the input structure is shown in Figure 9 with a top view shown in Figure 10. Reference 1 and 2 describe the theory and advantages of such a structure.

#### The Resistors

P-type base diffusion was used for all of the resistors. This diffusion had a resistivity of about  $1,000\Omega/\square$ . This sheet resistance was obtained by counting squares and comparing to values shown in the electrical schematic in Figure 6. The diffusion depth was measured to be about  $1.8\mu\text{m}$  ( $71\ \mu\text{inches}$ ).

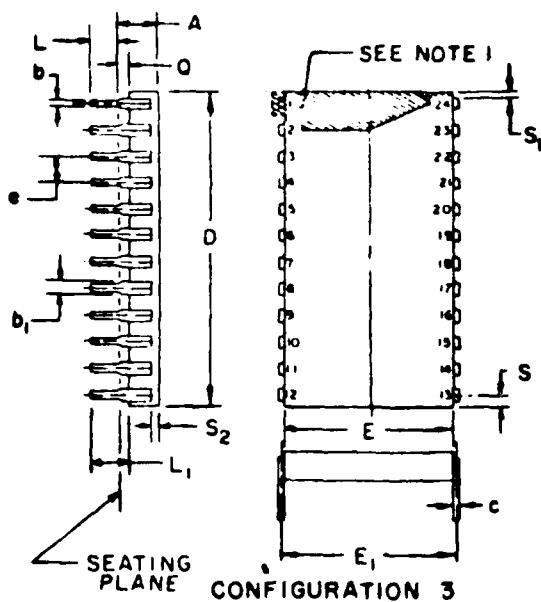
#### Conclusions and Recommendations

In performing a construction analysis of Vendor B's 54LS181, two potential reliability hazards were identified. An oxide defect was seen in the vicinity of the ground metallization run. Since similar oxide weaknesses occurring elsewhere could result in shorting, it is recommended that the Vendor's inspection procedures be reviewed. Also, wire bond pull testing revealed strengths only slightly better than the 2.0 gm-f minimum specified in MIL-STD-883B, Method 2011.2, for 1 mil aluminum wires. A review of the vendor's bonding procedures is recommended.

References

1. RADC-TR-292, Reliability Evaluation of Schottky Barrier Diode Microcircuits, Raytheon Company, Sept. 1976, Appendix B, P. 158.
2. R.A. Zettler and A.M. Cowley, "p-n Junction-Schottky Barrier Hybrid Diode" IEEE Transactions on E.D., Vol. ED-61, No. 1, January 1969.

THIS PAGE IS BEST QUALITY FRAGILE  
KODAK COPY FURNISHED TO DDC



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		.224		.572	
b	.011	.023	.28	.58	8
b <sub>1</sub>	.050	.070	.76	1.78	2, 8
c	.008	.015	.20	.38	8
D	1.290		32.77		4
E	.500	.610	12.70	15.49	4
E <sub>1</sub>	.590	.620	14.00	15.75	7
E <sub>2</sub>	.270		6.86		
E <sub>3</sub>	.050		1.27		
e	.100 RSC		2.54 LSC		5, 9
L	.120	.200	3.05	5.08	
L <sub>1</sub>	.170		3.81		
Q	.015	.075	.38	1.91	3
Q <sub>1</sub>	.020		.51		
S		.008		.249	8
S <sub>1</sub>	.005		.13		8
S <sub>2</sub>	.005		.13		
w	0°	15°	0°	15°	

NOTES:

- Index area; a notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
- The minimum limit for dimension b<sub>1</sub> may be .020 (.51 mm) for leads number 1, 12, 13 and 24 only.
- Dimension Q shall be measured from the seating plane to the base plane.
- This dimension allows for off-center lid, meniscus and glass overrun.
- The basic pin spacing is .100 (2.54 mm) between centerlines. Each pin centerline shall be located within ±.010 (.25 mm) of its exact longitudinal position relative to pins 1 and 24.
- Applies to all four corners (leads number 1, 12, 13, and 24), and 40.5 shall apply.
- Lead center when a is 0. E<sub>1</sub> shall be measured at the centerline of the leads (see 40.4 of this appendix).
- All leads - Increase maximum limit by .003 (.08 mm) measured at the center of the flat, when lead finish A is applied.
- Twenty-two spaces.
- If this configuration is used, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.

Figure 1: Package outline and dimensions specified for 24-lead ceramic dual-in-line package (CERDIP).

**Figure 2: Package Dimensions**

<u>Designation</u>	<u>Measured Value</u>	
A	5.5	(0.22)
b	0.5	(0.020)
b <sub>1</sub>	1.3	(0.051)
e	0.3	(0.012)
D	31.6	(1.24)
E	13.1	(0.516)
E <sub>1</sub>	15.0	(0.59)
E <sub>2</sub>	-	
E <sub>3</sub>	-	
e	2.5	(0.098)
L	3.2	(0.13)
L <sub>1</sub>	4.4	(0.17)
Q	1.8	(0.071)
Q <sub>1</sub>	0.8	(0.031)
S	1.5	(0.059)
S <sub>1</sub>	2.2	(0.087)
S <sub>2</sub>	0.8	(0.031)

**Note:** Values outside parentheses are in millimeters.  
Values within parentheses are in inches.



Figure 3: External view showing package markings of device as received. Magnification: 3x.

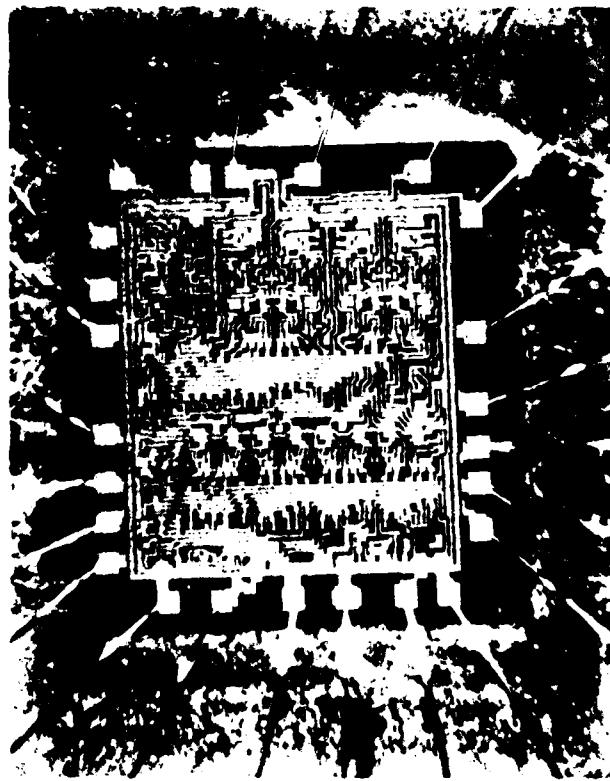
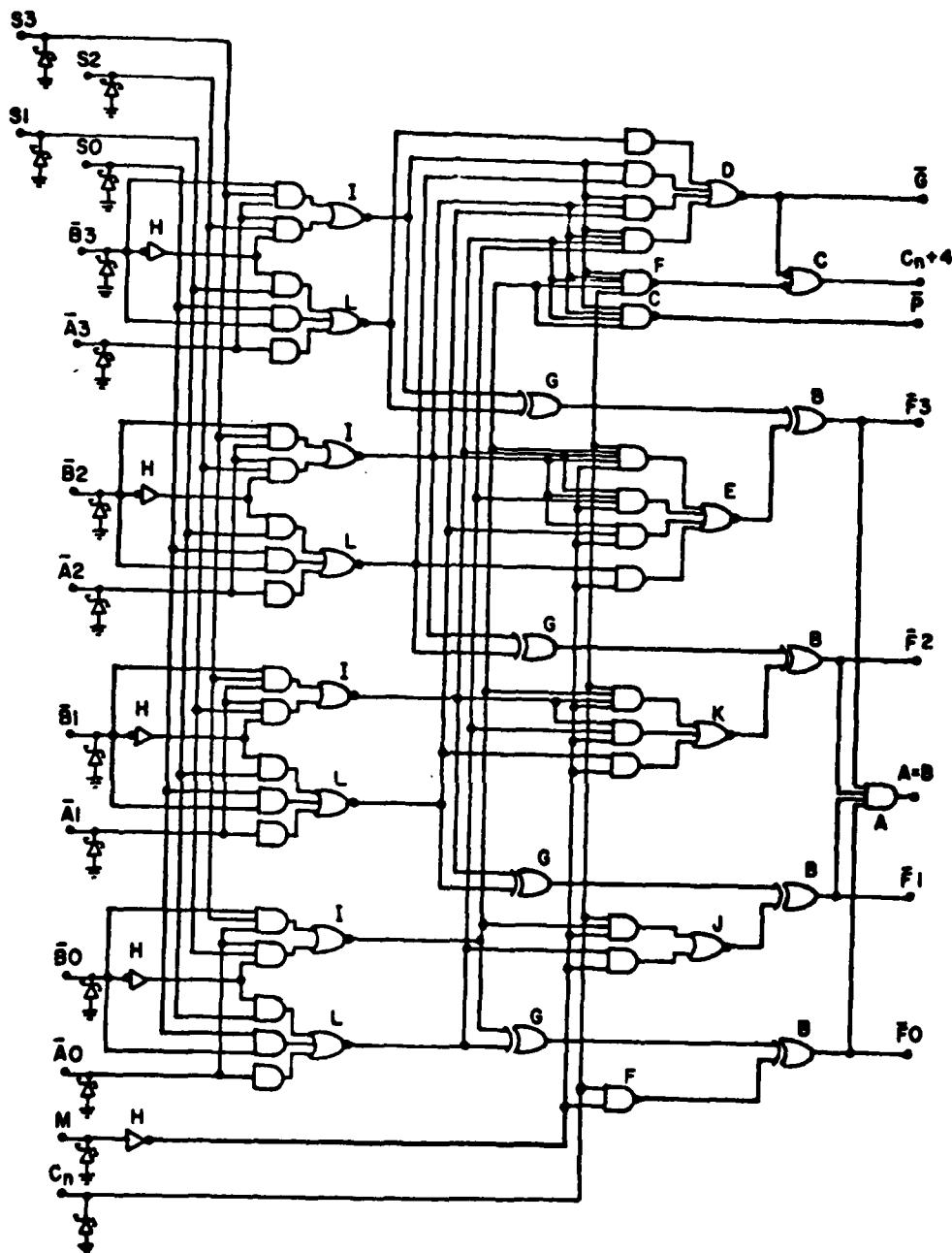
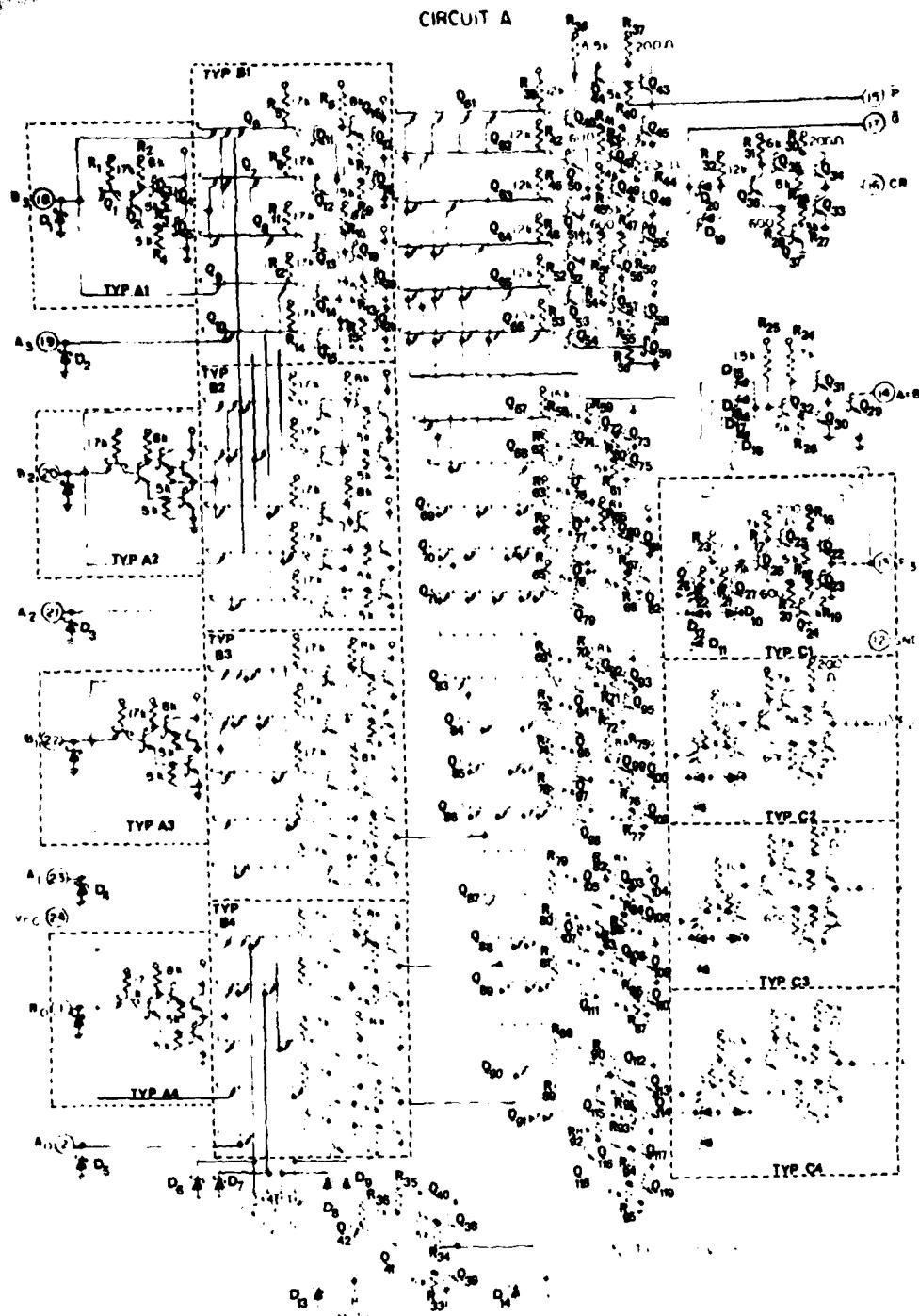


Figure 4: Interior view showing layout of chip. Mag.: 35X



**Figure 5:** Logic diagram for the device.



**FIGURE 3.** Logic diagram and schematic for device type 01 - Continued.

THIS PAGE IS BEST QUALITY PRACTICABLE  
FROM COPY FURNISHED TO DDC

**Figure 6:** Detailed schematic of the device showing external pin connections.

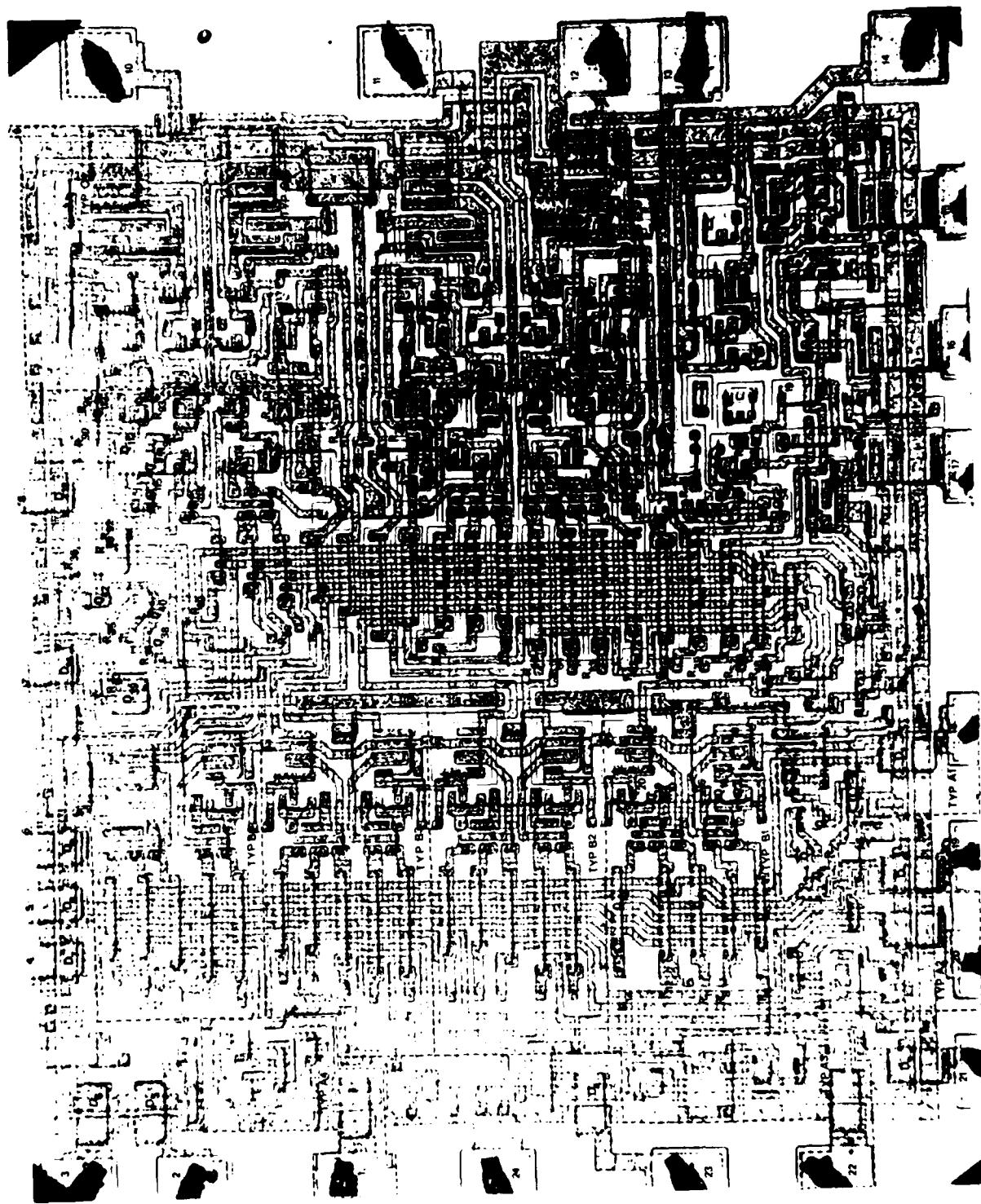


Figure 7: Detailed map of chip with device component designations corresponding to those in Figure 6.  
Magnification: ~100x. (Reversed image).

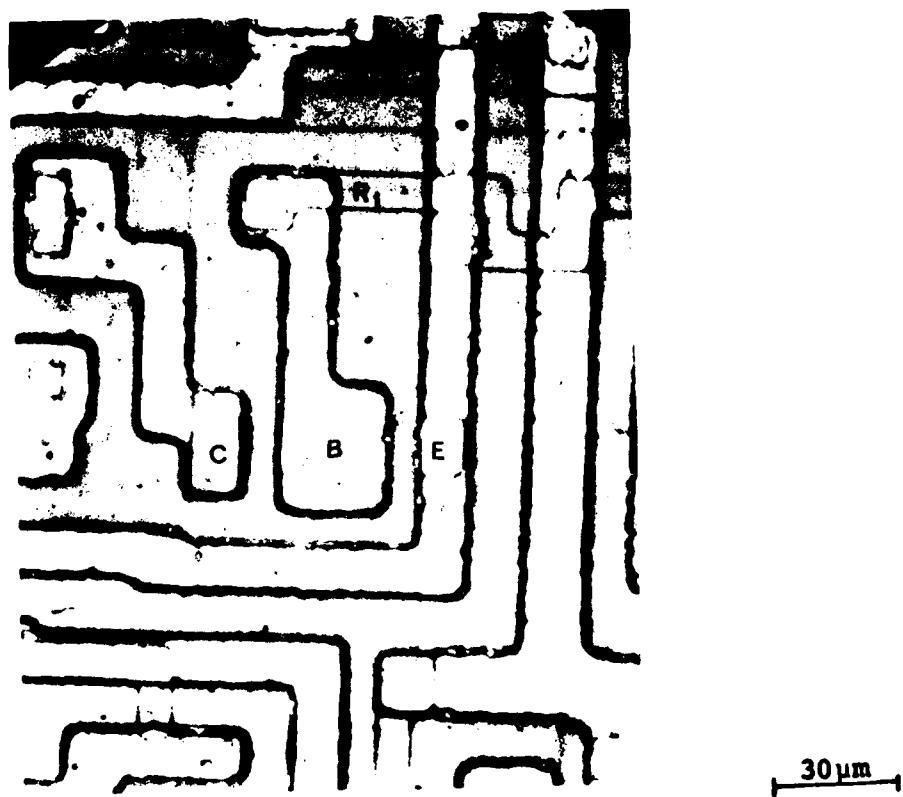


Figure 8: Photomicrograph showing top view of input transistor Q1.

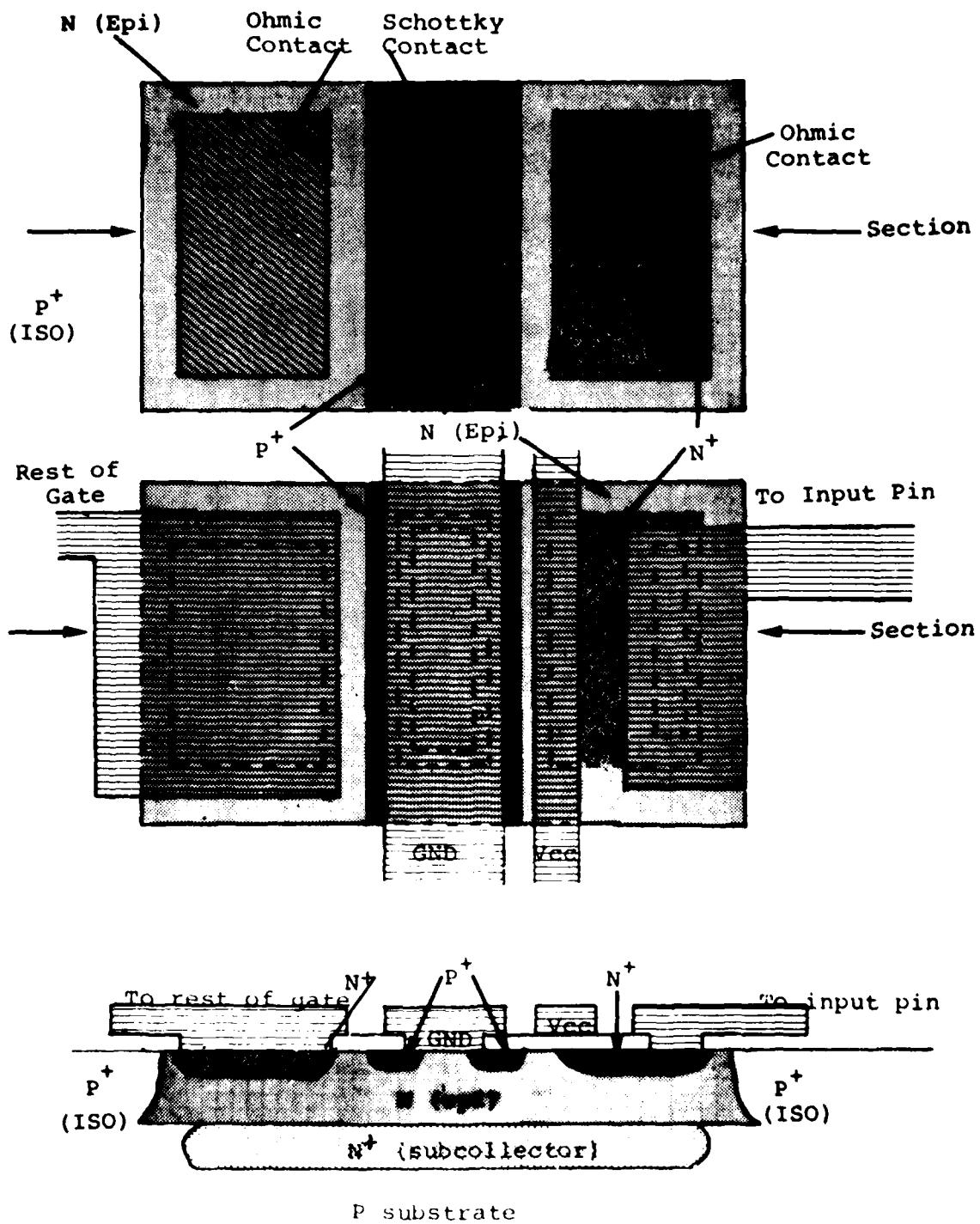


Figure 9: Schematic diagram showing cross-sectional view of input structure (not to scale).

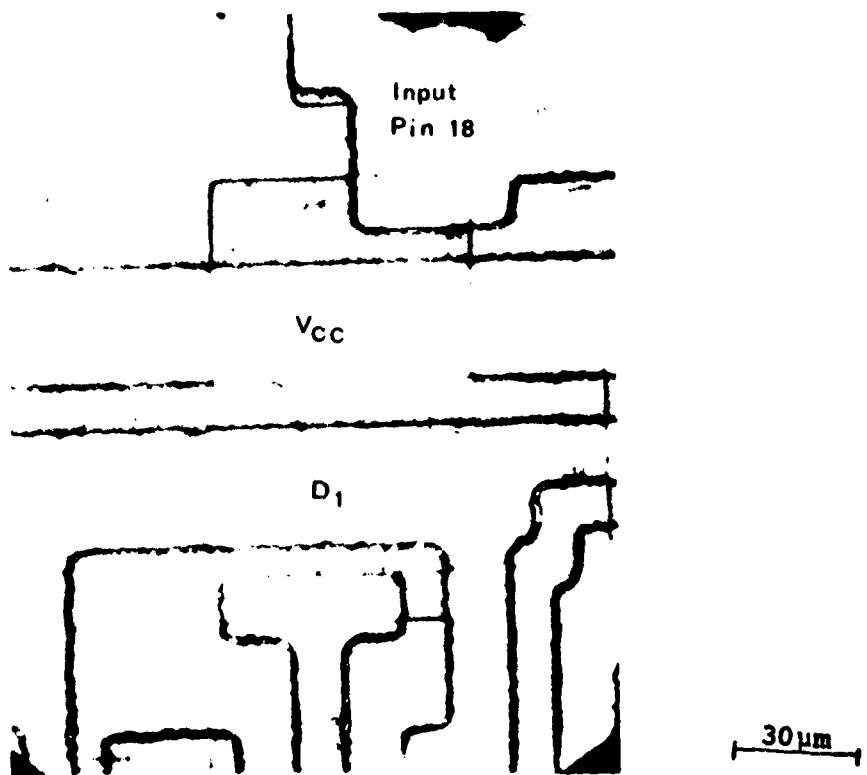


Figure 10: Photomicrograph showing top view of input structure.

APPENDIX C  
CONSTRUCTION ANALYSIS OF VENDOR A 54LS251  
STANDARD SCHOTTKY TTL INTEGRATED CIRCUIT IN CERAMIC DIP

ABSTRACT

A Vendor A high speed eight input digital multiplexer, incorporating full on-chip binary decoding to select one of eight data sources and featuring a strobe controlled tri-state output, was subjected to a detailed construction analysis. Two devices were received packaged in standard 16-pin ceramic dual-in-line packages (CERDIP's), and date coded 7811. They were low power Schottky devices. The internal wires were found to be 1 mil Al, while the single level chip metallization was as follows: vapor deposited Al over sputtered Ti-W over  $Pt_xSi_y$ . The chip is entirely coated with vapor deposited  $SiO_2$ . Some differences were noted between the schematic diagram included in the latest edition of MIL-M-38510/309A and the actual layout of the device. No weaknesses in construction or workmanship were noted.

INTRODUCTION

This analysis was performed as part of an evaluation of this device for Rome Air Development Center (RADC). The analysis was designed to document the construction details and materials used in these units and to identify shortcomings in the design or defects in workmanship, if any.

RESULTS

The Package

The units were packaged in 16-lead ceramic dual-in-line packages (CERDIP). Both lid and base were of smooth alumina, with a fritted glass seal. The leads were embedded in the seal

and consisted of tin plated Kovar. The thickness of the tin plating was measured to 6.25  $\mu\text{m}$  (250  $\mu\text{inches}$ ). Package dimensions were found to be within the limits specified in MIL-M-38510D and are shown in Figure 2; the case outline drawing and specifications for dimensions are shown in Figure 1. The package markings were as shown in Figure 3.

The leads consisted of a Kovar base with tin plating 6.25  $\mu\text{m}$  (250  $\mu\text{in.}$ ) thick. The area of the lead frame which made internal contacts to the aluminum wires was clad with aluminum. This is rolled on prior to assembly of the package, and was measured to be 3.5  $\mu\text{m}$  (140  $\mu\text{inches}$ ) thick.

#### The Chip

The lid was removed by applying a mechanical stress to it and forcing a chisel edge into the seal in a controlled manner until the seal fractured. An overall view of the cavity and chip is shown in Figure 4. The chip was measured to be 1.44 x 1.44 x 0.215 mm (57.6 x 57.6 x 8.6 mils). The volume of the cavity was 0.027  $\text{cm}^3$ , including the recess in the package lid. The chip was mounted using a silicon-gold eutectic from 16 to 24  $\mu\text{m}$  (.64 to .96 mils) thick, with a thick film gold paste providing the gold. This thick film gold paste also contains minute glass cylinders which are fired into the ceramic at 920°C, thus providing the adhesion to the ceramic substrate. Away from the chip the gold metallization which lined the bottom of the cavity was measured to be 7  $\mu\text{m}$  (.28 mils) thick and the presence of voids was noted. Thermal resistances were measured to be  $\theta_{\text{junction-to-air}} = 107.0^\circ\text{C/W}$  and  $\theta_{\text{junction-to-case}} = 15.9^\circ\text{C/W}$ .

The internal wires were ultrasonically bonded, 1 mil diameter aluminum. Microbond-pull testing of 5 of the 16 wires yielded a range in pull-strength from 3.5 to 5.5 grams-force, with an average of 4.5. These wires exceed the pull-strength of 2 gm-f specified in MIL-STD-883B.

The chip metallization was a single level interconnection scheme which used aluminum 1.3  $\mu\text{m}$  (52  $\mu\text{inches}$ ) thick over a Ti-W layer approximately 2600Å thick. The presence of the Ti-W layer provides good adhesion to the Si and  $\text{SiO}_2$  and is a diffusion barrier to the aluminum. The platinum-silicide in the contact areas gives good ohmic and Schottky barrier contact. The above thicknesses were measured in an angle cross-section. The aluminum layer was vapor deposited and the Ti-W was sputter deposited in an undisclosed ratio. The  $\text{Pt}_x\text{Si}_y$  is formed by sputtering on Pt in a very thin layer and sintering to form

$\text{Pt}_x\text{Si}_y$  in the contact areas, followed by blanket etching to remove the Pt elsewhere. A  $\text{SiO}_2$  layer about  $1.3 \mu\text{m}$  (52  $\mu\text{inches}$ ) thick covered the entire chip as passivation and protection against scratching during handling.

The highest current density was found to exist in the emitter metallization from the output transistor at outputs y and w (pins 5 and 6). Here the current is 4.6mA maximum and the metallization is  $9.2 \times 10^{-4} \text{ cm}$  wide by  $1.3 \times 10^{-4} \text{ cm}$  thick, resulting in a current density of  $3.85 \times 10^4 \text{ A/cm}^2$ . Over an oxide step the current density could reach  $5.8 \times 10^4 \text{ A/cm}^2$ , since the metallization thins to about 2/3 its thickness as it goes over an oxide step. This is within the MIL-M-38510 specification of  $5 \times 10^5 \text{ A/cm}^2$  as a maximum current density for Al to avoid an unacceptable level of electromigration.

The chip was photographed and mapped to identify all the components. Figure 5 shows the logic layout of the device as related to the external pin connections and Figure 6 shows a detailed schematic of the device. Figure 7 shows the chip with all of the components labelled with the schematic symbol designations corresponding to those given in Figure 6. In mapping the device, some discrepancies from the schematic diagram given in MIL-M-38150/309A were found. (Amendment 2, 31 May 1978, showed no change.) The transistor with base connection coming out of the "TYP h" box in the slash sheet is actually Q<sub>1h</sub> and should be included in the box. The line coming out of the "TYP h" box near the top of the box and going to R<sub>21</sub> and R<sub>22</sub> should be the V<sub>CC</sub> line, not the one parallel to and just above it as shown in the slash sheet. The base and emitter of Q<sub>24</sub> should not be shown shorted together, and the anode side of Z<sub>6c</sub> is missing a connection dot in the slash sheet. Corrections were made accordingly, so that the schematic of the devices analyzed is that shown in Figure 6.

Visual inspection of the chip was performed using Method 2010.3 of MIL-STD-883B as a guide. No weaknesses in workmanship were noted.

#### The Components

The substrate is P-type. Subcollectors approximately  $8 \mu\text{m}$  (.32 mils) deep, consisting of low resistivity N-type diffusions, are made in positions corresponding to the transistors

prior to the growth of the epitaxial layer. These provide high conductivity paths from the vicinity of the base-collector junctions to the collector contact diffusions. An N-type epitaxy about 2.8  $\mu\text{m}$  (.111 mils) thick is then grown.

After the growth of the epitaxial layer, P-type isolation diffusions approximately 4.0  $\mu\text{m}$  (0.157 mils) deep are made, partitioning the epitaxial layer into individual collector regions and other components. The P-type base diffusion follows, and the resistors are also made at this time. This diffusion was measured to be about 1.6  $\mu\text{m}$  (64 micromes) deep. This also creates the p-n junction guard rings for the input clamping diodes to be discussed later. The N<sup>+</sup>-type diffusion, measured to be about 1  $\mu\text{m}$  (39.4 micromes) deep, then creates the emitters and the collector contact enhancement regions. This latter is necessary to achieve ohmic contact to the low-doped epitaxial layer.

#### The Transistors

With the exception of Q<sub>4</sub>, Q<sub>9</sub>, Q<sub>12</sub>, Q<sub>16</sub>, and Q<sub>21</sub>, all transistors utilize the Schottky design. The base regions of these Schottky transistors are annular, having a rectangular "hole" within a rectangular shaped diffusion. Hence a portion of the epitaxial region at the surface is surrounded by this annular ring. The contact hole in the base oxide exposes both part of the base region and all of the epitaxial region which is surrounded by the base ring. This latter is part of the collector. When the metallization is deposited within the contact hole, it creates the ohmic contact to the base region and also creates the Schottky diode between base and collector. This occurs because of the relative doping level of the base region (high doping yields ohmic contact) versus that of the epitaxial (collector) region (low doping yields rectifying Schottky contact). The five transistors mentioned above as exceptions from this design are of standard bipolar construction. One of the Schottky transistors, Q<sub>1</sub>, is essentially eight transistors with common collectors and common emitters, each having a unique base. A photomicrograph of Q<sub>1</sub> with contacts labelled appears in Figure 8.

#### The Diodes

Each input has a Schottky barrier clamping diode to ground to provide protection for the input against negative voltage spikes. The construction is quite similar to that in the transistors, forming what is actually a p-n junction - Schottky barrier hybrid diode. A cross-sectional diagram (not to scale) of the construction of the input structure is shown in Figure 9, with a top view shown in Figure 10. References 1 and 2 describe the theory and advantages of such a structure.

### The Resistors

P-type base diffusion is used for all of the resistors. This diffusion has a resistivity of about  $1000\Omega/\square$ . This sheet resistance was obtained by counting squares and comparing to values shown in the electrical schematic in Figure 6. The diffusion depth was measured to be about  $1.6 \mu\text{m}$  (63 micches).

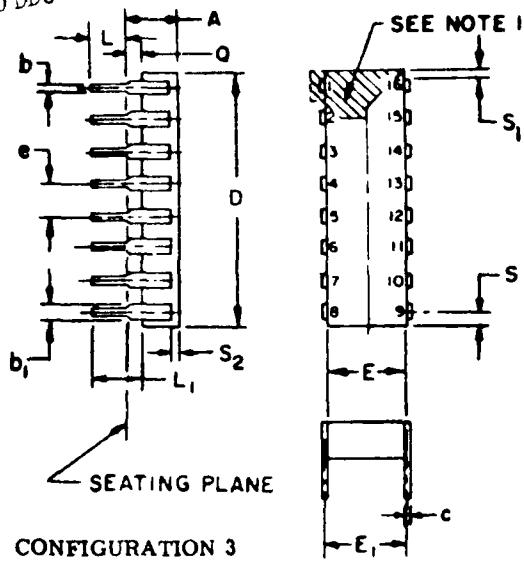
### CONCLUSIONS

The construction and workmanship of this device appear to be sound and in keeping with military specification, with one exception. Some differences were noted between the schematic diagram included for the device in the latest edition of the slash sheet and the actual layout of the device. These differences are detailed specifically above. No weaknesses in construction or workmanship were noted.

### REFERENCES

1. RADC-TR-76-292, Reliability Evaluation of Schottky Barrier Diode Microcircuits, Raytheon Company, Sept. 1976, Appendix B, p. 158.
2. R.A. Zettler and A.M. Cowley, "p-n Junction-Schottky Barrier Hybrid Diode" IEEE Transactions on E.D., Vol. ED-16, no. 1, January 1969.

THIS PAGE IS BEST QUALITY PRACTICABLE  
FROM OUR Y FILMISUE TO DDC



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		.200		5.08	
b	.014	.023	.36	.58	8
b <sub>1</sub>	.030	.070	.76	1.78	2, 8
c	.008	.015	.20	.38	8
D	.840			21.34	4
E	.220	.310	5.59	7.87	4
E <sub>1</sub>	.290	.320	7.37	8.13	7
E <sub>2</sub>	.100		2.54		
E <sub>3</sub>	.050		1.27		
e	.100 BSC		2.54 BSC		5, 9
L	.125	.203	3.18	5.08	
L <sub>1</sub>	.150		3.81		
Q	.015	.060	.38	1.52	3
Q <sub>1</sub>	.020		.51		
S		.080		2.03	6
S <sub>1</sub>	.005		.13		6
S <sub>2</sub>	.005		.13		
$\alpha$	0°	15°	0°	15°	

NOTES:

1. Index area; a notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The minimum limit for dimension b<sub>1</sub> may be .020 (.51 mm) for leads number 1, 8, 9 and 16 only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrum.
5. The basic pin spacing is .100 (2.54 mm) between centerlines. Each pin centerline shall be located within  $\pm .010$  (.25 mm) of its exact longitudinal position relative to pins 1 and 16.
6. Applies to all four corners (leads number 1, 8, 9, and 16), and 40.5 shall apply.
7. Lead center when  $\alpha$  is 0°. E<sub>1</sub> shall be measured at the centerline of the leads (see 40.4 of this appendix).
8. All leads - Increase maximum limit by .003 (.08 mm) measured at the center of the flat, when lead finish A is applied.
9. Fourteen spaces.
10. If this configuration is used, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.

Figure 1: Package outline and dimensions specified for 16-lead ceramic dual-in-line package (CERDIP).

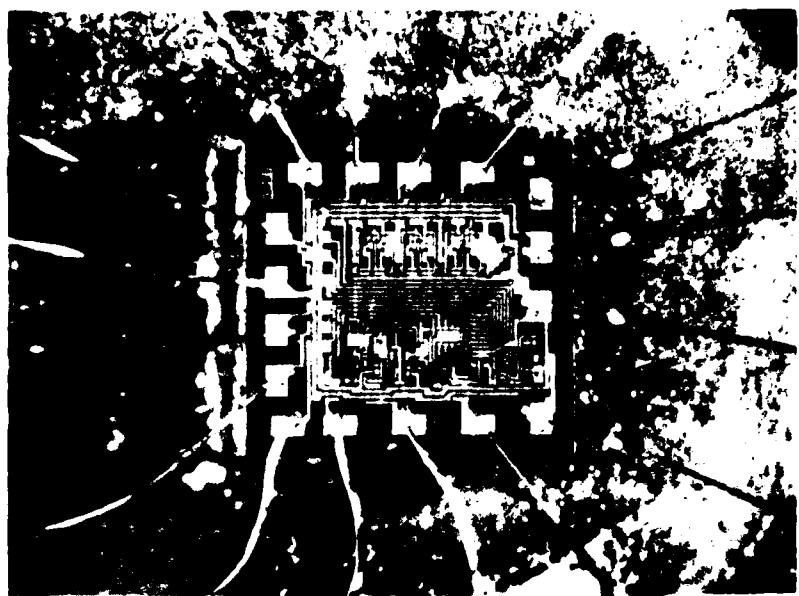
Figure 2. Package Dimensions

<u>Designation</u>	<u>Unit S/N 5</u>	<u>Unit S/N 9</u>
A	3.94 (.155)	3.96 (.156)
b	0.46 (.018)	0.43 (.017)
b <sub>1</sub>	1.52 (.06)	1.27 (.05)
C	0.28 (.011)	0.28 (.011)
D	19.5 (.767)	19.5 (.767)
E	6.32 (.249)	6.30 (.248)
E <sub>1</sub>	7.37 (.29)	7.62 (.30)
E <sub>2</sub>	---	---
E <sub>3</sub>	---	---
e	2.54 (.10)	2.54 (.10)
L	3.56 (.14)	3.30 (.13)
L <sub>1</sub>	4.32 (.17)	4.32 (.17)
Q	0.76 (.03)	0.76 (.03)
Q <sub>1</sub>	---	---
S	0.76 (.03)	0.51 (.02)
S <sub>1</sub>	0.76 (.03)	0.76 (.03)
S <sub>2</sub>	1.52 (.06)	1.52 (.06)

Note: Values shown outside parentheses are in millimeters;  
values within parentheses are in inches.



Figure 3: Device as received, showing package markings. Mag.:3X.



**Figure 4:** Overall view of internal package layout, showing chip and internal wires. Mag.: 36X.

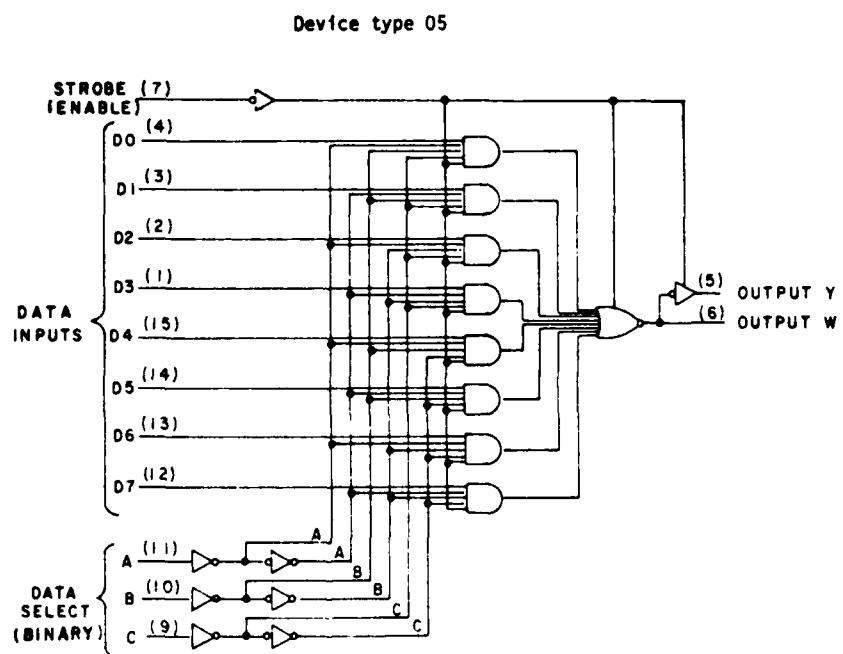


Figure 5: Logic diagram for the 54LS251.

DEVICE TYPES 01 AND 05

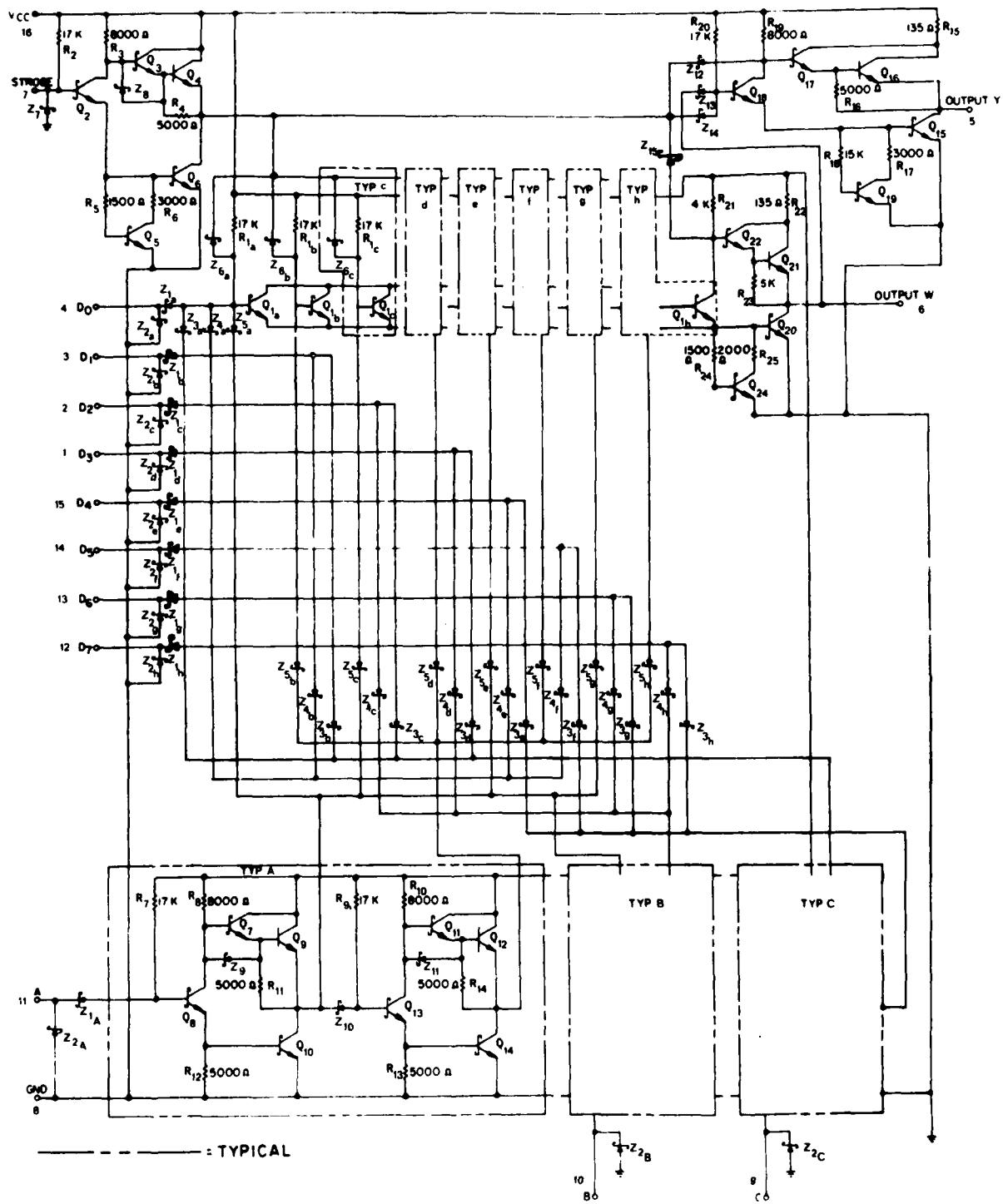


Figure 6: Detailed electrical schematic diagram of device.

THIS PAGE IS BEST QUALITY PRACTICABLE  
DO NOT SCALE THIS DRAWING

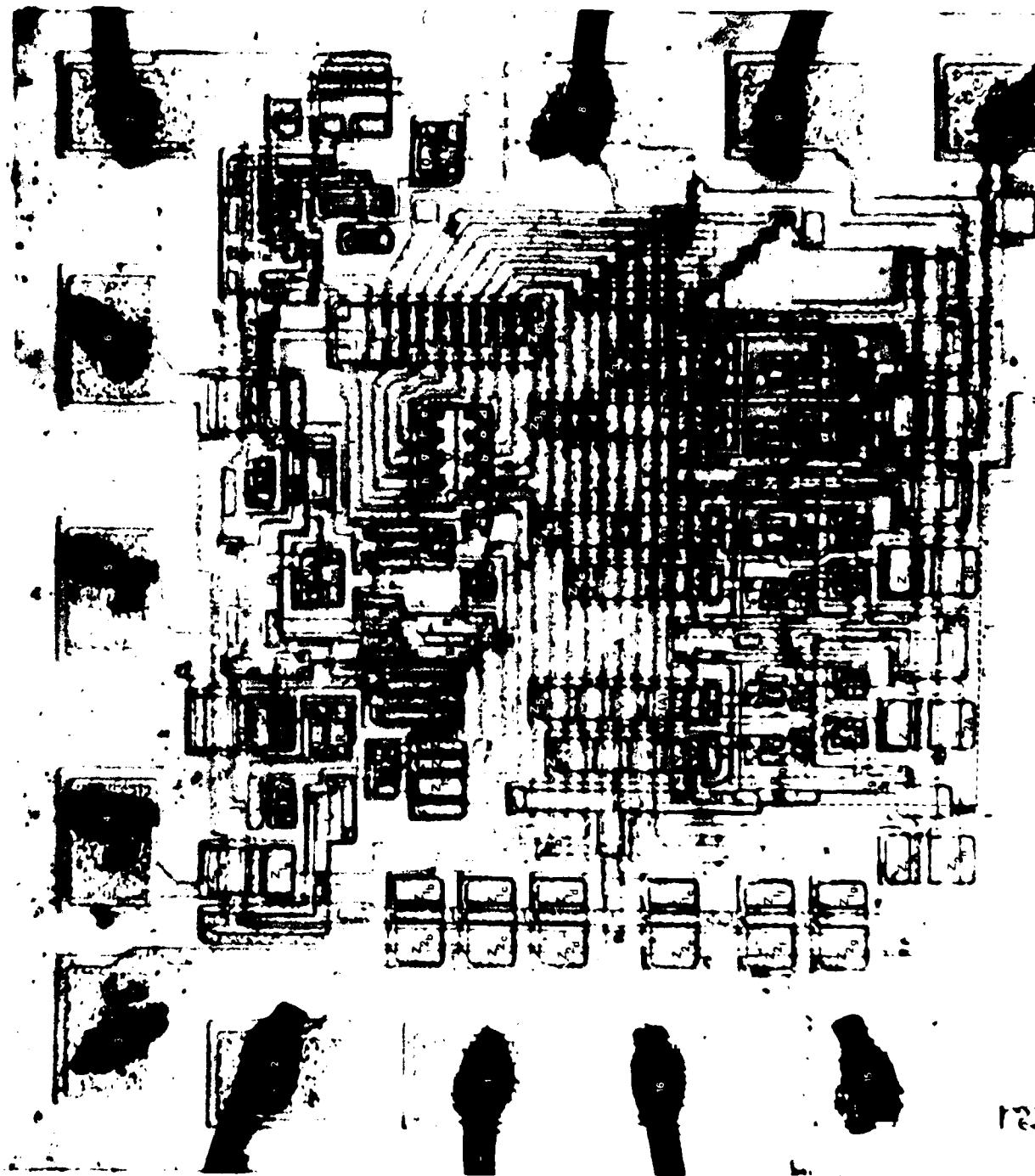


Figure 7: Overall view of chip, mapped with schematic symbols designations corresponding to Fig. 6 Mag: 100X.  
(Reversed image).

1: ~~PRINTED CIRCUITS - HIGH QUALITY PRACTICABLE~~  
~~PRINT COPY FEB 1968 BY 10000~~

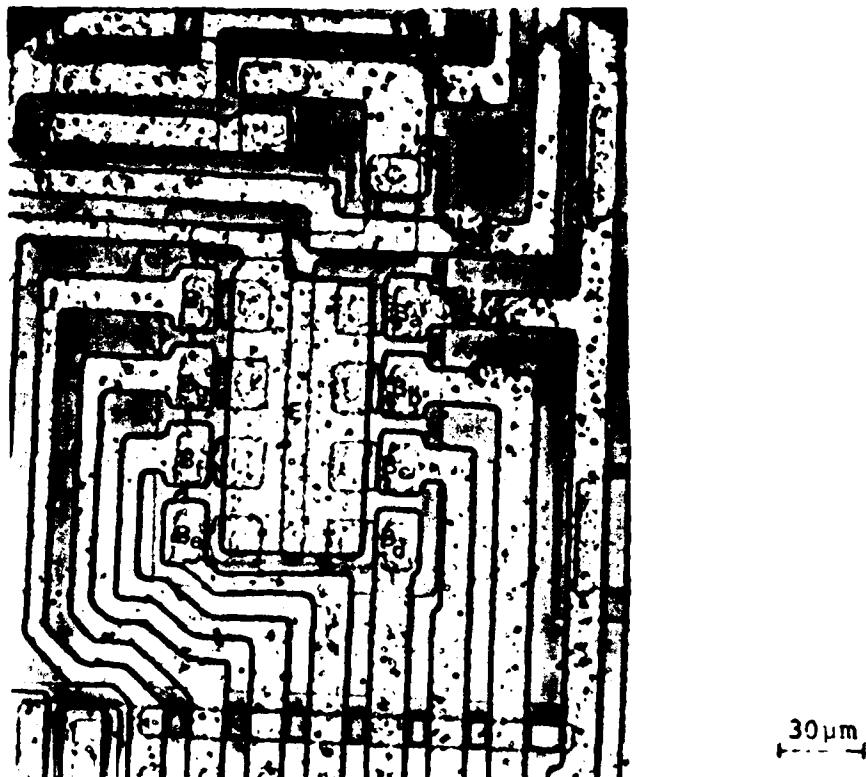
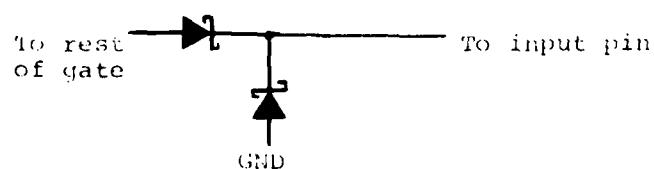
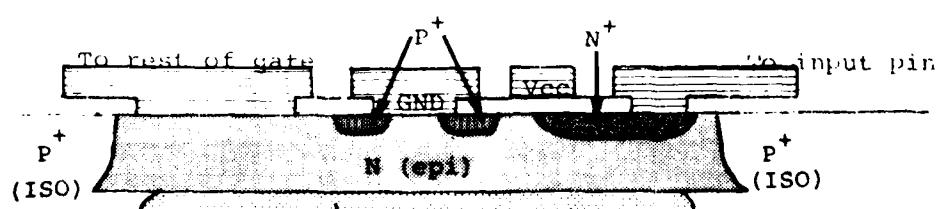
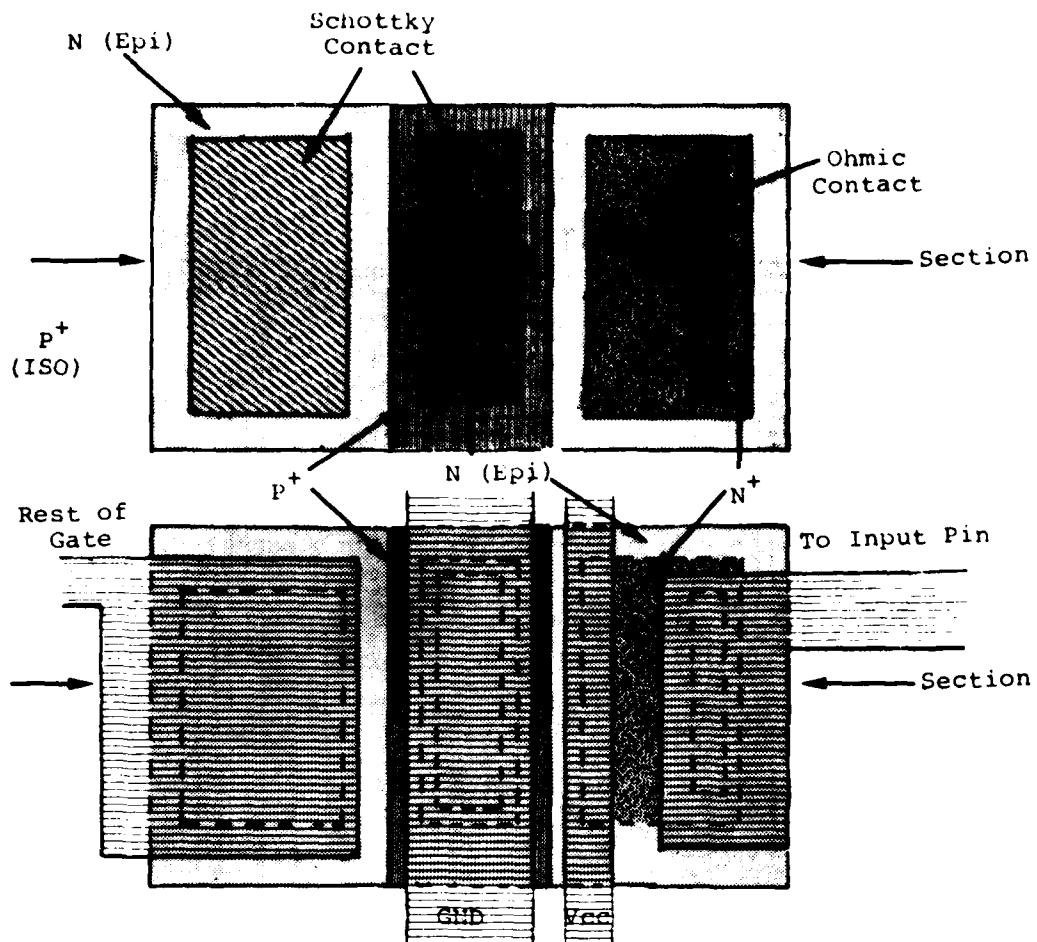


Figure 8: Photomicrograph of  $Q_1$ , actually eight transistors having common collectors and common emitters.



**FIGURE 9:** Schematic diagram showing cross-sectional view of input structure (not to scale).

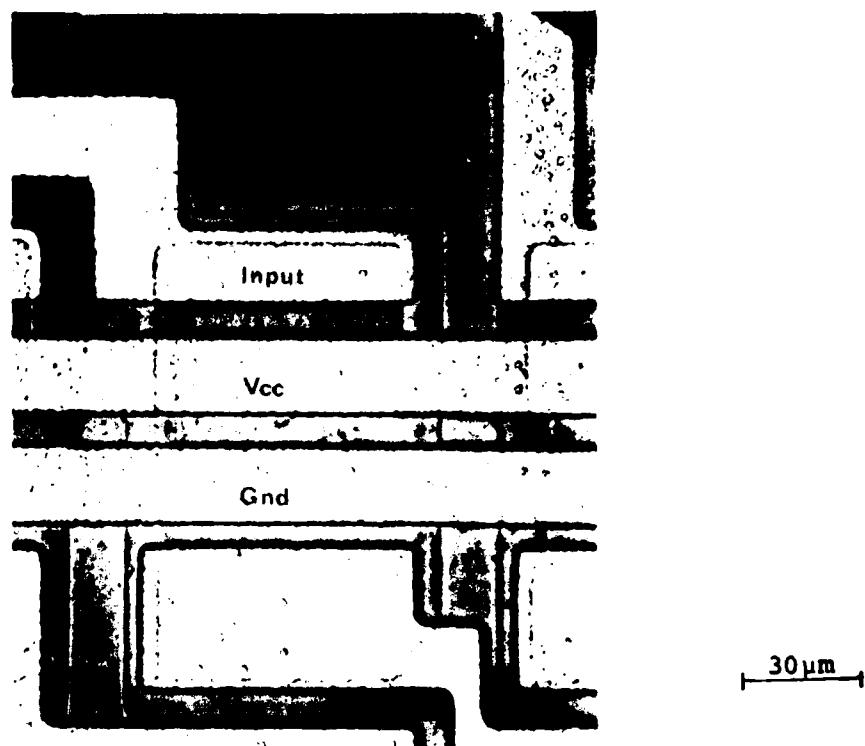


Figure 10: Photomicrograph of input structure.

APPENDIX D  
CONSTRUCTION ANALYSIS OF VENDOR B 54LS251  
STANDARD SCHOTTKY TTL INTEGRATED CIRCUIT IN CERAMIC DIP

ABSTRACT

A Vendor B high speed eight input digital multiplexer, incorporating full on-chip binary decoding to select one of eight data sources and featuring a strobe controlled tri-state output, was subjected to a detailed construction analysis. Two devices were received packaged in standard 16-pin ceramic dual-in-line packages (CERDIP's). One was date coded 7711 and the other 7712. They were low power Schottky devices. The internal wires were found to be 1 mil Al, while the single level chip metallization was as follows: vapor deposited Al over sputtered Ti-W over  $Pt_xSi_y$ . The chip was entirely coated with vapor deposited  $SiO_2$ . No weaknesses in construction or workmanship were noted.

INTRODUCTION

This analysis was performed as part of an evaluation of this device for Rome Air Development Center (RADC). The analysis was designed to document the construction details and materials used in these units and to identify shortcomings in the design or defects in workmanship, if any.

RESULTS

The Package

The units were packaged in 16-lead ceramic dual-in-line packages (CERDIP). Both lid and base were of smooth alumina, with a fritted glass seal. The leads were embedded in the seal and consisted of tin plated Kovar. Package dimensions were found to be within the limits specified in MIL-M-38510D and are shown in Figure 2; the case outline drawing and specifications for dimensions are shown in Figure 1. The package markings were as shown in Figure 3.

The leads consisted of a Kovar base with tin plating 7.50  $\mu\text{m}$  (300  $\mu\text{in.}$ ) thick. The area of the lead frame which made internal contacts to the aluminum wires was clad with aluminum. This is rolled on prior to assembly of the package, and was measured to be 3.5  $\mu\text{m}$  (140  $\mu\text{inches}$ ) thick.

#### The Chip

The lid was removed by applying a mechanical stress to it and forcing a chisel edge into the seal in a controlled manner until the seal fractured. An overall view of the cavity and chip of each device is shown in Figure 4. A comparison of the two chips showed that the masks had not changed between the times of manufacture. The chip was measured to be 13.4 x 1.44 x 0.210 mm (43 x 57.6 x 8.4 mils). The volume of the cavity was 0.027 cm<sup>3</sup>, including the recess in the package lid. The chip was mounted using a silicon-gold eutectic about 7  $\mu\text{m}$  (.28 mils) thick, with a thick film gold paste providing the gold. This thick film gold paste also contains minute glass particles which are fired into the ceramic at 920°C, thus providing the adhesion to the ceramic substrate. Away from the chip the gold metallization which lined the bottom of the cavity was measured to be 5  $\mu\text{m}$  (.20 mils) thick and the presence of voids was noted. Thermal resistances were measured to be  $\theta_{\text{junction-to-air}} = 145.1^{\circ}\text{C/W}$  and  $\theta_{\text{junction-to-case}} = 27.8^{\circ}\text{C}$ .

The internal wires were ultrasonically bonded, 1 mil diameter aluminum. Microbond-pull testing of 8 of the 14 wires yielded a range in pull strength from 3.0 to 5.5 grams-force, with an average of 4.0. These wires exceed the pull-strength of 2 gm-f specified in MIL-STD-883B.

The chip metallization was a single level interconnection scheme which used aluminum 2.4  $\mu\text{m}$  (94  $\mu\text{inches}$ ) thick over a Ti-W layer approximately 2500A thick. The presence of the Ti-W layer provides good adhesion to the Si and SiO<sub>2</sub> and is a diffusion barrier to the aluminum. The platinum-silicide in the contact areas gives good ohmic and Schottky barrier contact. The above thicknesses were measured in an angle cross-section. The aluminum layer was vapor deposited and the Ti-W was sputter deposited in an undisclosed ratio. The Pt<sub>x</sub>Si<sub>y</sub> was formed by sputtering on Pt in a very thin layer and sintering to form Pt<sub>x</sub>Si<sub>y</sub> in the contact areas, followed by a blanket etching to remove the Pt elsewhere. A SiO<sub>2</sub> layer about 2.4  $\mu\text{m}$  (94  $\mu\text{in.}$ ) thick covered the entire chip as passivation and protection against scratching during handling.

The highest current density was found to exist in the emitter metallization from the output transistor at output y and w (pins 5 & 6). Here the current is 1.6mA maximum and the metallization is  $1.1 \times 10^{-3}$  cm wide by  $2.4 \times 10^{-4}$  cm thick, resulting in a current density of  $6.1 \times 10^3$  A/cm<sup>2</sup>. Over an oxide step the current density could reach  $9.1 \times 10^3$  A/cm<sup>2</sup>, since the metallization thins to about 2/3 its thickness as it goes over an oxide step. This is within the MIL-M-38510 specification of  $5 \times 10^5$  A/cm<sup>2</sup> as a maximum current density for Al to avoid an unacceptable level of electromigration.

The chip was photographed and mapped to identify all the components. Figure 5 shows the logic layout of the device as related to the external pin connections and Figure 6 shows a detailed schematic of the device. Figure 7 shows the chip with all of the components labelled with the schematic symbol designations corresponding to those given in Figure 6.

Visual inspection of the chip was performed using Method 2010.3 of MIL-STD-883B as a guide. No weaknesses in construction or workmanship defects were found.

#### The Components

The substrate is P-type. Subcollectors approximately 200  $\mu\text{m}$  (7.8 mils) deep, consisting of low resistivity N-type diffusions, are made in positions corresponding to the transistors prior to the growth of the epitaxial layer. These provide high conductivity paths from the vicinity of the base-collector junctions to the collector contact diffusions. An N-type epitaxy about 3.5  $\mu\text{m}$  (.138 mils) thick is then grown.

After the growth of the epitaxial layer, P-type isolation diffusions approximately 4.4  $\mu\text{m}$  (0.17 mils) deep are made, partitioning the epitaxial layer into individual collector regions and other components. The P-type base diffusion follows, and the resistors are also made at this time. This diffusion was measured to be about 2.0  $\mu\text{m}$  (78  $\mu\text{inches}$ ) deep. This also creates the p-n junction guard rings for the input clamping diodes to be discussed later. The N<sup>+</sup>-type diffusion, measured to be about 1  $\mu\text{m}$  (39  $\mu\text{inches}$ ) deep, then creates the emitters and the collector contact enhancement regions. This latter is necessary to achieve ohmic contact to the low-doped epitaxial layer.

### The Transistors

With the exception of  $Q_4$ ,  $Q_9$ ,  $Q_{12}$ ,  $Q_{16}$ , and  $Q_{21}$ , all transistors utilize the Schottky design. The base regions of these Schottky transistors are annular, having a rectangular "hole" within a rectangular shaped diffusion. Hence a portion of the epitaxial region at the surface is surrounded by this annular ring. The contact hole of the base oxide exposes both part of the base region and all of the epitaxial region which is surrounded by the base ring. This latter is part of the collector. When the metallization is deposited within the contact hole, it creates the ohmic contact to the base region and also creates the Schottky diode between base and collector. This occurs because of the relative doping level of the base region (high doping yields ohmic contact) versus that of the epitaxial (collector) region (low doping yields rectifying Schottky contact). The five transistors mentioned above as exceptions from this design are of standard bipolar construction. One of the Schottky transistors,  $Q_1$ , is essentially eight transistors with common collectors and common emitters, each having a unique base. A photomicrograph of  $Q_1$  with contacts labelled appears in Figure 8.

### The Diodes

Each input has a Schottky barrier clamping diode to ground to provide protection for the input against negative voltage spikes. The construction is quite similar to that in the transistors, forming what is actually a p-n junction - Schottky barrier hybrid diode. A cross-sectional diagram (not to scale) of the construction of the input structure is shown in Figure 9, and a photomicrograph showing the top view appears in Figure 10. References 1 and 2 describe the theory and advantages of such a structure.

### The Resistors

P-type base diffusion is used for all of the resistors. This diffusion has a resistivity of about  $1000\Omega/\square$ . This sheet resistance was obtained by counting squares and comparing to values shown in the electrical schematic in Figure 6. The diffusion depth was measured to be about  $2.0 \mu m$  ( $78 \mu$  inches).

### CONCLUSIONS

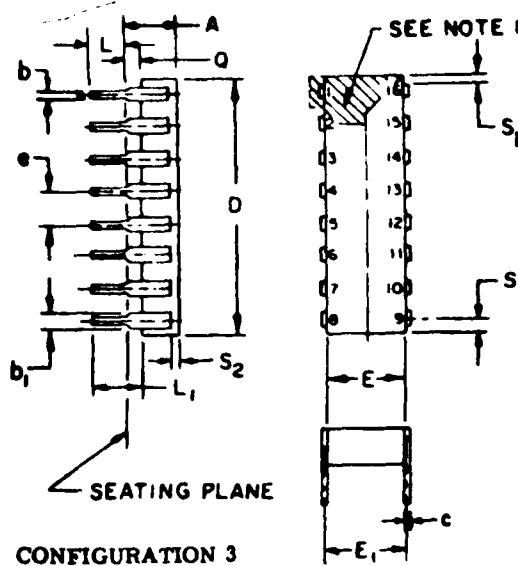
The construction and workmanship of this device appear to be sound and in keeping with military specification.

This evaluation of the device from a reliability stand-point revealed no weaknesses in construction or workmanship.

REFERENCES

1. RADC-TR-76-292, Reliability Evaluation of Schottky Barrier Diode Microcircuits, Raytheon Company, Sept 1976, Appendix B, p. 158, A032001.
2. R. A. Zettler and A. M. Cowley, "p-n Junction Schottky Barrier Hybrid Diode" IEEE Transactions on E.D., Vol. ED-16, no. 1, January 1969.

THIS PAGE IS BEST QUALITY PRACTICABLE  
FROM COPY FILMED 100000



CONFIGURATION 3

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	.014	.024	.36	.58	8
b <sub>1</sub>	.030	.070	.76	1.74	2, 8
c	.008	.013	.20	.38	8
D		.040		2.34	4
E	.220	.310	5.59	7.87	4
E <sub>1</sub>	.290	.320	7.37	8.13	7
E <sub>2</sub>	.100		2.54		
E <sub>3</sub>	.050		1.27		
e	100 BSC		2.54 BSC		5, 9
L	.125	.200	3.18	5.08	
L <sub>1</sub>	.150		3.81		
Q	.015	.060	.38	1.52	3
Q <sub>1</sub>	.020		.51		
S		.080		2.03	6
S <sub>1</sub>	.005		.13		6
S <sub>2</sub>	.005		.13		
a	0°	15°	0°	15°	

NOTES:

- Index area; a notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
- The minimum limit for dimension b<sub>1</sub> may be .020 (.51 mm) for leads number 1, 8, 9 and 16 only.
- Dimension Q shall be measured from the seating plane to the base plane.
- This dimension allows for off-center lid, meniscus and glass overrun.
- The basic pin spacing is .100 (2.54 mm) between centerlines. Each pin centerline shall be located within ±.010 (.25 mm) of its exact longitudinal position relative to pins 1 and 16.
- Applies to all four corners (leads number 1, 8, 9, and 16), and 40.5 shall apply.
- Lead center when a is 0. E<sub>1</sub> shall be measured at the centerline of the leads (see 40.4 of this appendix).
- All leads - Increase maximum limit by .003 (.08 mm) measured at the center of the flat, when lead finish A is applied.
- Fourteen spaces.
- If this configuration is used, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.

Figure 1: Package outline and dimensions specified for 16-lead ceramic dual-in-line package (CERDIP).

Figure 2: Package dimensions as measured

<u>Designation</u>	<u>Measured Value</u>
A	3.9 (.153)
b	0.50 (.020)
b <sub>1</sub>	1.50 (.059)
C	0.30 (.012)
D	19.1 (.752)
E	6.3 (.248)
E <sub>1</sub>	7.9 (.311)
E <sub>2</sub>	---
E <sub>3</sub>	---
e	2.5 (.098)
L	3.7 (.146)
L <sub>1</sub>	5.7 (.224)
Q	1.9 (.075)
Q <sub>1</sub>	0.8 (.031)
S	0.9 (.035)
S <sub>1</sub>	1.0 (.039)
S <sub>2</sub>	1.6 (.063)

Note: Values shown outside parentheses are in millimeters,  
values within parentheses are in inches.



Figure 3: Devices as received, showing package markings. Note the different date codes. Mag.: 3X.

THIS PAGE IS BEST QUALITY PRACTICABLE  
COPY STANISHED TO EDC

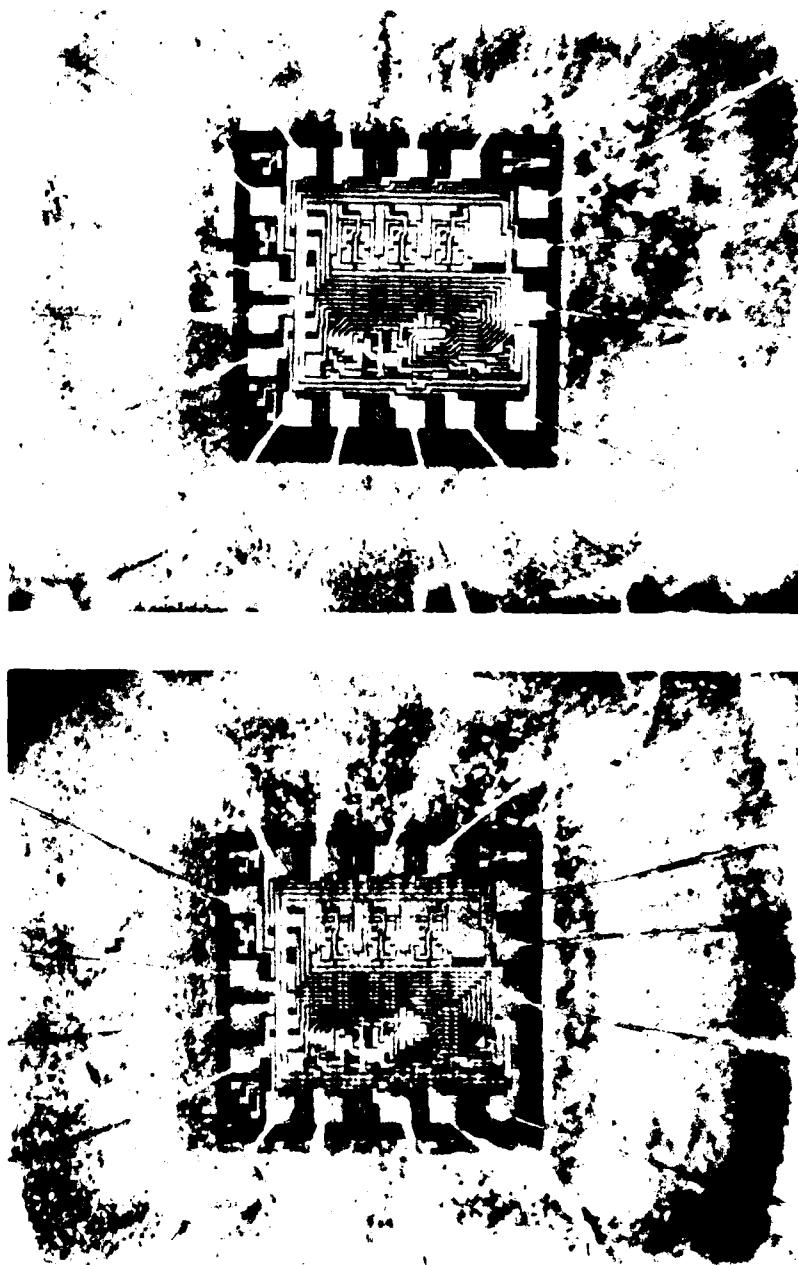


Figure 4: (a) Overall view of chip and internal package of unit date coded 7711 and (b) The same for unit date coded 7712. Mag.: 35X.

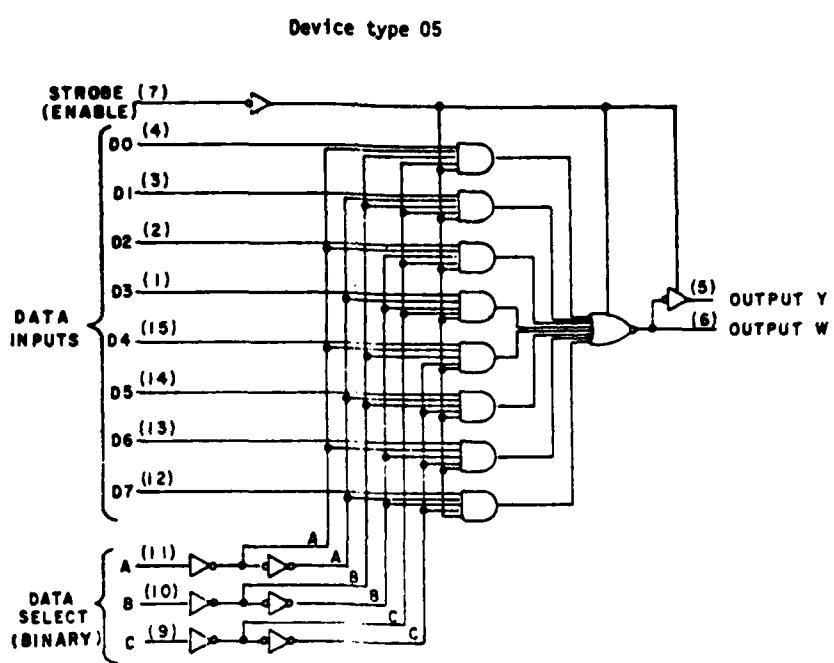


Figure 5: Logic diagram for the device (type 54LS251).

THIS PAGE IS BEST QUALITY PRACTICABLE  
FROM COPY FURNISHED TO DDC

DEVICE TYPES 01 AND 05

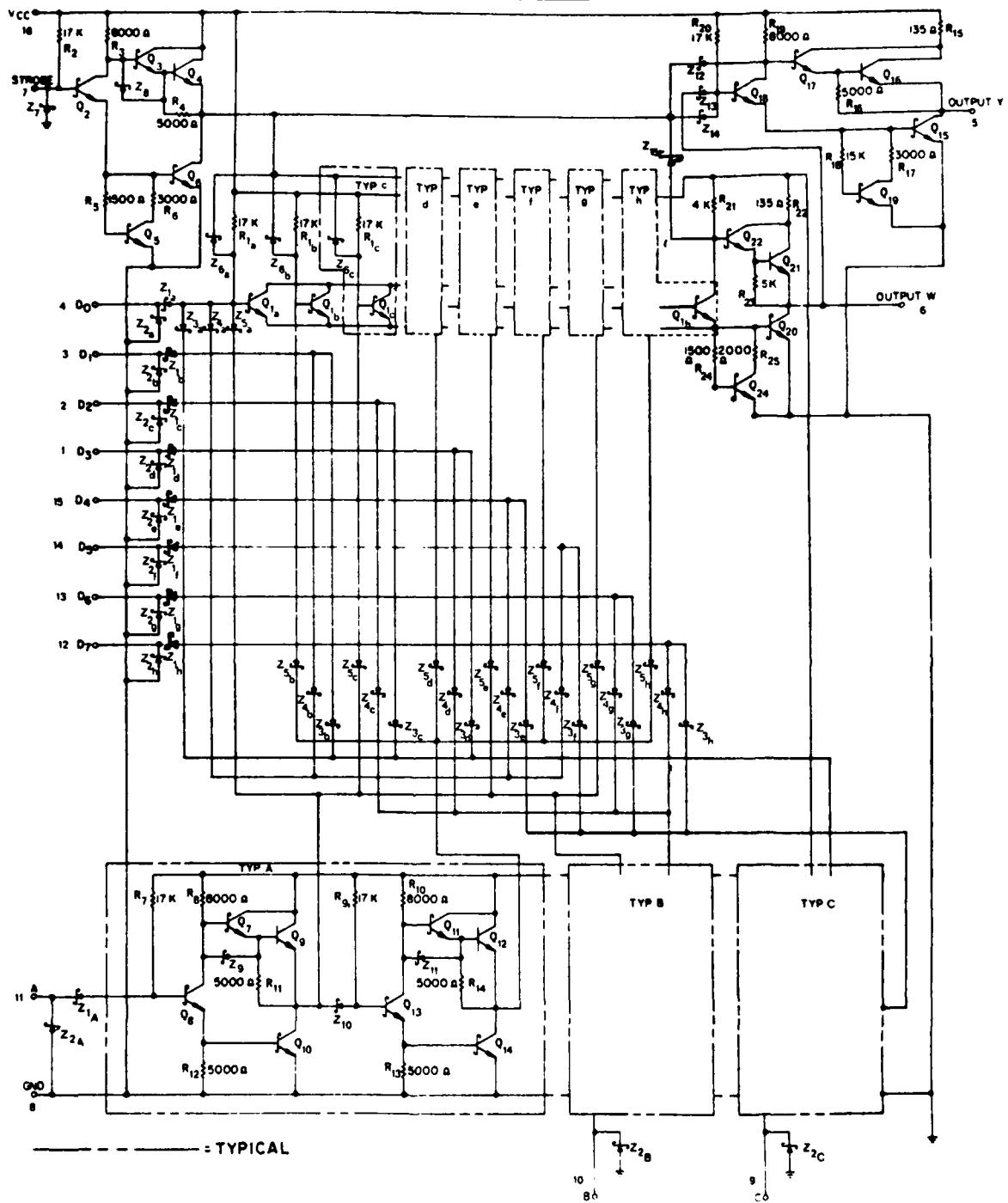


Figure 6: Detailed electrical schematic diagram of device.

PRINTED IN U.S.A. QUALITY PRACTICABLE  
PRINTING CO., INC. 1000

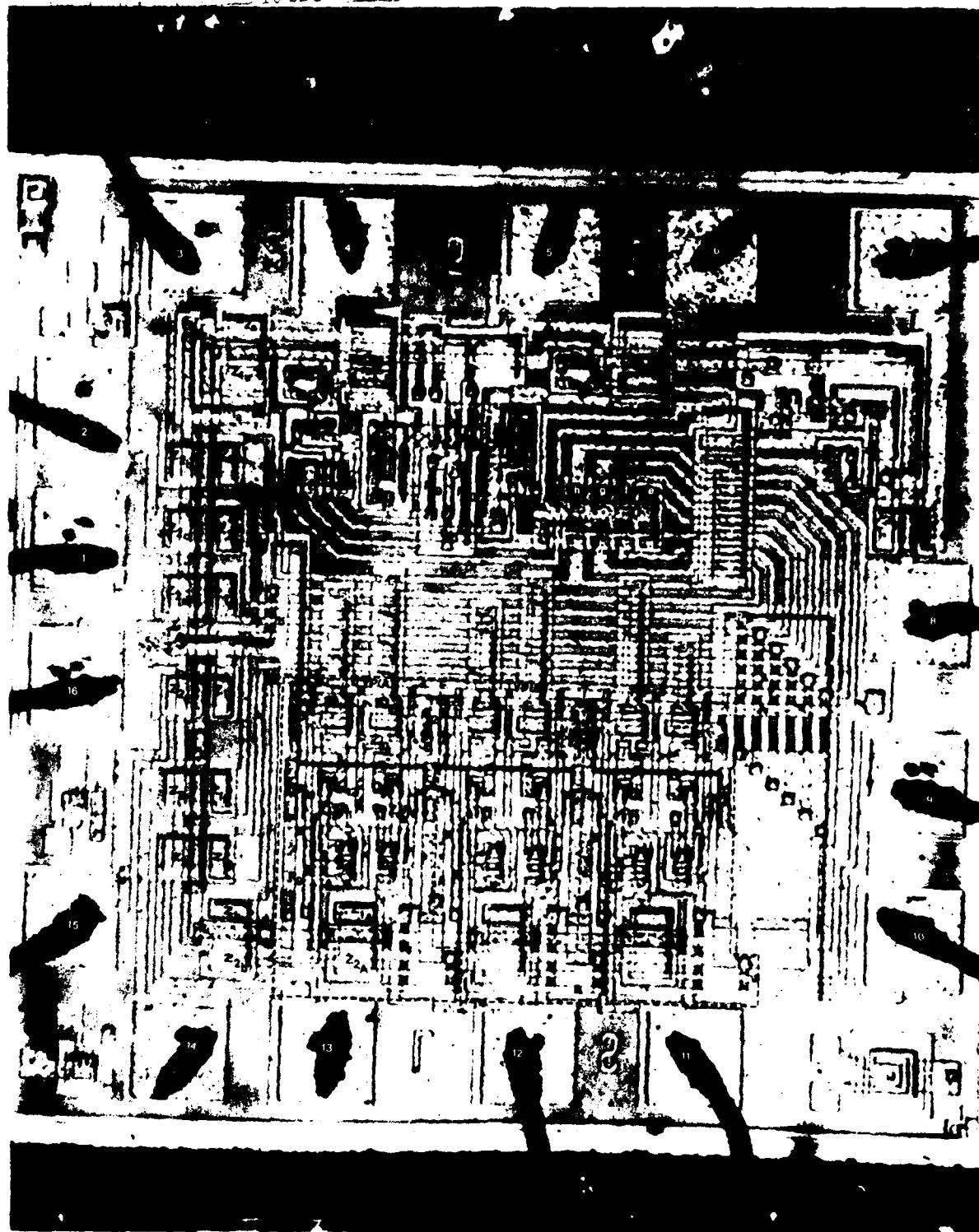


Figure 7: Overall view of the chip, mapped with schematic symbol designations corresponding to Figure 6.  
Mag.: 100X (reversed image).

THIS PAGE IS BEST QUALITY PRACTICABLE  
FROM COPY FURNISHED TO DDC

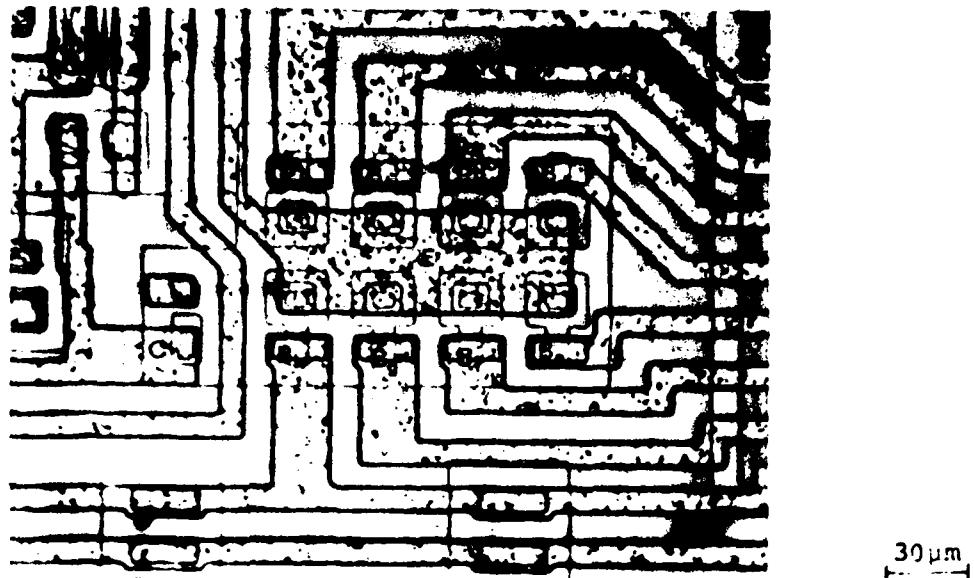


Figure 8: Photomicrograph of  $Q_1$ , actually eight transistors having common collectors and common emitters.

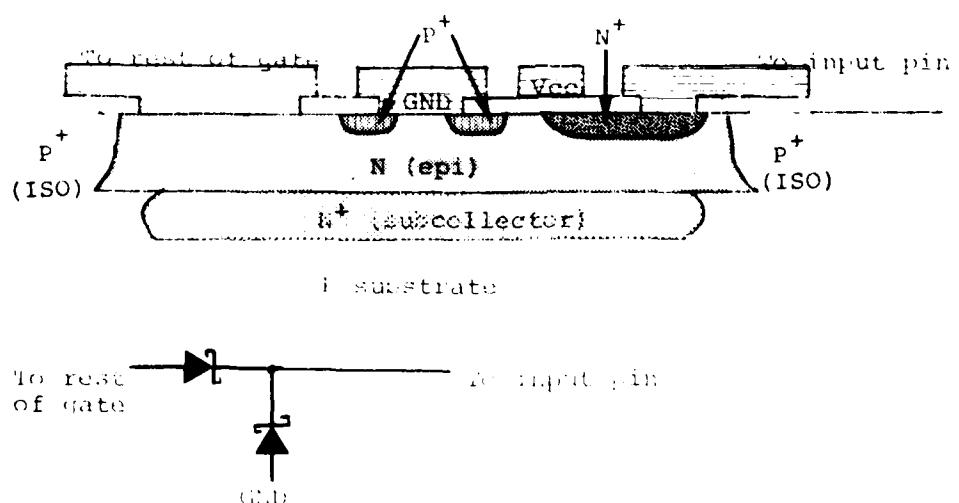
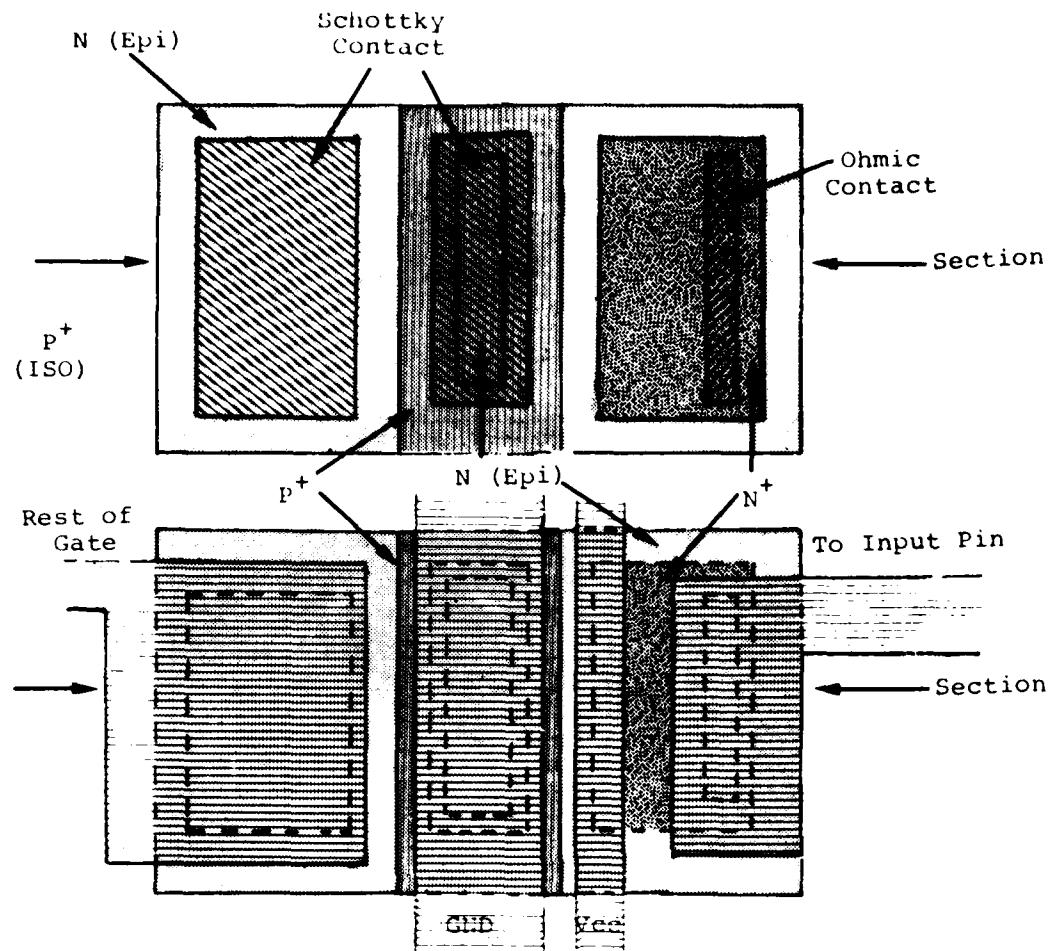


Figure . Schematic diagram showing cross-sectional view of input structure (not to scale).

THIS PAGE IS OF HIGH QUALITY PRACTICABLE  
FROM COMPUTER TO PLOTTER

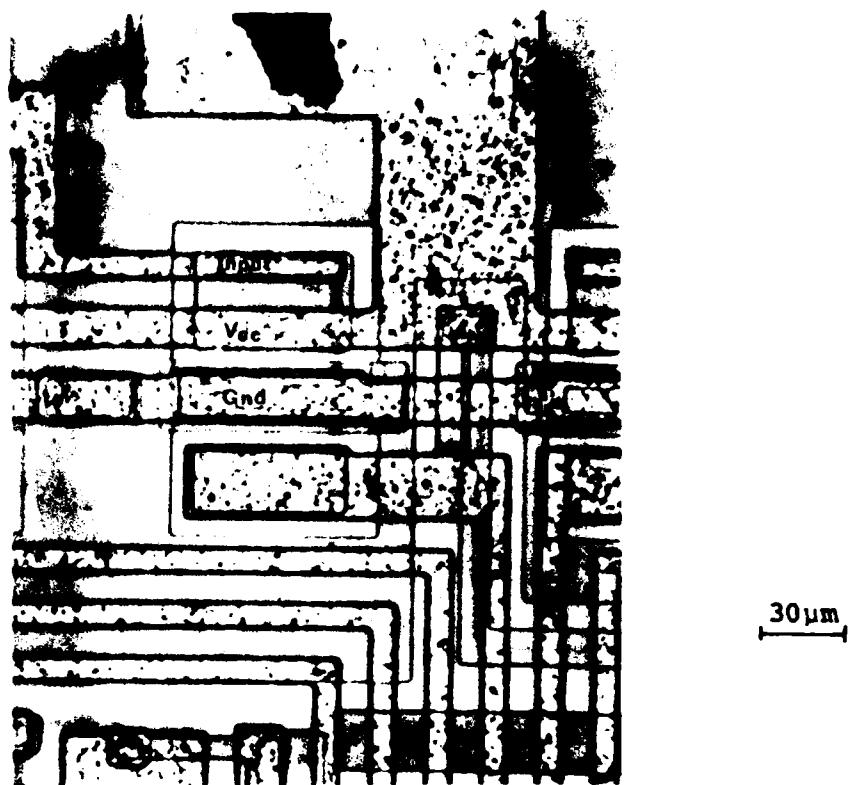


Figure 10: Photomicrograph of input structure.

## APPENDIX E

### CONSTRUCTION ANALYSIS OF VENDOR A 54LS283

#### STANDARD SCHOTTKY TTL INTEGRATED CIRCUIT IN CERAMIC DIP

##### Abstract

A Vendor A high speed 4-Bit binary full adder with internal carry look ahead was subjected to a detailed construction analysis. The device accepts two 4-bit binary words and a carry input and generates the binary sum outputs and the carry output from the most significant bit. Device complexity is 36 equivalent gates, and low power Schottky technology is employed in the device fabrication.

Two devices were received packaged in standard 16-pin ceramic dual-in-line packages (CERDIP's) date coded 7732. The leads were tin plated Kovar; the internal wires were 1 mil aluminum, having better than adequate pull-strengths. The single level chip metallization was vapor deposited Al over sputtered Ti-W over Pt<sub>x</sub>Si<sub>y</sub>. The chip is entirely covered with vapor deposited PSG for scratch protection and passivation. A defect in the oxide near pad 14 was noted, and the wire bonds at pads 7 and 13 were of questionable integrity, as they just met the requirements for internal visual inspection under MIL-STD-883B, Method 2010.3, Test Condition B. No other weaknesses in construction or workmanship were noted.

##### Introduction

This analysis was performed as part of an evaluation of this device for Rome Air Development Center (RADC). The analysis was designed to document the construction details and materials used in these units and to identify shortcomings in the design or defects in workmanship, if any.

##### Results

###### The Package

The units were packaged in 16-lead ceramic dual-in-line packages (CERDIP). Both lid and base were of smooth alumina, with a fritted glass seal. The leads were embedded in the seal and

consisted of tin plated Kovar. The thickness of the tin plating was measured to be  $5.0\mu\text{m}$  ( $200\mu\text{inches}$ ). The package dimensions were found to be within the limits specified in MIL-M-38510D and are shown in Figure 2; the case outline drawing and specifications for dimensions are shown in Figure 1. The package markings were as shown in Figure 3.

The internal area of the lead frame which is used for bonding pads for the aluminum wires was clad with aluminum. This is rolled on prior to assembly of the package, and was measured to be  $8.1\mu\text{m}$  ( $320\mu\text{inches}$ ) thick.

#### The Chip

The lid was removed by applying a mechanical stress to it and forcing a chisel edge into the seal in a controlled manner until the seal fractured. An overall view of the chip is shown in Figure 4. The chip was measured to be  $1.58 \times 1.74 \times 0.19\text{mm}$  ( $62.2 \times 68.5 \times 7.5$  mils). The volume of the cavity was  $0.031\text{ cm}^3$ , including the recess in the package lid. The chip was mounted using a silicon-gold eutectic approximately  $14.3\mu\text{m}$  ( $0.56$  mils) thick, with a thick film gold paste providing the gold. This thick film gold paste also contains minute glass particles which are fired into the ceramic at  $920^\circ\text{C}$ , thus providing the adhesion to the ceramic substrate. Away from the chip the gold metallization which lined the bottom of the cavity was measured to be about  $11\mu\text{m}$  ( $0.43$  mils) thick. Thermal resistances were measured to be  $\theta_{\text{junction-to-air}} = 118.5^\circ\text{C/W}$  and  $\theta_{\text{junction-to-case}} = 17.9^\circ\text{C/W}$ .

The internal wires were ultrasonically bonded, 1 mil diameter aluminum. Microbond-pull testing of 8 of the 16 wires yielded a range in pull strength from 4.5 to 5.0 grams-force, with an average of 5.3. These wires exceed the minimum pull-strength of 2 gm-f specified in MIL-STD-883B, Method 2011.2. No bond defects were noted.

The chip metallization was a single level interconnection scheme which used aluminum  $1.6\mu\text{m}$  ( $63\mu\text{inches}$ ) thick over a Ti-W layer approximately  $3200\text{A}$  thick. The presence of the Ti-W layer provides good adhesion to the Si and  $\text{SiO}_2$  and is a diffusion barrier to the aluminum. The platinum-silicide in the contact areas gives good ohmic contact for base (P) and emitter diffusion ( $N^+$ ) and Schottky barrier contacts for collector diffusion ( $N^+$ ). The above thicknesses were measured in an angle cross-section. The aluminum layer was vapor deposited and the Ti-W was sputter deposited in an undisclosed ratio. The  $\text{Pt}_x\text{Si}_y$  is formed by sputtering on Pt in a very thin layer and

sintering to form  $\text{Pt}_x\text{Si}_y$  in the contact areas, followed by blanket etching to remove the Pt elsewhere. A PSG layer about  $1.6\mu\text{m}$  ( $63\mu\text{inches}$ ) thick covered the entire chip as passivation and protection against scratching during handling.

The highest current density was found to exist in the metallization run between the emitter of Q36 and the base of Q30. Here the current is 1.6mA maximum and the smallest metallization width is  $5.65 \times 10^{-4}\text{cm}$ . The metallization thickness of  $1.6 \times 10^{-4}\text{cm}$  results in a minimum cross-sectional area of  $9.2 \times 10^{-8}\text{cm}^2$ , which yields a maximum current density of  $1.8 \times 10^4 \text{ A/cm}^2$ . Over an oxide step the current density could reach  $2.7 \times 10^4 \text{ A/cm}^2$ , since the metallization thins to about 2/3 its thickness as it goes over an oxide step. This is within the specification of  $5 \times 10^5 \text{ A/cm}^2$  found in MIL-M-38510 as a maximum current density for Al to avoid an unacceptable level of electromigration.

The chip was photographed and mapped to identify all the components. Figure 5 shows the logic layout of the device as related to the external pin connections and Figure 6 shows a detailed schematic of the device. Figure 7 shows the chip with all of the components labelled with the schematic symbol designations corresponding to those given in Figure 6.

Visual inspection of the chip was performed using Method 2010.3 of MIL-STD-883B as a guide, and some workmanship weaknesses which pose potential reliability problems were noted. The first was the presence of an oxide defect near pad 14 of the chip. The other two weaknesses were not bad enough to meet the criteria for a reject under Method 2010.3, but both came close to meeting these criteria and so are mentioned here in order to identify them as potential reliability hazards. In one case, barely 50% of the bond at pad 13 was on the bond pad area. Method 2010.3 Test Condition B specifies a minimum of 50% of the area of the bond to be on the pad in order for the device not to be considered a reject. In the other case, there was barely a clear metallization path in view at the exit from pad 7, as the placement of the wire bond had nearly obstructed this path entirely from view. Method 2010.3 specifies that a clear path be visible where the metallization exits the bond pad in order for the device not to be considered a reject. Other than these workmanship weaknesses, no faults were found in the construction of the device.

### The Components

The substrate was P-type. Subcollectors approximately  $8\mu\text{m}$  (.32 mils) deep, consisting of low resistivity N-type diffusions, were made in positions corresponding to the transistors prior to the growth of the epitaxial layer. These provided high conductivity paths from the vicinity of the base-collector junctions to the collector contact diffusions. An N-type epitaxy about  $3.3\mu\text{m}$  (.13 mils) thick was then grown.

After the growth of the epitaxial layer, P-type isolation diffusions approximately  $5.4\mu\text{m}$  (0.21 mils) deep were made, partitioning the epitaxial layer into individual collector regions and other components. The P-type base diffusion followed and the resistors were also made at this time. This diffusion was measured to be about  $1.6\mu\text{m}$  ( $64\mu\text{inches}$ ) deep. This also created the p-n junction guard rings for the input clamping diodes to be discussed later. The N+-type diffusion, measured to be about  $1\mu$  ( $39.4\mu\text{inches}$ ) deep, then created the emitters and the collector contact enhancement regions. This latter was necessary to achieve ohmic contact to the low-doped epitaxial layer.

### The Transistors

With the exception of  $Q_2$ ,  $Q_8$ ,  $Q_{14}$ ,  $Q_{17}$ ,  $Q_{18}$ ,  $Q_{22}$ ,  $Q_{27}$ , and  $Q_{28}$ , all transistors utilized the Schottky design. The base regions of these Schottky transistors were annular, having a rectangular "hole" within a rectangular shaped diffusion. Hence a portion of the epitaxial region at the surface was surrounded by this annular ring. The contact hole in the base oxide exposed both part of the base region and all of the epitaxial region which was surrounded by the base ring. This latter was part of the collector. When the metallization was deposited within the contact hole, it created the ohmic contact to the base region and also created the Schottky diode between base and collector. This occurred because of the relative doping level of the base region (high doping yields ohmic contact) versus that of the epitaxial (collector) region (low doping yields rectifying Schottky contact). The eight transistors mentioned above as exceptions from this design were standard bipolar construction.

### The Diodes

Each input had a Schottky barrier diode to ground to provide protection for the input against negative voltage spikes. The construction was quite similar to that in the

transistors, forming what was actually a p-n junction - Schottky barrier hybrid diode. A cross-sectional diagram (not to scale) of the construction of the input structure is shown in Figure 8, with a top view shown in Figure 9. References 1 and 2 describe the theory and advantages of such a structure.

#### The Resistors

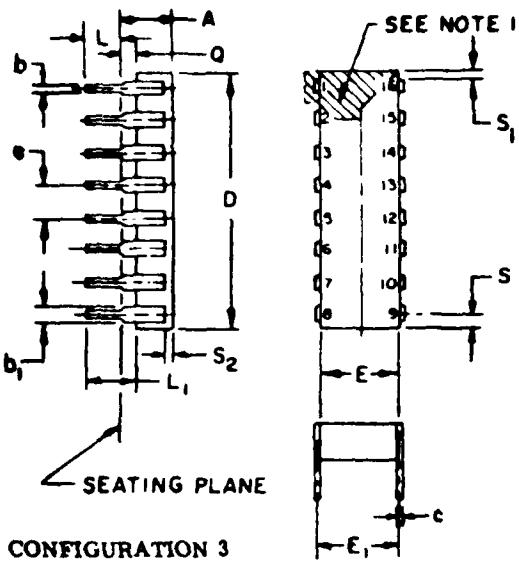
P-type base diffusion was used for all of the resistors. This diffusion had a resistivity of about  $1000\Omega/\square$ . This sheet resistance was obtained by counting squares and comparing to values shown in the electrical schematic in Figure 6. The diffusion depth was measured to be about  $1.6\mu\text{m}$  ( $63\mu\text{inches}$ ).

#### Conclusions

The construction and workmanship of this device appear to be sound and in keeping with military specification, although three exceptions were noted. The first was the presence of an oxide defect near chip pad 14. The other two defects were identified as potential bonding problems at chip pads 7 and 13, and these were detailed specifically above. While both of these latter two met minimum requirements for internal visual inspection given in MIL-STD-883B, Method 2010.3, Test condition B, they did present potential reliability hazards. Other than these defects, no weaknesses in construction or workmanship were found.

#### References

1. RADC-TR-76-292, Reliability Evaluation of Schottky Barrier Diode Microcircuits, Raytheon Company, Sept. 1976, Appendix B, p. 158.
2. R.A. Zettler and A.M. Cowley, "p-n Junction-Schottky Barrier Hybrid Diode" IEEE Transactions on E.D., Vol. ED-16, no. 1, January 1969.



CONFIGURATION 3

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		.200		5.08	
b	.014	.023	.36	.58	8
b <sub>1</sub>	.030	.070	.76	1.78	2, 8
c	.008	.015	.20	.38	8
D		.840		21.34	4
E	.220	.310	5.59	7.87	4
E <sub>1</sub>	.290	.320	7.37	8.13	7
E <sub>2</sub>	.100		2.54		
E <sub>3</sub>	.050		1.27		
c	100 BSC		2.54 BSC		5, 9
L	.125	.200	3.18	5.08	
L <sub>1</sub>	.150		3.81		
Q	.015	.060	.38	1.32	3
Q <sub>1</sub>	.020		.51		
S		.080		2.03	8
S <sub>1</sub>	.005		.13		8
S <sub>2</sub>	.005		.13		
o	0°	15°	0°	15°	

NOTES:

- Index area; a notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
- The minimum limit for dimension b<sub>1</sub> may be .020 (.51 mm) for leads number 1, 8, 9 and 16 only.
- Dimension Q shall be measured from the seating plane to the base plane.
- This dimension allows for off-center lid, meniscus and glass overrun.
- The basic pin spacing is .100 (2.54 mm) between centerlines. Each pin centerline shall be located within ±.010 (.25 mm) of its exact longitudinal position relative to pins 1 and 16.
- Applies to all four corners (leads number 1, 8, 9, and 16), and 40.5 shall apply.
- Lead center when o is 0°. E<sub>1</sub> shall be measured at the centerline of the leads (see 40.4 of this appendix).
- All leads - Increase maximum limit by .003 (.08 mm) measured at the center of the flat, when lead finish A is applied.
- Fourteen spaces.
- If this configuration is used, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.

Figure 1: Package outline and dimensions specified for 16-lead ceramic dual-in-line package (CERDIP).

FIGURE 2: Package Dimensions as Measured.

<u>Designation</u>	<u>Measured Value</u>
A	3.96 (0.156)
b	0.43 (0.017)
b <sub>1</sub>	1.52 (0.060)
c	0.25 (0.010)
D	19.0 (0.750)
E	6.30 (0.248)
E <sub>1</sub>	7.62 (0.300)
E <sub>2</sub>	- -
E <sub>3</sub>	- -
e	2.54 (0.100)
L	3.30 (0.130)
L <sub>1</sub>	4.06 (0.160)
Q	0.64 (0.025)
Q <sub>1</sub>	- -
S	0.64 (0.025)
S <sub>1</sub>	0.51 (0.020)
S <sub>2</sub>	1.52 (0.060)

NOTE: Values shown outside parentheses are in millimeters.  
Values within parentheses are in inches.

THIS PRACTICALLY INEVITABLY PRACTICABLE  
FOR THE FUTURE OF THE WORLD



FIGURE 3: Device as received, showing package markings.  
Magnification: 1.7X.

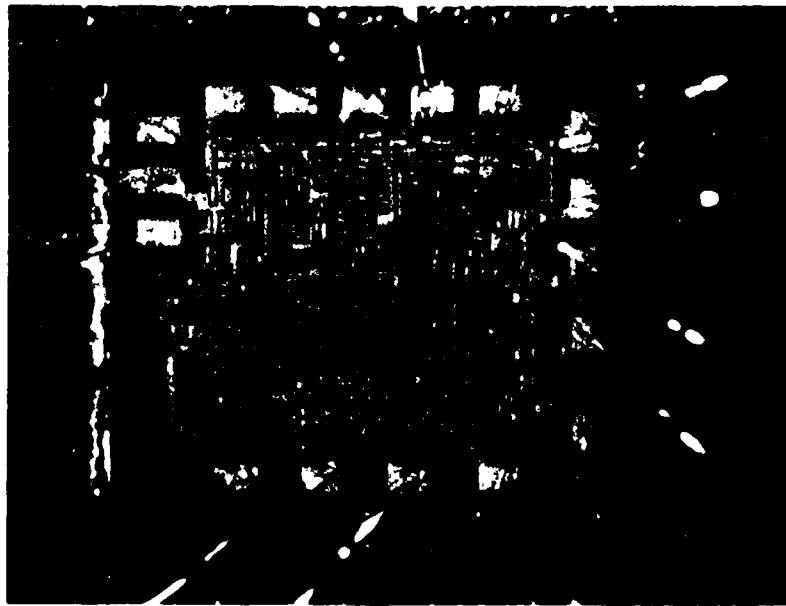


FIGURE 4: Overall view of chip and internal wires.  
Magnification: 43X.

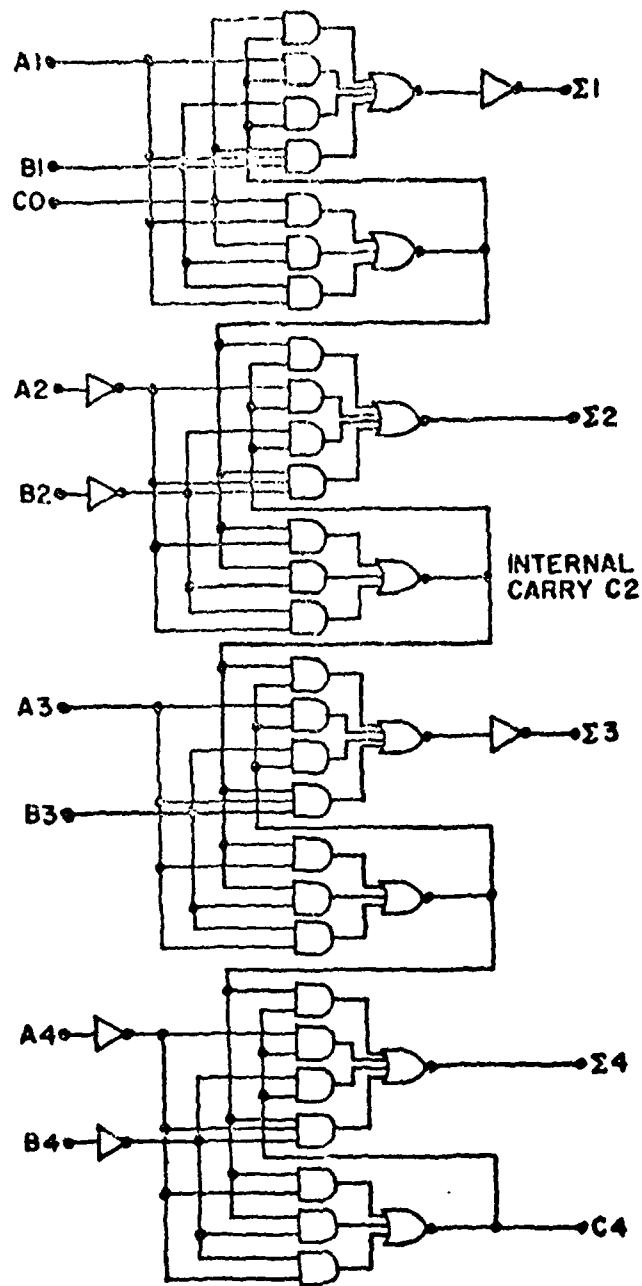


FIGURE 5: Logic diagram for the 54LS283.

THIS PAGE IS BEST QUALITY PRACTICABLE  
PRINTED IN INK ON PAPER TO DDC

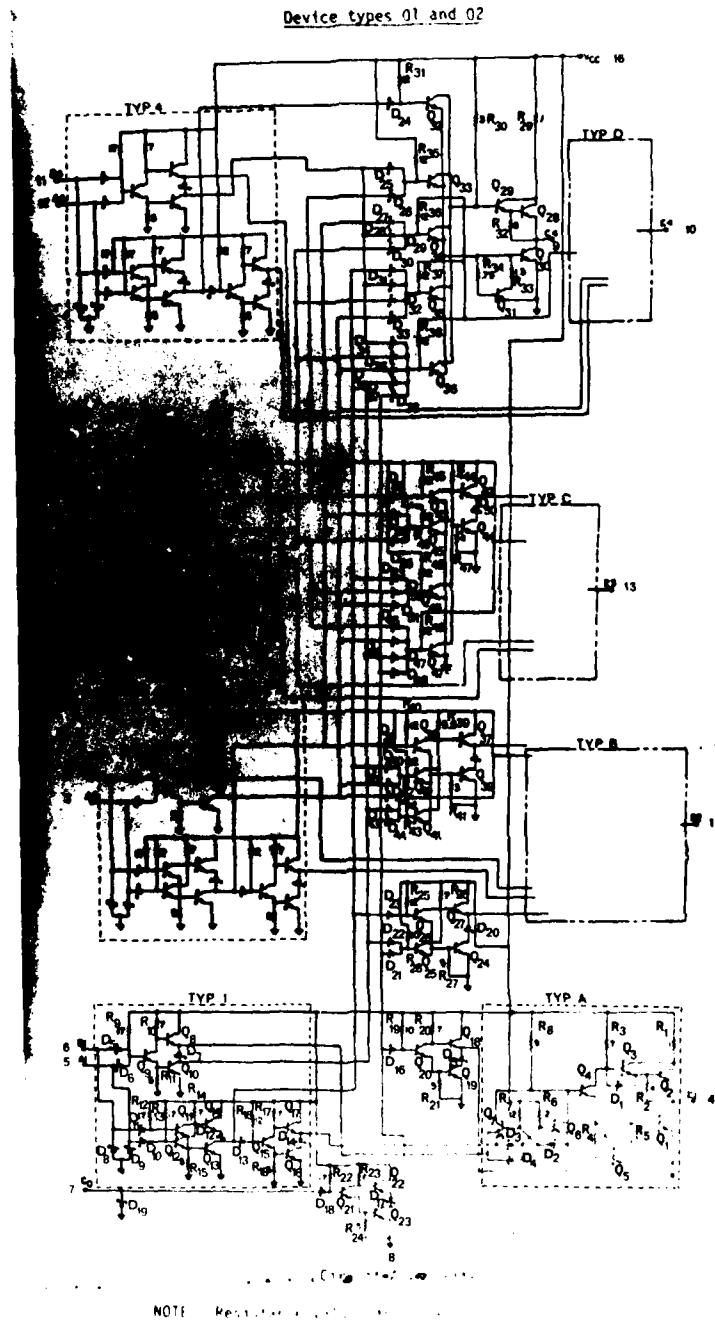


FIGURE 6: Detailed electrical schematic of the device.

THIS PAGE IS BEST QUALITY PRACTICABLE  
FROM COPY FROM 1000 TO 500

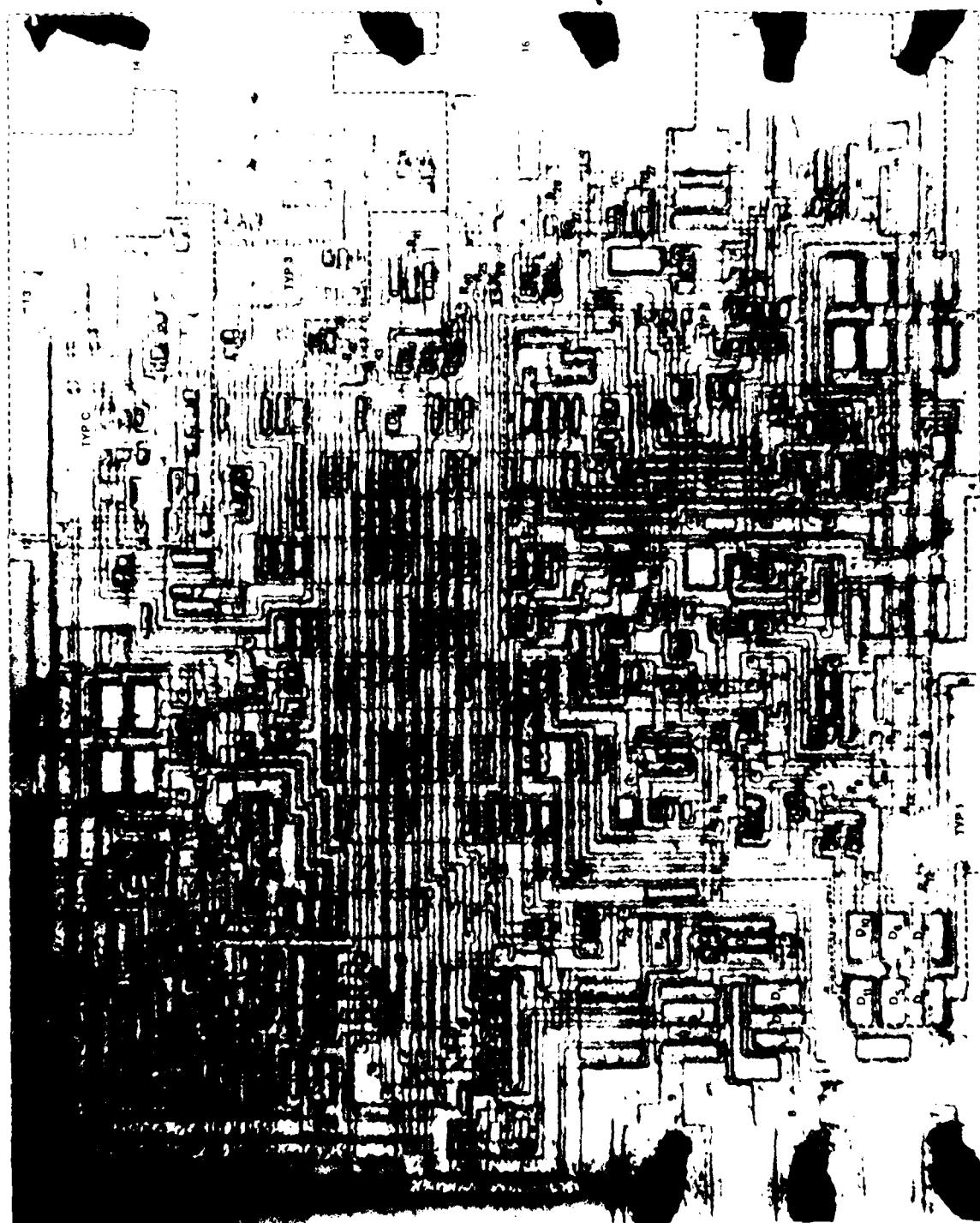


FIGURE 7: Overall view of chip, mapped with schematic symbols  
designations corresponding to those in Figure 6.  
Magnification: 80X. (inverted image)

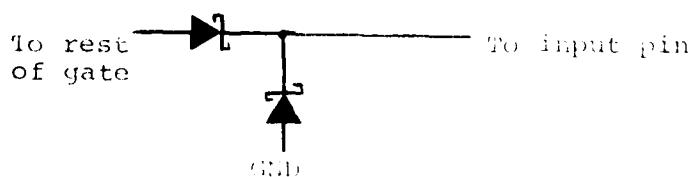
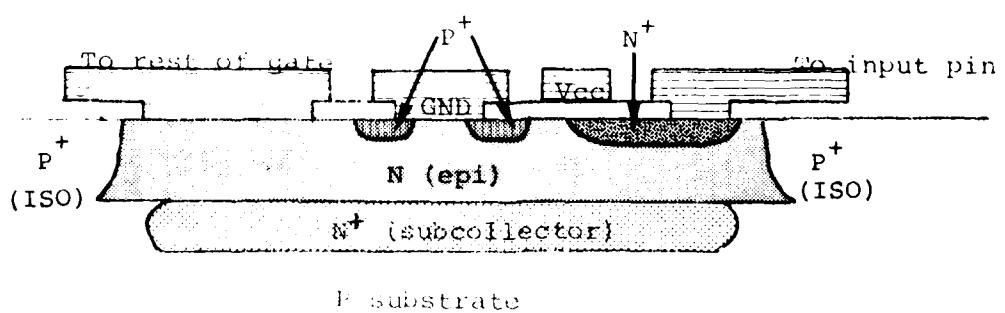
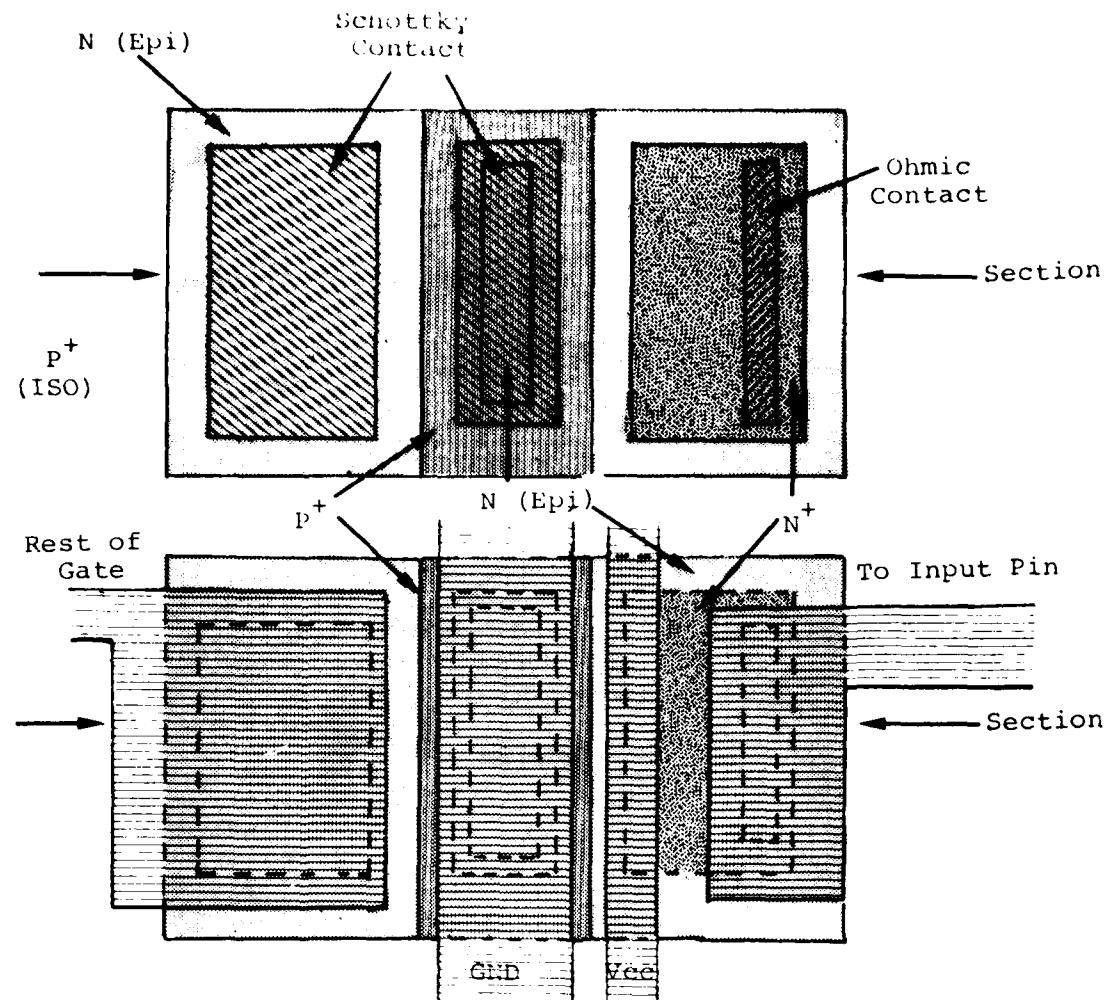
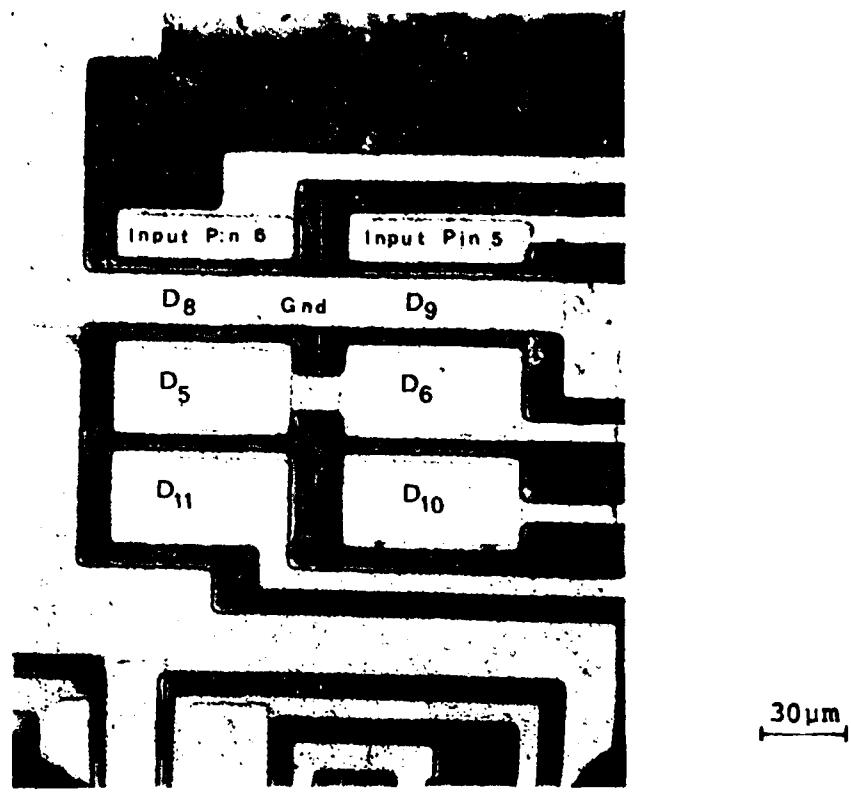


Figure 8. Schematic diagram showing cross-sectional view of input structure (not to scale).



**FIGURE 9:** Photomicrograph of input structure. Diode designations correspond to those in Figures 6 and 7.

## APPENDIX F

### CONSTRUCTION ANALYSIS OF VENDOR B 54LS283 STANDARD SCHOTTKY TTL INTEGRATED CIRCUIT IN CERAMIC DIP

#### Abstract

A Vendor B high speed 4-Bit binary full adder with internal carry lookahead was subjected to a detailed construction analysis. The device accepts two 4-Bit binary words and a carry input and generates the binary sum outputs and the carry output from the most significant bit. Device complexity is 36 equivalent gates, and low power Schottky technology is employed in the device fabrication.

Two devices were received packaged in standard 16-pin ceramic dual-in-line packages (CERDIP's) date coded 7741. The leads were tin plated Kovar; the internal wires were 1 mil aluminum, having better than adequate pull-strengths. The single level chip metallization was vapor deposited Al over sputtered Ti-W over  $Pt_xSi_y$ . The chip was entirely covered with vapor deposited PSG for scratch protection and passivation. The metallization everywhere appeared porous and in some places it had been severely damaged, apparently by a probe which had been dragged across the surface of the chip. No other weaknesses in construction or workmanship were noted.

#### Introduction

This analysis was performed as part of an evaluation of this device for Rome Air Development Center (RADC). The analysis was designed to document the construction details and materials used in these units and to identify shortcomings in the design or defects in workmanship, if any.

#### Results

##### The Package

The units were packaged in 16-lead ceramic dual-in-line packages (CERDIP). Both lid and base were of smooth alumina, with a fritted glass seal. The leads were embedded in the seal and

consisted of tin plated Kovar. The thickness of the tin plating was measured to be  $8.8 \mu\text{m}$  ( $350 \mu\text{inches}$ ). The package dimensions were found to be within the limits specified in MIL-M-38510D and are shown in Figure 2; the case outline drawing and specification for dimensions are shown in Figure 1. The package markings were as shown in Figure 3.

The internal area of the lead frame which is used for bonding pads for the aluminum wires was clad with aluminum. This is rolled on prior to assembly of the package, and was measured to be  $6.3$  to  $8.2 \mu\text{m}$  ( $248$  to  $323 \mu\text{inches}$ ) thick.

#### The Chip

The lid was removed by applying a mechanical stress to it and forcing a chisel edge into the seal in a controlled manner until the seal fractured. An overall view of the chip is shown in Figure 4. The chip was measured to be  $1.42 \times 1.50 \times 0.20 \text{mm}^3$  ( $55.9 \times 59.1 \times 7.9 \text{ mils}$ ). The volume of the cavity was  $0.021 \text{ cm}^3$ , including the recess in the package lid. The chip was mounted using a silicon-gold eutectic approximately  $3.2$  to  $6.3 \mu\text{m}$  ( $0.126$  to  $0.248 \text{ mils}$ ) thick with a thick film gold paste providing the gold. This thick film gold paste also contains minute glass particles which are fired into the ceramic at  $920^\circ\text{C}$ , thus providing the adhesion to the ceramic substrate. Away from the chip the gold metallization which lined the bottom of the cavity was measured to be from  $3.8$  to  $7.6 \mu\text{m}$  ( $0.154$  to  $0.30 \text{ mils}$ ) thick. Thermal resistances were measured to be  $\theta_{\text{junction-to-air}} = 122.1^\circ\text{C/W}$  and  $\theta_{\text{junction-to-case}} = 19.4^\circ\text{C/W}$ .

The internal wires were ultrasonically bonded, 1 mil diameter aluminum. Microbond-pull testing of 8 of the 16 wires yielded a range in pull strength from 3.0 to 4.0 grams-force, with an average of 3.8. These wires exceed the minimum pull-strength of 1.5 gm-f specified in MIL-STD-883B, Method 2011.2. No bond defects were noted.

The chip metallization was a single level interconnection scheme which used aluminum  $1.9 \mu\text{m}$  ( $76 \mu\text{inches}$ ) thick over Ti-W approximately  $4000 \text{ \AA}$  thick. The presence of the Ti-W layer provides good adhesion to the Si and  $\text{SiO}_2$  and is a diffusion barrier to the aluminum. The platinum-silicide in the contact areas gives good ohmic contact for base (P) and emitter (N+) diffusions and Schottky barrier contacts for collector diffusions (N). The above thicknesses were measured in an angle cross-section. The aluminum layer was vapor deposited and the Ti-W was sputter deposited in an undisclosed ratio. The  $\text{Pt}_x\text{Si}_y$  is formed by sputtering on Pt in a very thin layer and sintering to form  $\text{Pt}_x\text{Si}$  in the contact areas, followed by blanket etching to remove the Pt elsewhere. A PSG layer about  $1.9 \mu\text{m}$  ( $76 \mu\text{inches}$ ) thick covered the entire chip as passivation and protection against scratching during handling.

The highest current density was found to exist in the metallization run between the collector of Q33 and R30. Here the current is 1.47mA maximum and the smallest metallization width is  $7.8 \times 10^{-4}$  cm. The metallization thickness of  $1.9 \times 10^{-4}$  cm results in a minimum cross-sectional area of  $1.48 \times 10^{-7}$  cm<sup>2</sup> which yields a maximum current density of  $9.9 \times 10^3$  A/cm<sup>2</sup>. Over an oxide step the current density could reach  $1.5 \times 10^4$  A/cm<sup>2</sup>, since the metallization thins to about 2/3 its thickness as it goes over an oxide step. This is within the specification of  $5 \times 10^5$  A/cm<sup>2</sup> found in MIL-M-38510 as a maximum current density for Al to avoid an unacceptable level of electromigration failures by a factor of 13.3.

The chip was photographed and mapped to identify all the components. Figure 5 shows the logic layout of the device as related to the external pin connections and Figure 6 shows a detailed schematic of the device. Figure 7 shows the chip with all of the components labelled with the schematic symbol designations corresponding to those given in Figure 6.

Visual inspection of the chip was performed using Method 2010.3 of MIL-STD-883B as a guide, and some workmanship weaknesses which pose potential reliability problems were noted. The metallization everywhere appeared porous, and in some places it was severely damaged. It appeared that a probe had been dragged across the chip surface resulting scarring and smearing of metallization. This substantially reduces device reliability, as it can result in an unacceptable level of electromigration (due to increased current densities), or in short or open circuits. A photograph showing some of this metallization damage appears in Figure 8. Other than these workmanship weaknesses, no faults were found in the construction of the device.

#### The Components

The substrate was P-type. Subcollectors approximately  $13.6 \mu\text{m}$  (.53 mils) deep, consisting of low resistivity N-type diffusions, were made in positions corresponding to the transistors prior to the growth of the epitaxial layer. These provided high conductivity paths from the vicinity of the base-collector junctions to the collector contact diffusions. An N-type epitaxy about  $4.1 \mu\text{m}$  (.16 mils) thick was then grown.

After the growth of the epitaxial layer, P-type isolation diffusions approximately  $4.8\mu m$  (0.19 mils) deep were made, partitioning the epitaxial layer into individual collector regions and other components. The P-type base diffusion followed and the resistors were also made at this time. This diffusion was measured to be about  $1.1\mu m$  ( $44\mu$  inches) deep. This also created the p-n junction guard rings for the input clamping diode to be discussed later. The N<sup>+</sup> type diffusion, measured to be about  $0.6\mu m$  ( $24\mu$  inches) deep, then created the emitters and the collector contact enhancement regions. This latter was necessary to achieve ohmic contact to the low-doped epitaxial layer.

#### The Transistors

With the exception of Q<sub>2</sub>, Q<sub>8</sub>, Q<sub>14</sub>, Q<sub>17</sub>, Q<sub>18</sub>, Q<sub>22</sub>, Q<sub>27</sub>, and Q<sub>28</sub>, all transistors utilized the Schottky design. The base regions of these Schottky transistors were annular, having a rectangular "hole" within a rectangular shaped diffusion. Hence a portion of the epitaxial region at the surface was surrounded by this annular ring. The contact hole in the base oxide exposed both part of the base region and all of the epitaxial region which was surrounded by the base ring. This latter was part of the collector. When the metallization was deposited within the contact hole, it created the ohmic contact to the base region and also created the Schottky diode between base and collector. This occurred because of the relative doping level of the base region (high doping yields ohmic contact) versus that of the epitaxial (collector) region (low doping yields rectifying Schottky contact). The eight transistors mentioned above as exceptions from this design were standard bipolar construction.

#### The Diodes

Each input had a Schottky barrier diode to ground to provide protection for the input against negative voltage spikes. The construction was quite similar to that in the transistors, forming what was actually a p-n junction - Schottky barrier hybrid diode. A cross-sectional diagram (not to scale) of the construction of the input structure is shown in Figure 9, with a top view shown in Figure 10. References 1 and 2 describe the theory and advantages of such a structure.

#### The Resistors

P-type base diffusion was used for all of the resistors. This diffusion had a resistivity of about  $1000\Omega/\square$ . This sheet resistance was obtained by counting squares and comparing

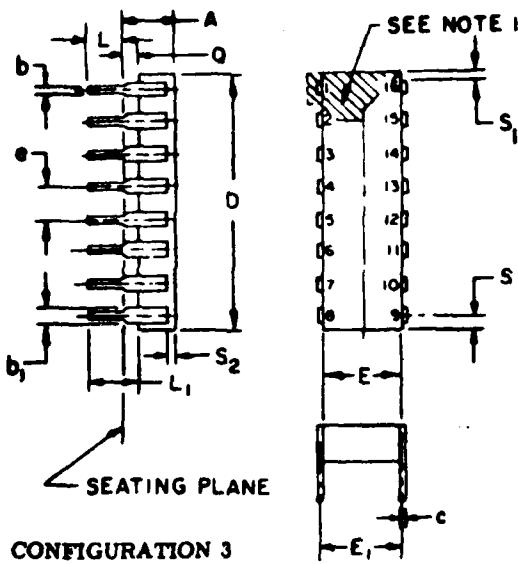
to values shown in the electrical schematic in Figure 6.  
The diffusion depth was measured to be about  $1.1\mu\text{m}$  ( $44\mu\text{inches}$ ).

#### Conclusions

The construction and workmanship of this device appear to be sound and in keeping with military specification with the exception that flaws in the metallization existed, as noted above. The metallization appeared porous everywhere and was damaged, apparently by a probe, in places. Other than these defects, no weaknesses in construction or workmanship were noted.

#### References

1. RADC-TR-76-292, Reliability Evaluation of Schottky Barrier Diode Microcircuits, Raytheon Company, Sept. 1976, Appendix B, p. 158.
2. R.A. Zettler and A.M. Cowley, "p-n Junction-Schottky Barrier Hybrid Diode" IEEE Transactions on E.D., Vol. ED-16, no. 1, January 1969.



CONFIGURATION 3

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		200		5.08	
b <sub>1</sub>	.014	.023	.36	.58	8
b <sub>2</sub>	.030	.070	.76	1.78	2, 8
c	.008	.015	.20	.38	8
D	.840			21.34	4
E	.220	.310	5.59	7.87	4
E <sub>1</sub>	.290	.320	7.37	8.13	7
E <sub>2</sub>	.100		2.54		
E <sub>3</sub>	.050		1.27		
F	.100 BSC		2.54 BSC		5, 9
L	.125	.200	3.18	5.08	
L <sub>1</sub>	.150		3.81		
Q	.015	.060	.38	1.02	3
Q <sub>1</sub>	.020		.51		
S		.080		2.03	8
S <sub>1</sub>	.005		.13		6
S <sub>2</sub>	.005		.13		
α	0°	15°	0°	15°	

NOTES:

- Index area; a notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
- The minimum limit for dimension b<sub>1</sub> may be .020 (.51 mm) for leads number 1, 8, 9 and 16 only.
- Dimension Q shall be measured from the seating plane to the base plane.
- This dimension allows for off-center lid, meniscus and glass overrun.
- The basic pin spacing is .100 (2.54 mm) between centerlines. Each pin centerline shall be located within ±.010 (.25 mm) of its exact longitudinal position relative to pins 1 and 16.
- Applies to all four corners (leads number 1, 8, 9, and 16), and 40.5 shall apply.
- Lead center when α is 0°. E<sub>1</sub> shall be measured at the centerline of the leads (see 40.4 of this appendix).
- All leads - Increase maximum limit by .003 (.08 mm) measured at the center of the flat, when lead finish A is applied.
- Fourteen spaces.
- If this configuration is used, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.

Figure 1: Package outline and dimensions specified for 16-lead ceramic dual-in-line package (CERDIP).

Figure 2: Package Dimensions

<u>Designation</u>	<u>Measured Value</u>
A	4.14 (.163)
b	0.46 (.018)
b <sub>1</sub>	1.52 (.060)
c	0.25 (.010)
D	19.6 (.770)
E	6.32 (.249)
E <sub>1</sub>	7.37 (.290)
E <sub>2</sub>	- -
E <sub>3</sub>	- -
e	2.54 (.100)
L	0.36 (.014)
L <sub>1</sub>	0.41 (.016)
Q	0.51 (.020)
Q <sub>1</sub>	- -
S	0.76 (.030)
S <sub>1</sub>	0.38 (.015)
S <sub>2</sub>	1.52 (.060)

Note: Values shown outside parentheses are in millimeters; values within parentheses are in inches.

AD-AB82 926

RAYTHEON CO BEDFORD MA MISSILE SYSTEMS DIV

F/8 9/5

RELIABILITY EVALUATION OF LOW POWER SCHOTTKY CLAMPED MICROCIRCUIT--ETC(U)

FEB 80 K B LASCH, D BARTELS, J J SPINALE

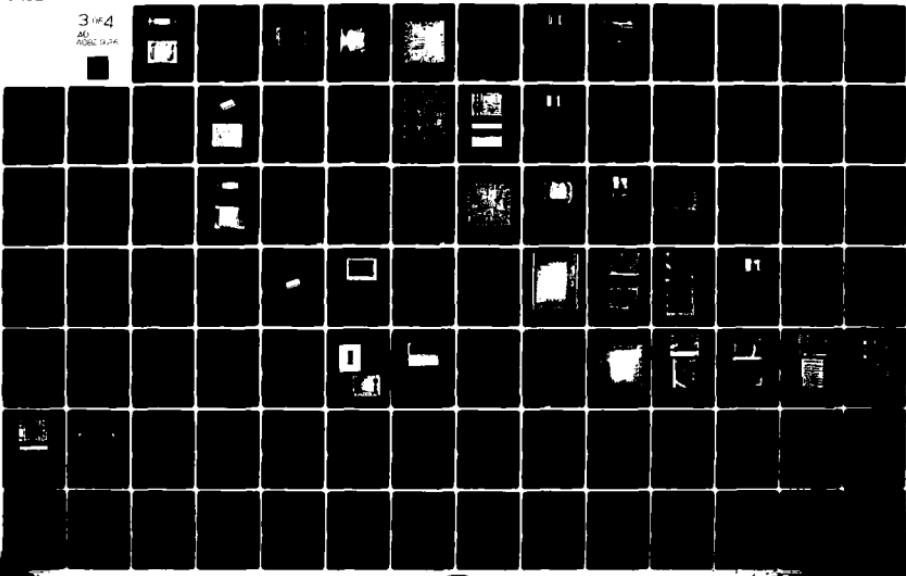
F30602-77-C-0186

ML

RADC-TR-80-5

UNCLASSIFIED

3164  
ML  
FEB 80-26



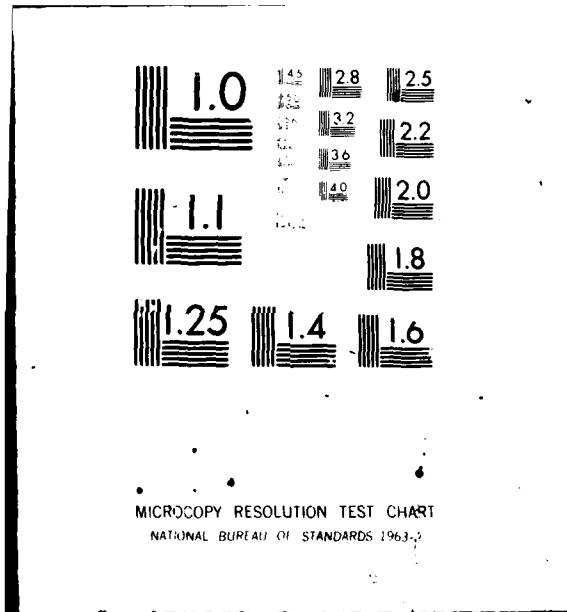




FIGURE 3: Device as received, showing package markings.  
Magnification: 3X.

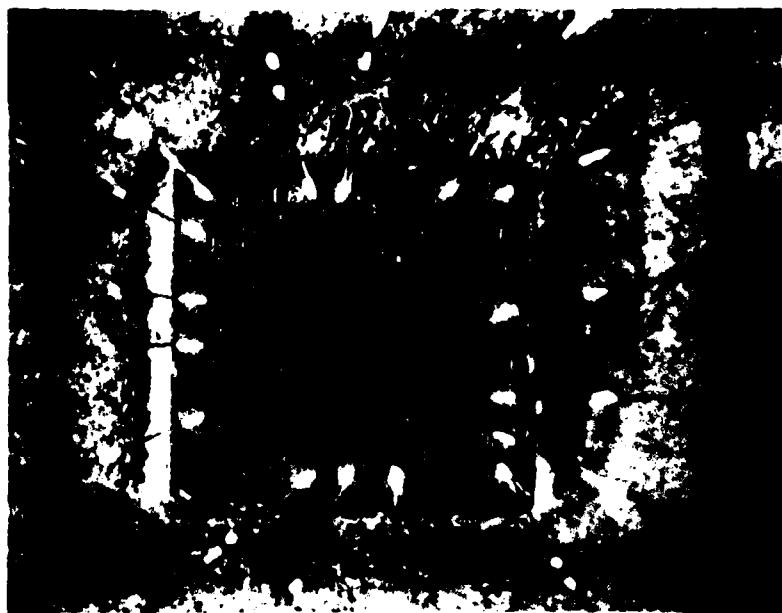
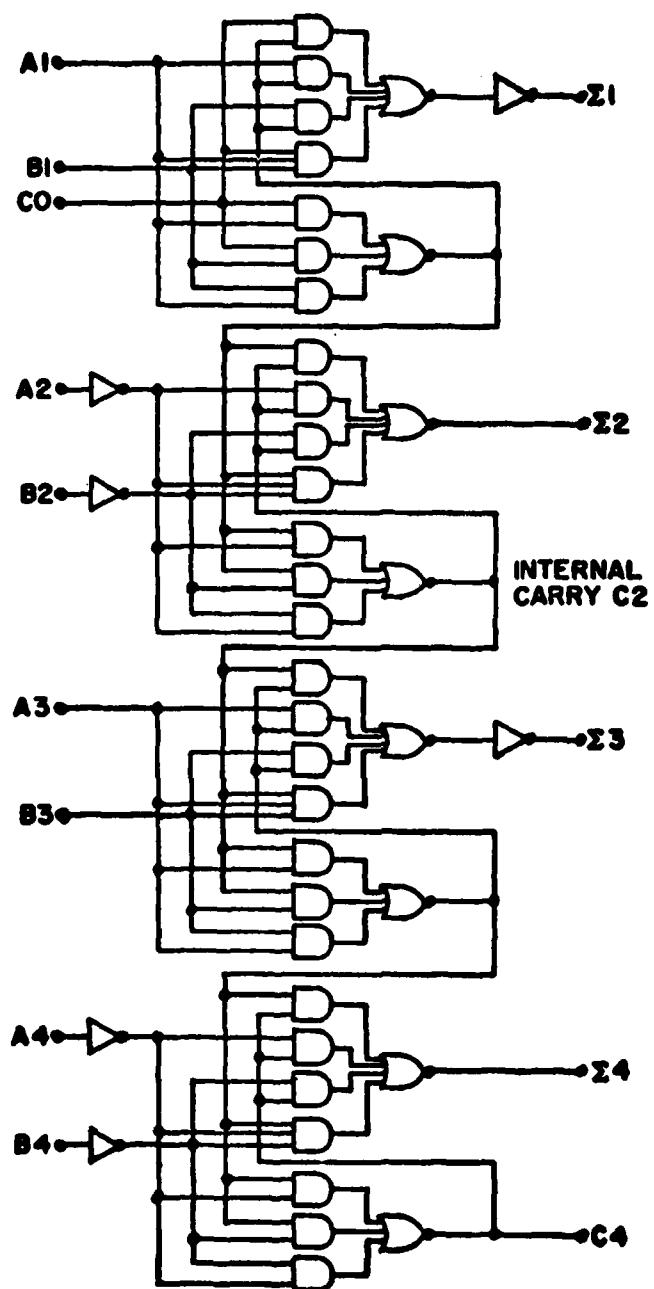


FIGURE 4: Overall view of internal package layout, showing  
chip and internal wires. Magnification: 35X.

THIS PAGE IS REPRODUCIBLE PRACTICABLE  
FROM COPY FURNISHED TO DDC

F-8



**FIGURE 5(a): Logic diagram for the 54LS283.**

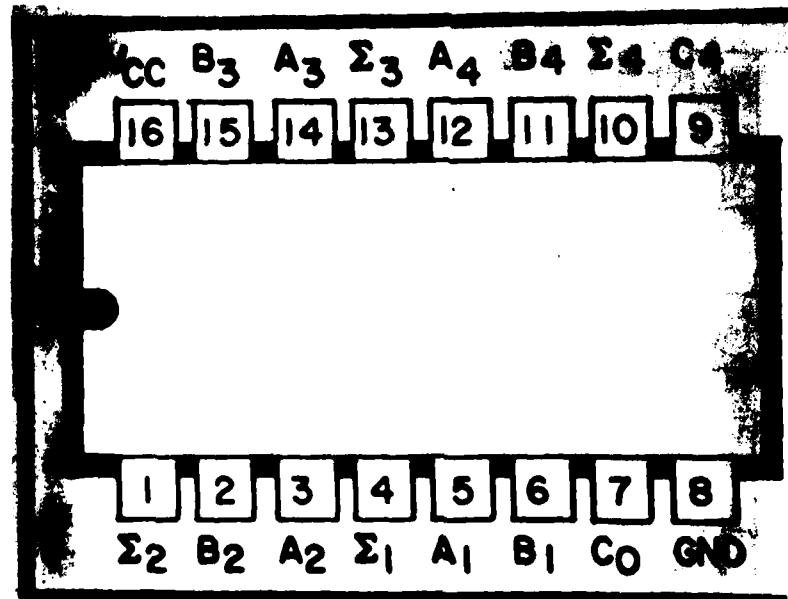


FIGURE 5(b): Package pin-out of device.

THIS PAGE IS BEST QUALITY PRACTICABLE  
FROM COPY FURNISHED TO DDC

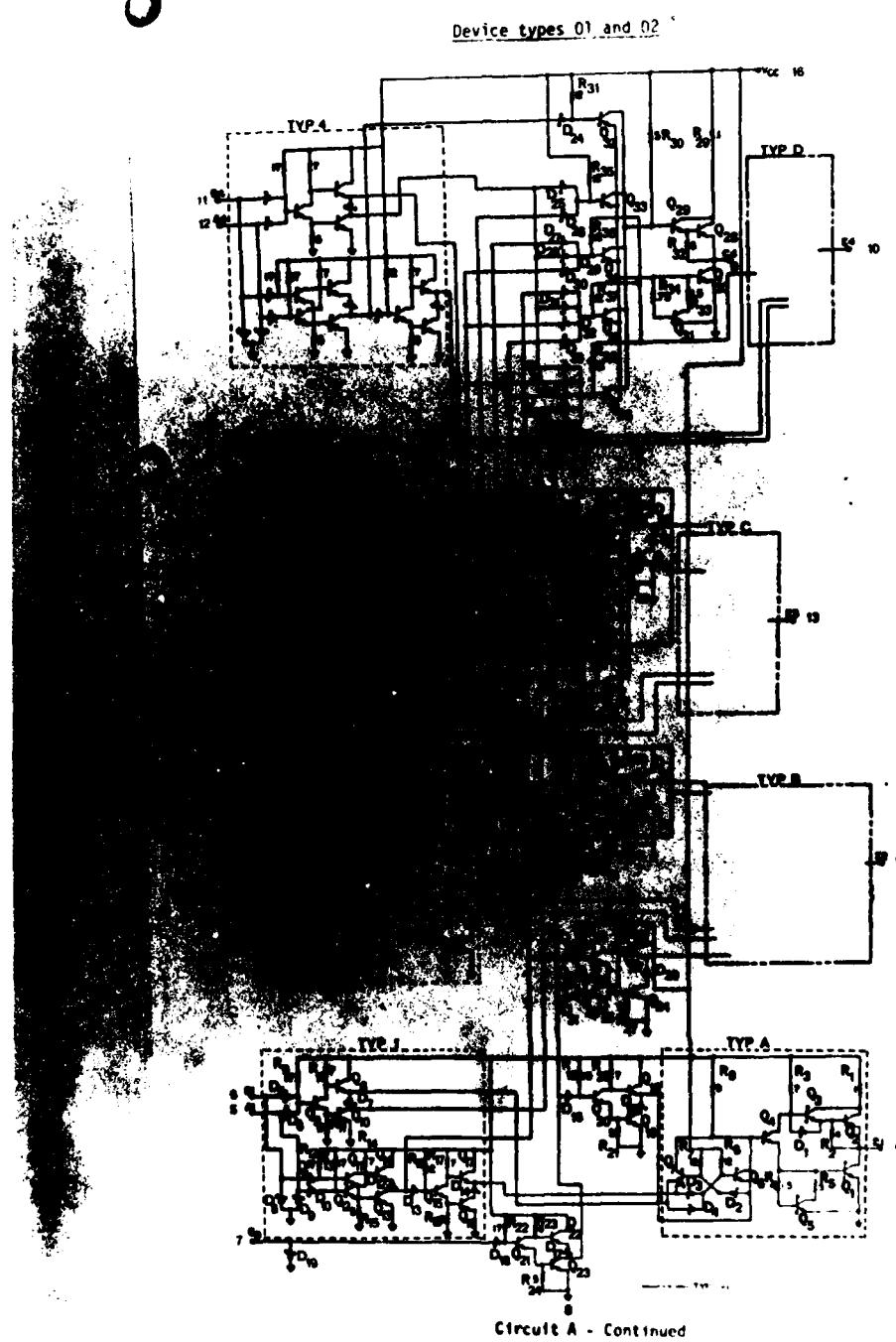


FIGURE 6: Detailed electrical schematic of device.

THIS PAGE IS BEST QUALITY PRACTICABLE  
FROM COPY FURNISHED TO DDC

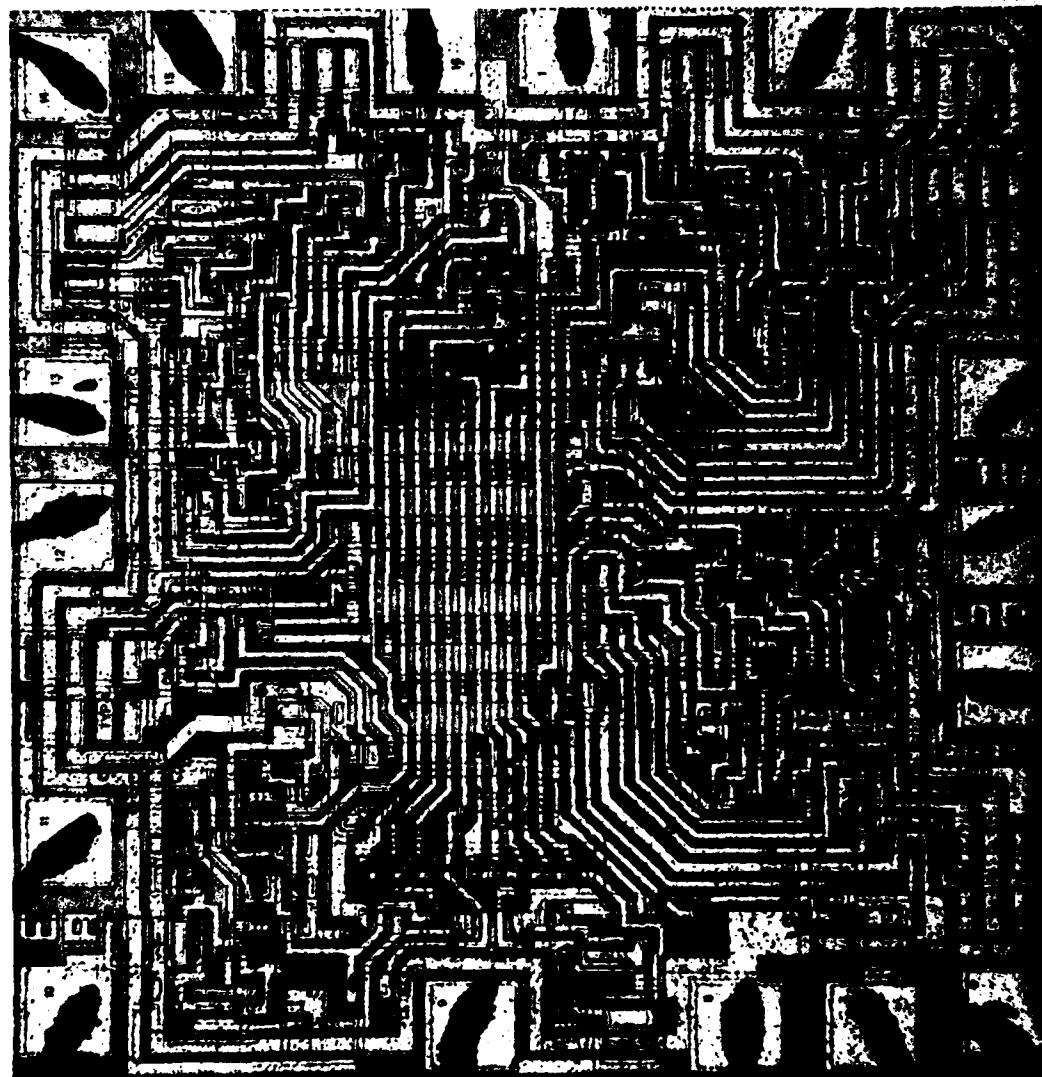
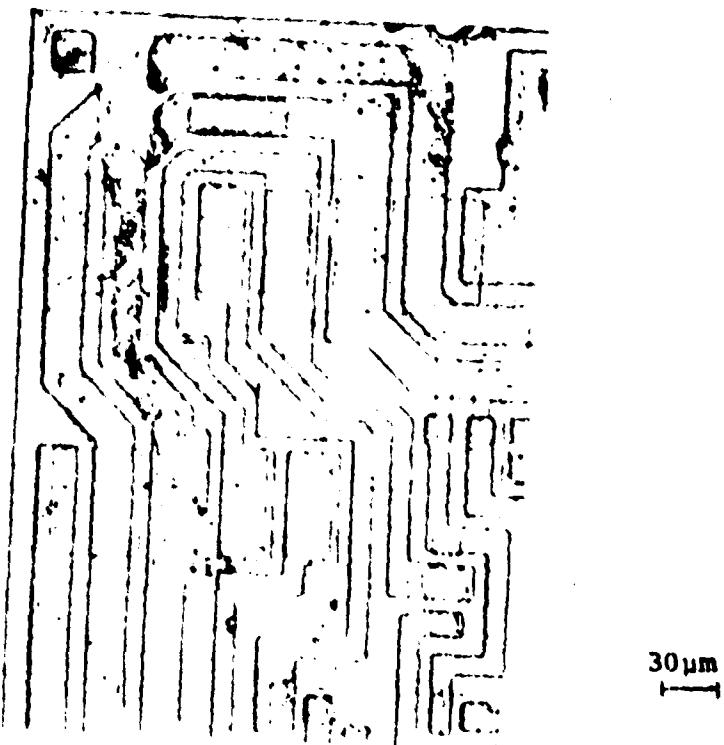
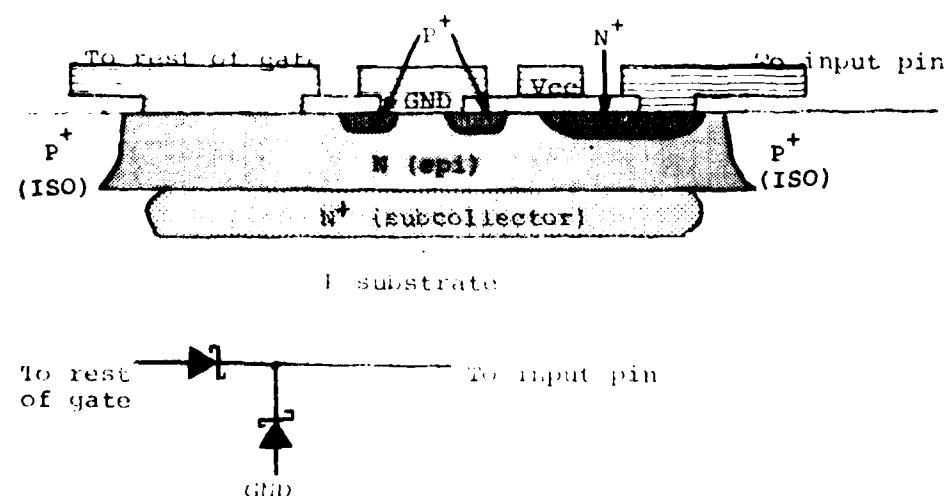
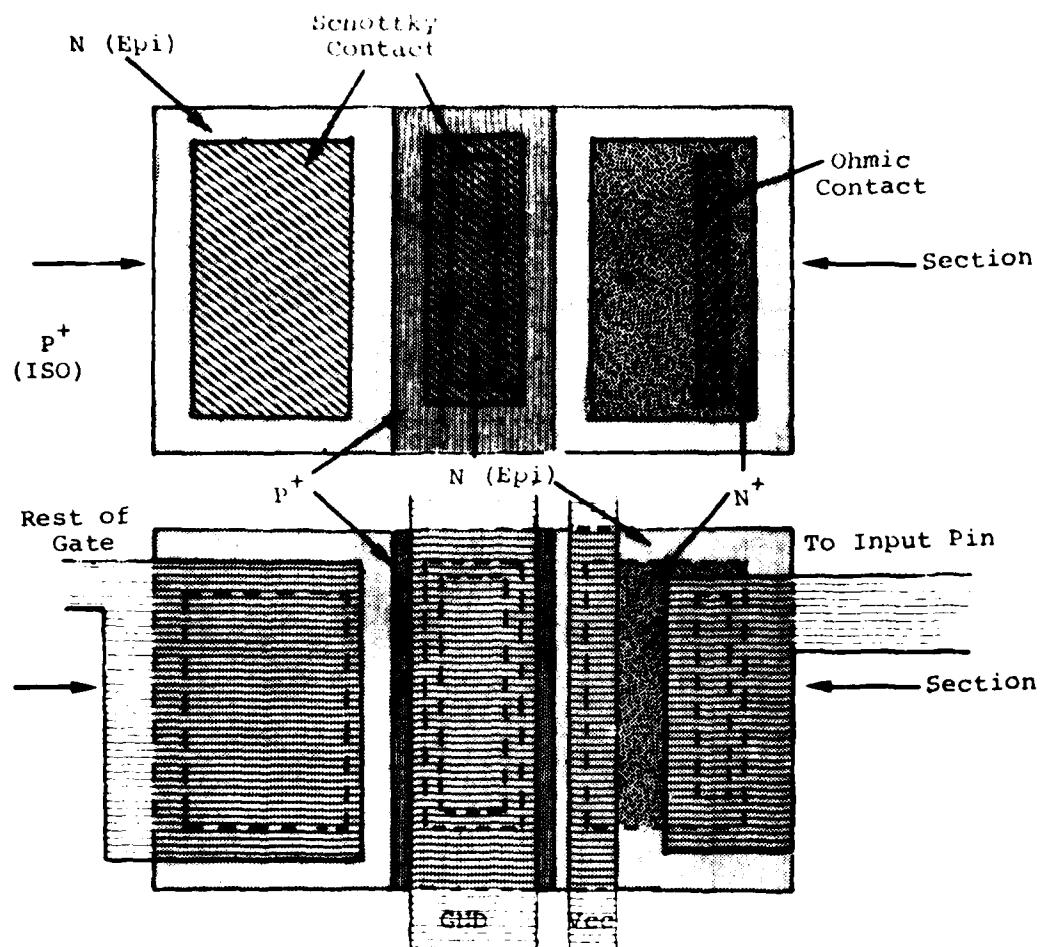


FIGURE 7: Overall view of chip, mapped with schematic symbol designations corresponding to those shown in Figure 6. Magnification: 100X. (reversed image).

THIS PAGE IS BEST QUALITY PRACTICABLE  
FROM COPY FURNISHED TO DDC



**FIGURE 8:** Photomicrograph showing metallization damage apparently caused by probes dragging across chip surface.



**FIGURE 9:** Schematic diagram showing cross-sectional view of input structure (not to scale).

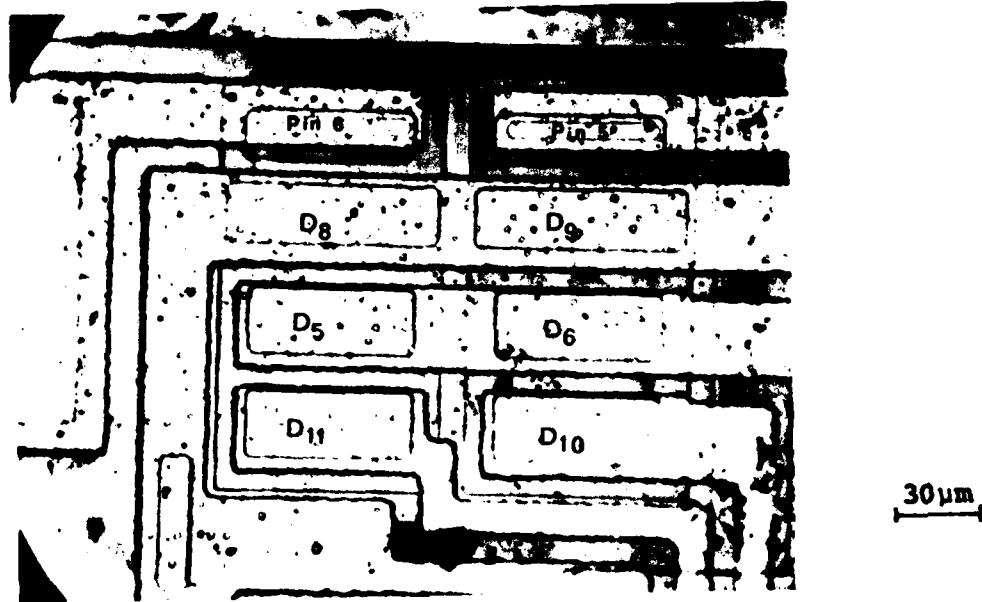


FIGURE 10: Photomicrograph of input structure.

## APPENDIX G

### CONSTRUCTION ANALYSIS OF VENDOR A 54LS191

#### STANDARD SCHOTTKY TTL INTEGRATED CIRCUIT IN CERAMIC DIP

##### Abstract

A Vendor A synchronous 4-bit binary up/down counter was subjected to a detailed construction analysis. State changes of the counter are synchronous with the low to high transition of the clock pulse input. The device complexity is 58 equivalent gates, and low power Schottky technology is employed in the device fabrication.

Two devices were received packaged in standard 16-pin ceramic dual-in-line packages (CERDIP's) date coded 7737. The leads were tin plated Kovar; the internal wires were 1 mil aluminum, having better than adequate pull-strengths. The single level chip metallization was vapor deposited Al over sputtered Ti-W over Pt<sub>x</sub>Si<sub>y</sub> in the contact areas. The chip is entirely covered with vapor deposited PSG for scratch protection and passivation. Two weaknesses in construction were noted. Numerous oxide defects were present in the passivation layer, and voids were present in the die attach area under one edge of one of the chips.

No other weaknesses in construction or workmanship were noted.

##### Introduction

This analysis was performed as part of an evaluation of this device for Rome Air Development Center (RADC). The analysis was designed to document the construction details and materials used in these units and to identify shortcomings in the design or defects in workmanship, if any.

##### Results

###### The Package

The units were packaged in 16-lead ceramic dual-in-line packages (CERDIP). Both lid and base were of smooth alumina, with a fritted glass seal. The leads were embedded in the seal and consisted

of tin plated Kovar. The thickness of the tin plating was measured to be 3.8-5.1  $\mu\text{m}$  (150-200  $\mu\text{inches}$ ). The package dimensions were found to be within the limits specified in MIL-M-38510D and are shown in Figure 2; the case outline drawing and specification for dimensions are shown in Figure 1. The package markings were as shown in Figure 3.

The internal area of the lead frame which is used for bonding pads for the aluminum wires was clad with aluminum. This is rolled on prior to assembly of the package, and was measured to be 3.6  $\mu\text{m}$  (142  $\mu\text{inches}$ ) thick.

#### The Chip

The lid was removed by applying a mechanical stress to it and forcing a chisel edge into the seal in a controlled manner until the seal fractured. An overall view of the chip is shown in Figure 4. The chip was measured to be 1.96 x 2.58 x 0.19 mm (77.2 x 101.6 x 7.7 mils). The volume of the cavity was 0.034  $\text{cm}^3$  including the recess in the package lid. The chip was mounted using a silicon-gold eutectic approximately 24  $\mu\text{m}$  (0.94 mils) thick with a thick film gold paste providing the gold. This thick film gold paste also contains minute glass particles which are fired into the ceramic at 920°C, thus providing the adhesion to the ceramic substrate. Away from the chip the gold metallization which lined the bottom of the cavity was measured to be 16  $\mu\text{m}$  (0.63 mils) thick. Thermal resistances were measured to be  $\theta_{\text{junction-to-air}} = 113.8^\circ\text{C/W}$  and  $\theta_{\text{junction-to-case}} = 12.8^\circ\text{C/W}$ .

The internal wires were ultrasonically bonded, 1 mil diameter aluminum. Microbond-pull testing of 8 of the 16 wires yielded a range in pull strength from 3.0 to 6.0 grams-force, with an average of 4.1. These wires exceed the minimum pull-strength of 1.5 gm-f specified in MIL-STD-883B, Method 2011.2. No bond defects were noted.

The chip metallization was a single level interconnection scheme which used aluminum 1.6  $\mu\text{m}$  (63  $\mu\text{inches}$ ) thick over Ti-W approximately 3,000 Å thick. The presence of the Ti-W layer provides good adhesion to the Si and  $\text{SiO}_2$  and is a diffusion barrier to the aluminum. The platinum-silicide in the contact areas gives good contact for base (P) and emitter (N<sub>+</sub>) diffusions and Schottky barrier contacts for collectors (N). The above thicknesses were measured in an angle cross-section. The aluminum layer was vapor deposited and the Ti-W was sputter deposited in an undisclosed ratio. The Pt<sub>x</sub>Si<sub>y</sub> is formed by sputtering on Pt in a very thin layer and sintering to form Pt<sub>x</sub>Si<sub>y</sub> in the contact areas, followed by blanket etching to remove the Pt<sub>x</sub> elsewhere. A phosphosilicate glass layer about 1.6  $\mu\text{m}$  (63  $\mu\text{inches}$ ) thick covered the entire chip as passivation and protection against scratching during handling.

The highest current density was found to exist in the ground metallization run. Here the current is 4.8mA maximum and the smallest metallization width is  $2 \times 10^{-3}$  cm. The metallization thickness of  $1.6 \times 10^{-4}$  cm results in a minimum cross-sectional area of  $3.2 \times 10^{-7}$  cm $^2$  which yields a maximum current density of  $1.5 \times 10^4$  A/cm $^2$ . Over an oxide step the current density could reach  $2.3 \times 10^4$  A/cm $^2$ , since the metallization thins to about 2/3 its thickness as it goes over an oxide step. This is within the specification of  $5 \times 10^5$  A/cm $^2$  found in MIL-M-38510 as a maximum current density for Al to avoid an unacceptable level of electro-migration failures.

The chip was photographed and mapped to identify all the components. Figure 5 shows the logic layout of the device as related to the external pin connections and Figure 6 shows a detailed schematic of the device. Figure 7 shows the chip with all of the components labelled with the schematic symbol designations corresponding to those given in Figure 6.

Visual inspection of the chip was performed using Method 2010.3 of MIL-STD-883B as a guide. Several oxide defects were noticed, and an aluminum etch was used to accentuate those which occurred over metallization. Figure 8 is a photomicrograph of some such defects.

When one of the units was cross-sectioned, voids were found under one edge of the chip. A photomicrograph of these voids is shown in Figure 9. Radiographic examination of the die attach area revealed that the voids extended only a very short distance under the chip. Examination of the void area using x-ray energy spectroscopy (XES) revealed no contaminants. Based on these findings it is believed that the voids noted do not present a reliability hazard in this unit, but that they do indicate the potential for one if they become more extensive in other units.

#### The Components

The substrate was P-type. Subcollectors approximately 8.9  $\mu$ m (.35 mils) deep, consisting of low resistivity N-type diffusions, were made in positions corresponding to the transistors prior to the growth of the epitaxial layer. These provided high conductivity paths from the vicinity of the base-collector junctions to the collector contact diffusions. An N-type epitaxy about 3.6  $\mu$ m (.14 mils) thick was then grown.

After the growth of the epitaxial layer, P-type isolation diffusions approximately 4.4  $\mu$ m (.17 mils) deep were made, partitioning the epitaxial layer into individual collector regions and other com-

ponents. The P-type base diffusion followed and the resistors were also made at this time. This diffusion was measured to be about  $1.4 \mu\text{m}$  (55 micches) deep. This also created the p-n junction guard rings for the input clamping diode to be discussed later. The N type diffusion, measured to be about  $0.8 \mu\text{m}$  (31 micches) deep, then created the emitters and the collector contact enhancement regions. This latter was necessary to achieve ohmic contact to the low-doped epitaxial layer.

#### The Transistors

With the exception of  $Q_2$ ,  $Q_8$ ,  $Q_{21}$ ,  $Q_{35}$ ,  $Q_{49}$  and  $Q_{63}$ , all transistors utilized the Schottky design. The base regions of these Schottky transistors were annular, having a rectangular "hole" within a rectangular shaped diffusion. Hence a portion of the epitaxial region at the surface was surrounded by this annular ring. The contact hole in the base oxide exposed both part of the base region and all of the epitaxial region which was surrounded by the base ring. This latter was part of the collector. When the metallization was deposited within the contact hole, it created the ohmic contact to the base region and also created the Schottky diode between base and collector. This occurred because of the relative doping level of the base region (high doping yields ohmic contact) versus that of the epitaxial (collector) region (low doping yields rectifying Schottky contact). The six transistors mentioned above as exceptions from this design were standard bipolar construction.

#### The Diodes

Each input had a Schottky barrier diode to ground to provide protection for the input against negative voltage spikes. The construction was quite similar to that in the transistors, forming what was actually a p-n junction - Schottky barrier hybrid diode. A cross-sectional diagram (not to scale) of the construction of the input structure is shown in Figure 10, with a top view shown in Figure 11. References 1 and 2 describe the theory and advantages of such a structure.

#### The Resistors

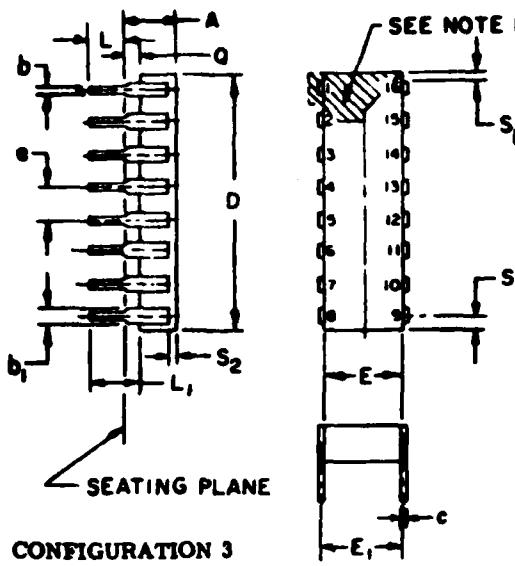
P-type base diffusion was used for all of the resistors. This diffusion had a resistivity of about  $1,000\Omega/\mu\text{m}$ . This sheet resistance was obtained by counting squares and comparing to values shown in the electrical schematic in Figure 6. The diffusion depth was measured to be about  $1.4 \mu\text{m}$  (55 micches).

### Conclusions and Recommendations

In performing a construction analysis of Vendor A's 54LS191, two areas of potential reliability hazards were identified. The first was that oxide defects were present. It is recommended that the vendor's pre-cap visual inspection procedures be reviewed. Also noticed were voids in the die attach area under one edge of one of the chips. It is recommended that a sample of chip attach areas be x-rayed in order to determine the extent of the problem. Other than those defects, no weaknesses in construction or workmanship were noted.

### References

1. RADC-TR-76-292, Reliability Evaluation of Schottky Barrier Diode Microcircuits, Raytheon Company, Sept. 1976, Appendix B, p. 158.
2. R.A. Zettler and A.M. Cowley, "p-n Junction-Schottky Barrier Hybrid Diode" IEEE Transactions on E.D., Vol. ED-16, No. 1, January 1969.



CONFIGURATION 3

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		.200		5.08	
b	.014	.023	.36	.58	8
b <sub>1</sub>	.030	.070	.76	1.78	2, 8
c	.008	.015	.20	.38	8
D		.840		21.34	4
E	.220	.310	5.59	7.87	4
E <sub>1</sub>	.290	.320	7.37	8.13	7
E <sub>2</sub>	.100		2.54		
E <sub>3</sub>	.050		1.27		
e	.100 BSC		2.54 BSC		5, 9
L	.125	.200	3.18	5.08	
L <sub>1</sub>	.150		3.81		
Q	.015	.060	.38	1.32	3
Q <sub>1</sub>	.020		.51		
S		.080		2.03	8
S <sub>1</sub>	.005		.13		8
S <sub>2</sub>	.005		.13		
θ	0°	15°	0°	15°	

NOTES:

- Index area; a notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
- The minimum limit for dimension b<sub>1</sub> may be .020 (.51 mm) for leads number 1, 8, 9 and 16 only.
- Dimension Q shall be measured from the seating plane to the base plane.
- This dimension allows for off-center lid, meniscus and glass overrun.
- The basic pin spacing is .100 (2.54 mm) between centerlines. Each pin centerline shall be located within ±.010 (.25 mm) of its exact longitudinal position relative to pins 1 and 16.
- Applies to all four corners (leads number 1, 8, 9, and 16), and 40.5 shall apply.
- Lead center when θ is 0°. E<sub>1</sub> shall be measured at the centerline of the leads (see 40.4 of this appendix).
- All leads - Increase maximum limit by .003 (.08 mm) measured at the center of the flat, when lead finish A is applied.
- Fourteen spaces.
- If this configuration is used, no organic or polymeric materials shall be welded to the bottom of the package to cover the leads.

Figure 1: Package outline and dimensions specified for 16-lead ceramic dual-in-line package (CERDIP).

<u>Designation</u>	<u>Measured Value</u>
A	3.9 (.155)
b	.46 (.018)
b <sub>1</sub>	1.52 (.060)
e	.25 (.010)
D	19.1 (.750)
E	6.9 (.270)
E <sub>1</sub>	7.1 (.280)
E <sub>2</sub>	-
E <sub>3</sub>	-
e	2.5 (.100)
L	3.6 (.140)
L <sub>1</sub>	4.1 (.160)
Q	.64 (.025)
Q <sub>1</sub>	-
S	.64 (.025)
S <sub>1</sub>	.51 (.020)
S <sub>2</sub>	1.52 (.060)

Note: Values outside parentheses are in millimeters.  
 Values within parentheses are in inches.

Figure 2: Package Dimensions

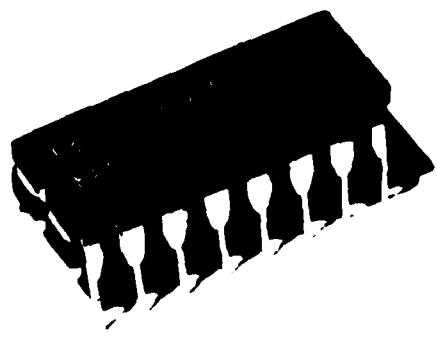


Figure 3: External view showing package markings  
of device as received Mag: 2.5X

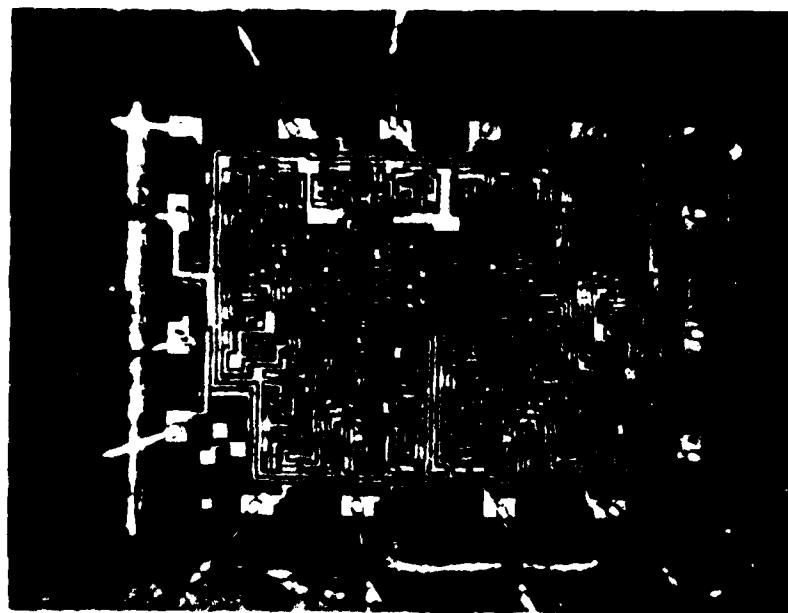


Figure 4: Interior view showing layout of chip  
Mag: 32X

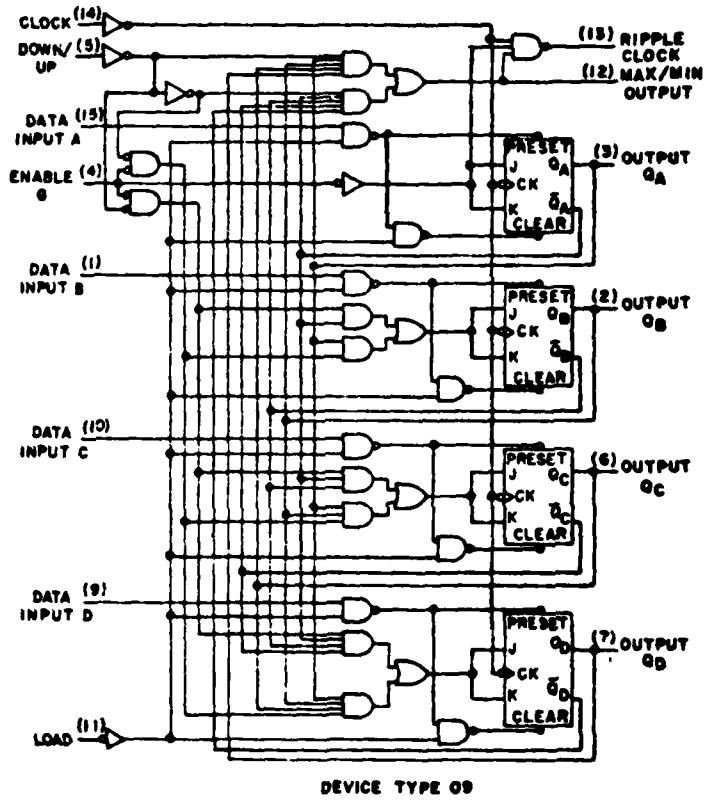
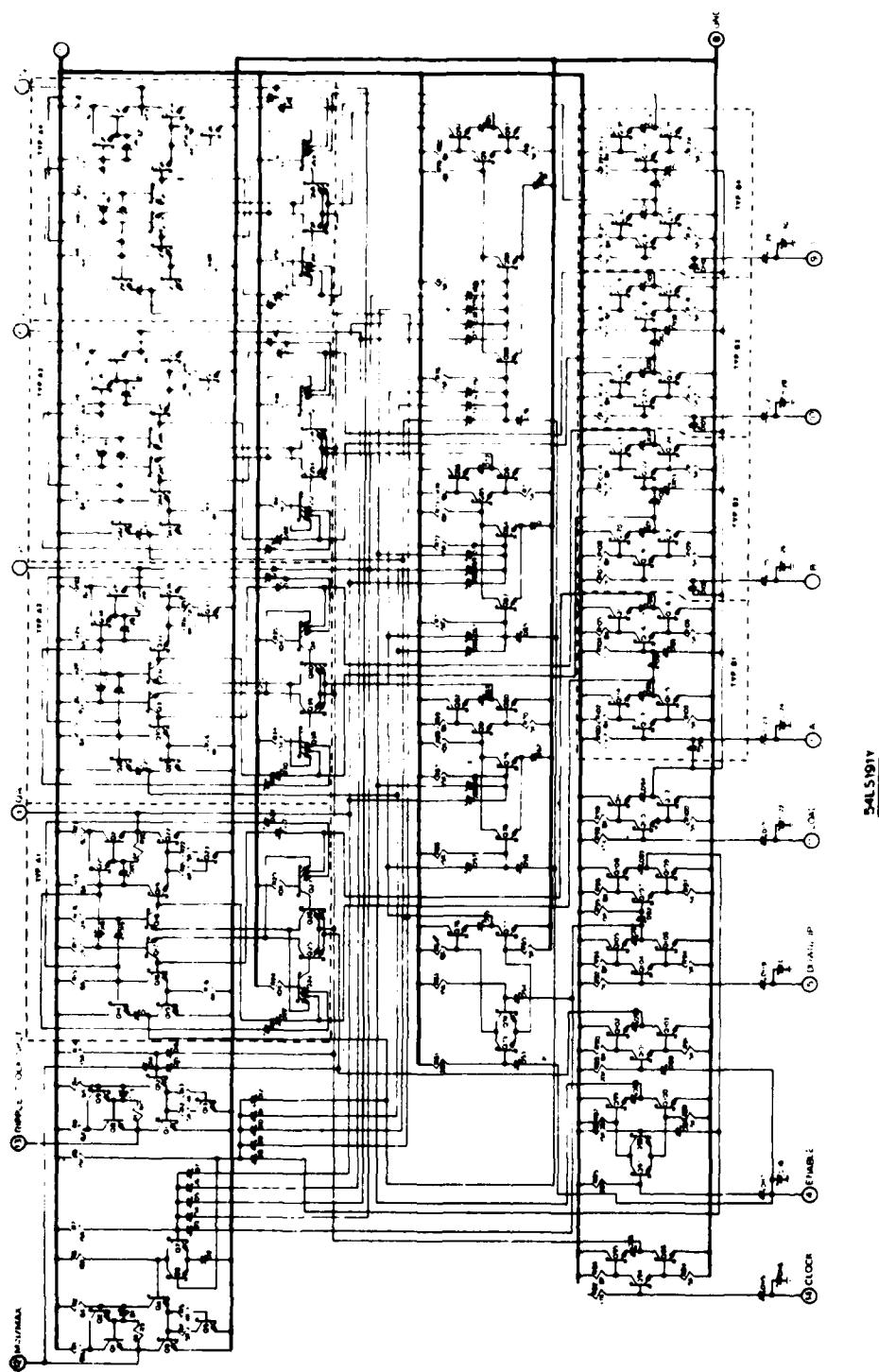


Figure 5: Logic diagram showing external pin connections for the device



**Figure 6:** Detailed schematic of the device

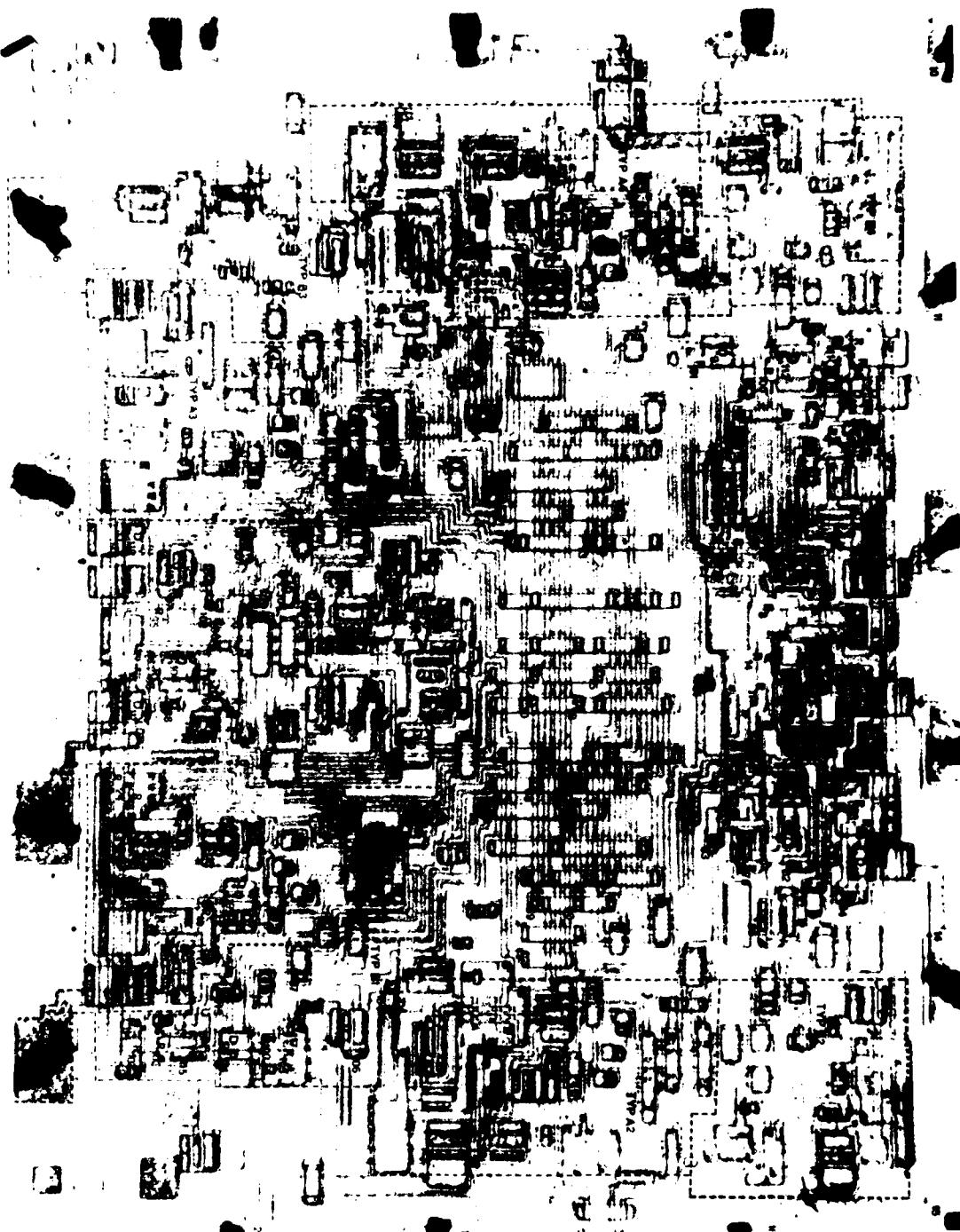


Figure 7: Detailed map of chip with device components  
designations corresponding to those in Figure 6  
Mag: 100X (Reversed image)

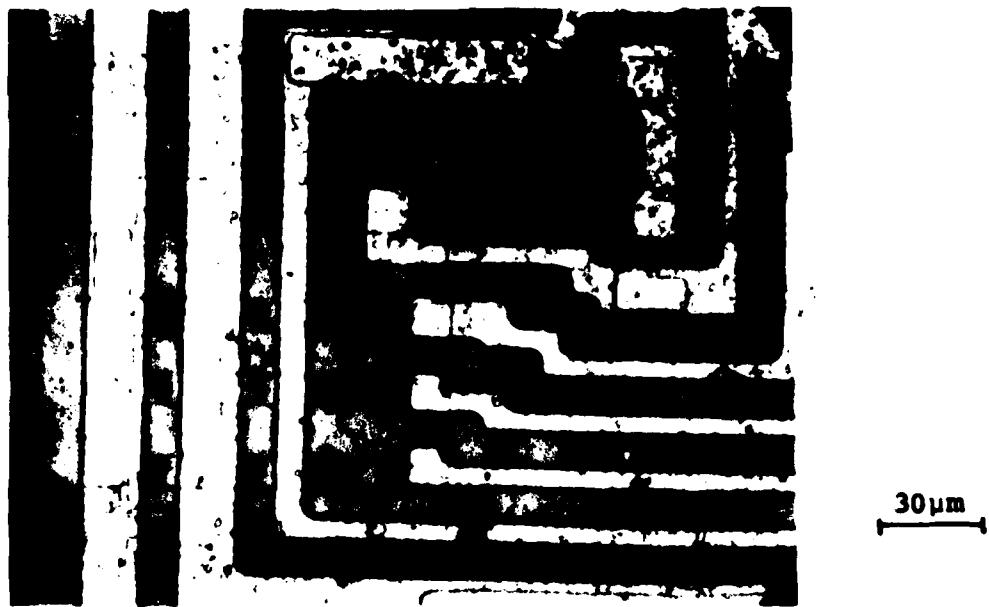


Figure 8: Arrows indicate oxide defects which have been accentuated by use of an aluminum etch

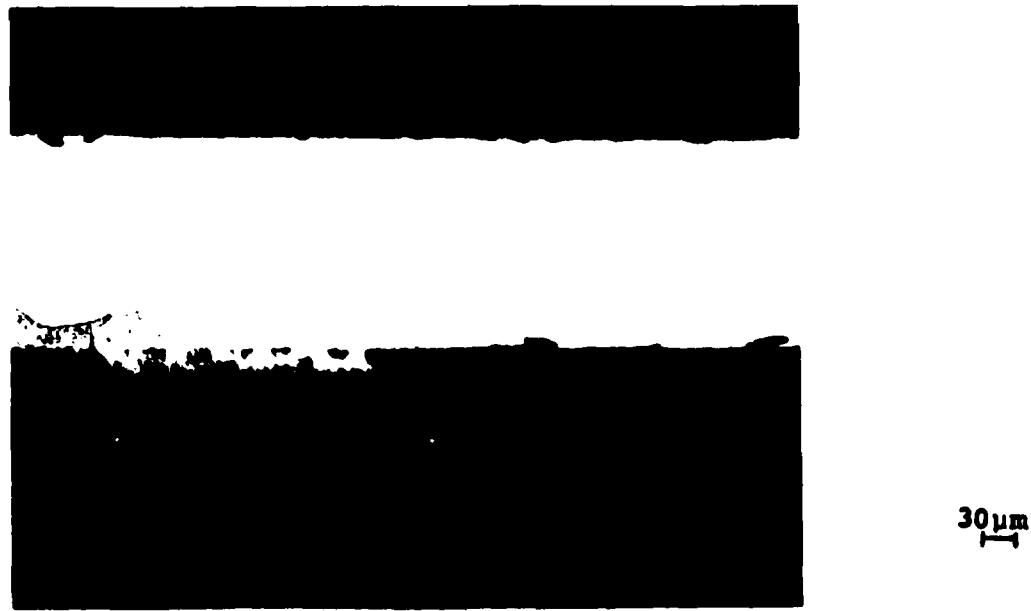


Figure 9: Voids under one edge of chip

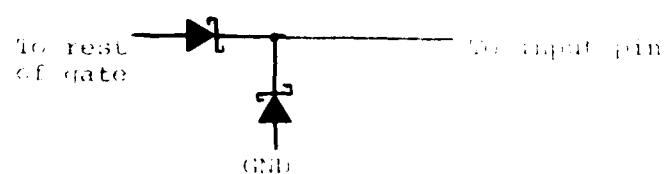
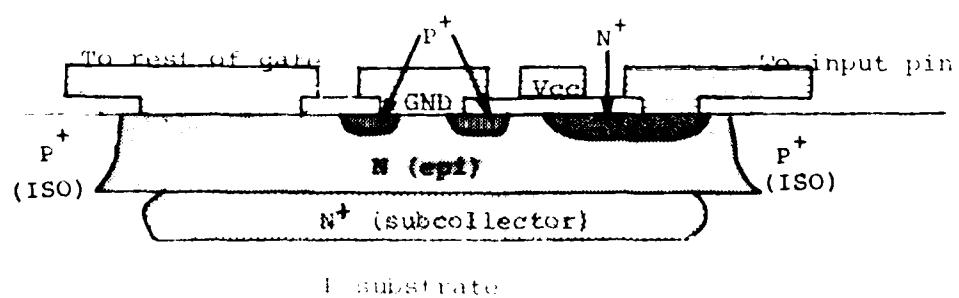
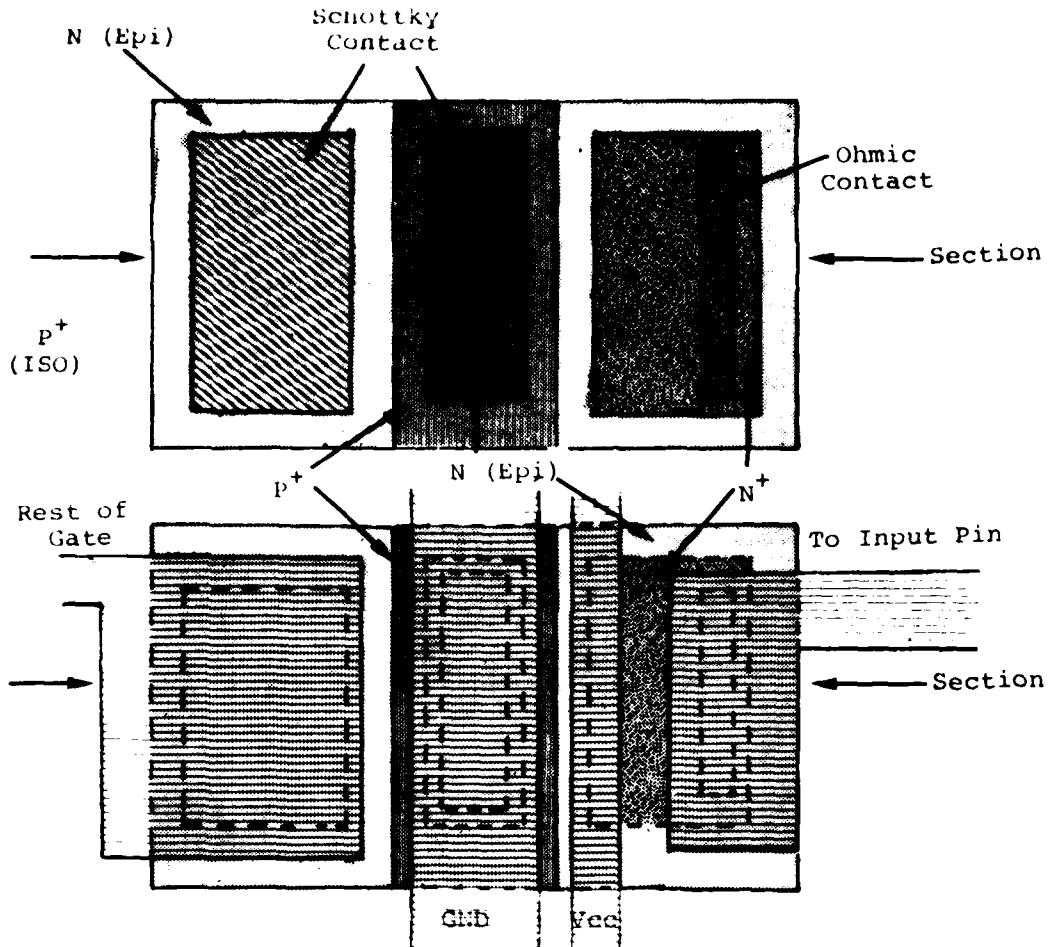


Figure 10: Schematic diagram showing cross-sectional view of input structure (not to scale).

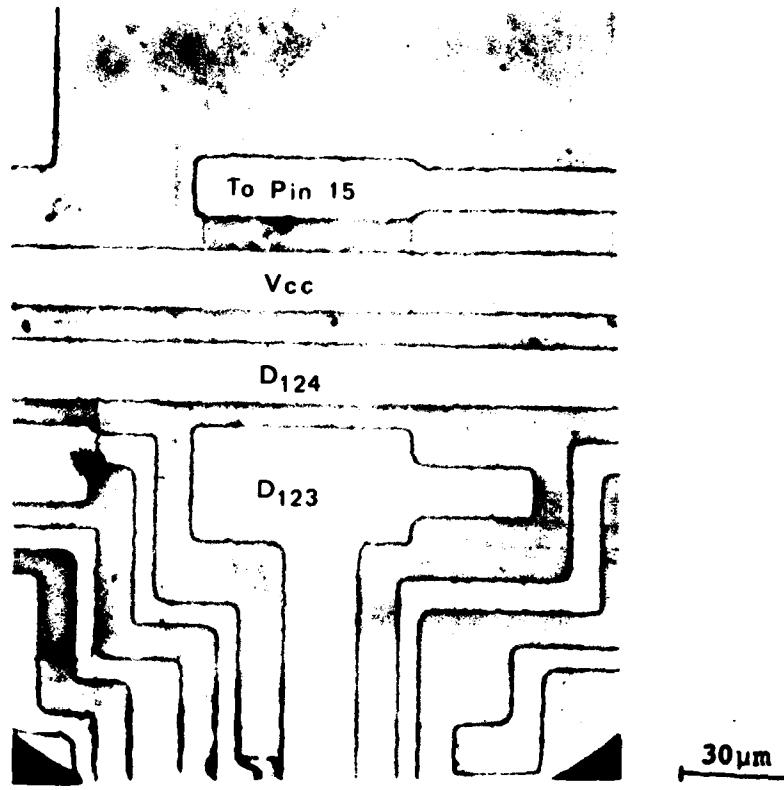


Figure 11: Photomicrograph showing top view of input structure

## APPENDIX H

### CONSTRUCTION ANALYSIS OF VENDOR B 54LS191 STANDARD SCHOTTKY TTL INTEGRATED CIRCUIT IN CERAMIC DIP

#### Abstract

A Vendor B synchronous 4-bit binary up/down counter was subjected to a detailed construction analysis. State changes of the counter are synchronous with the low to high transition of the clock pulse input. The device complexity is 58 equivalent gates, and low power Schotkky technology is employed in the device fabrication.

Three devices were received packaged in standard 16-pin ceramic dual-in-line packages (CERDIP's) date coded 7726. The leads were tin plated Kovar; the internal wires were 1 mil aluminum, having better than adequate pull-strengths. The single level chip metallization was vapor deposited Al over sputtered Ti-W over  $Pt_xSi_y$  in the contact areas. The chip is entirely covered with vapor deposited PSG for scratch protection and passivation. One weakness in workmanship was noted. One of the devices which was received packaged as an LS191 was actually an LS174A, and the branding on the package lid was incorrect. Other than this discrepancy, no weaknesses in construction or workmanship were noted.

#### Introduction

This analysis was performed as part of an evaluation of this device for Rome Air Development Center (RADC). The analysis was designed to document the construction details and materials used in these units and to identify shortcomings in the design or defects in workmanship, if any.

#### Results

##### The Package

The units were packaged in 16-lead ceramic dual-in-line packages (CERDIP). Both lid and base were of smooth alumina, with a fritted glass seal. The leads were embedded in the seal and consisted of tin plated Kovar. The thickness of the tin plating was measured to be 6.4 m (250 inches).

6.4  $\mu\text{m}$  (250  $\mu\text{inches}$ ). The package dimensions were found to be within the limits specified in MIL-M-38510D and are shown in Figure 2; the case outline drawing and specification for dimensions are shown in Figure 1. The package markings were as shown in Figure 3.

The internal area of the lead frame which is used for bonding pads for the aluminum wires was clad with aluminum. This is rolled on prior to assembly of the package, and was measured to be 3.4 to 16.2  $\mu\text{m}$  (134 to 638  $\mu\text{inches}$ ) thick.

#### The Chip

The lid was removed by applying a mechanical stress to it and forcing a chisel edge into the seal in a controlled manner until the seal fractured. An overall view of the chip is shown in Figure 4. The chip was measured to be 1.32 x 1.51 x 0.20 mm (51.9 x 59.4 x 7.9 mils). The volume of the cavity was 0.022  $\text{cm}^3$ , including the recess in the package lid. The chip was mounted using a silicon-gold eutectic approximately 8.5  $\mu\text{m}$  (0.33 mils) thick with a thick film gold paste providing the gold. This thick film gold paste also contains minute glass particles which are fired into the ceramic at 920°C, thus providing the adhesion to the ceramic substrate. Away from the chip the gold metallization which lined the bottom of the cavity also was measured to be 8.5  $\mu\text{m}$  (0.33 mils) thick. Thermal resistances were measured to be  $\theta_{\text{junction-to-air}} = 123.3^\circ\text{C/W}$  and  $\theta_{\text{junction-to-case}} = 19.0^\circ\text{C/W}$ .

The internal wires were ultrasonically bonded, 1 mil diameter aluminum. Microbond-pull testing of 8 of the 16 wires yielded a range in pull strength from 2.5 to 4.0 grams-force, with an average of 3.4. These wires exceed the minimum pull-strength of 1.5 gm-f specified in MIL-STD-883B, Method 2011.2. No bond defects were noted.

The chip metallization was a single level interconnection scheme which used aluminum 2.1  $\mu\text{m}$  (83  $\mu\text{inches}$ ) thick over Ti-W approximately 4,000Å thick. The presence of the Ti-W layer provides good adhesion to the Si and  $\text{SiO}_2$  and is a diffusion barrier to the aluminum. The platinum-silicide in the contact areas gives good ohmic contact for base (P) and emitter (N+) diffusions and Schottky barrier contacts for collectors (N). The above thicknesses were measured in an angle cross-section. The aluminum layer was vapor deposited and the Ti-W was sputter deposited in an undisclosed ratio. The  $\text{Pt}_x\text{Si}_y$  is formed by sputtering on Pt in a very thin layer and sintering to form  $\text{Pt}_x\text{Si}_y$  in the contact areas, followed by blanket etching to remove the Pt elsewhere. A phosphosilicate glass (PSG) layer about 2.0  $\mu\text{m}$  (79  $\mu\text{inches}$ ) thick covered the entire chip as passivation and protection against scratching during handling.

The highest current density was found to exist in the ground metallization run. Here the current is 4.3mA maximum and the smallest metallization width is  $2.1 \times 10^{-3}$ cm. The metallization thickness of  $2.1 \times 10^{-4}$ cm results in a minimum cross-sectional area of  $4.48 \times 10^{-7}$ cm<sup>2</sup> which yields a maximum current density of  $9.5 \times 10^3$ A/cm<sup>2</sup>. Over an oxide step the current density could reach  $1.4 \times 10^4$ A/cm<sup>2</sup>, since the metallization thins to about 2/3 its thickness as it goes over an oxide step. This is within the specification of  $5 \times 10^5$ A/cm<sup>2</sup> found in MIL-M-38510 as a maximum current density for Al to avoid an unacceptable level of electromigration failures.

The chip was photographed and mapped to identify all the components. Figure 5 shows the logic layout of the device as related to the external pin connections and Figure 6 shows a detailed schematic of the device. Figure 7 shows the chip with all of the components labelled with the schematic symbol designations corresponding to those given in Figure 6.

Visual inspection of the chip was performed using Method 2010.3 of MIL-STD-883B as a guide, and one workmanship weakness was noted. One of the devices received with package markings as shown in Figure 3 was not an LS191, but an LS174A. A comparison of the overall view of the chip (shown in Figure 8) with that shown in Figure 4 shows readily apparent differences. This 174A was apparently labelled incorrectly after packaging, and was subsequently shipped as a 191. Markings on the package bottom indicate that the device is a 174A. Other than this workmanship weakness, no faults were found in the device.

#### The Components

The substrate was P-type. Subcollectors approximately 16.6  $\mu$ m (.65 mils) deep, consisting of low resistivity N-type diffusions, were made in positions corresponding to the transistors prior to the growth of the epitaxial layer. These provided high conductivity paths from the vicinity of the base-collector junctions to the collector contact diffusions. An N-type epitaxy about 5.1  $\mu$ m (.20 mils) thick was then grown.

After the growth of the epitaxial layer, P-type isolation diffusions approximately 4.7  $\mu$ m (0.19 mils) deep were made, partitioning the epitaxial layer into individual collector regions and other components. The P-type base diffusion followed and the resistors were also made at this time. This diffusion was measured to be about 1.3  $\mu$ m (51  $\mu$ inches) deep. This also created the p-n junction guard rings for the input clamping diode to be discussed later. The N+ type diffusion, measured to be about 0.6  $\mu$ m (31  $\mu$ inches) deep, then created the emitters and the collector contact enhancement regions. This latter was necessary to achieve ohmic contact to the low-doped epitaxial layer.

### The Transistors

With the exception of 27 transistors (#'s 3, 7, 11, 15, 19, 23, 27, 31, 35, 37, 44, 53, 59, 67, 74, 82, 90, 98, 103, 108, 112, 117, 123, 128, 133, 139, 151), all transistors utilized the Schottky design. The base regions of these Schottky transistors were annular, having rectangular "hole" within a rectangular shaped diffusion. Hence a portion of the epitaxial region at the surface was surrounded by this annular ring. The contact hole in the base oxide exposed both part of the base region and all of the epitaxial region which was surrounded by the base ring. This latter was part of the collector. When the metallization was deposited within the contact hole, it created the ohmic contact to the base region and also created the Schottky diode between base and collector. This occurred because of the relative doping level of the base region (high doping yields ohmic contact) versus that of the epitaxial (collector) region (low doping yields rectifying Schottky contact). The 27 transistors mentioned above as exceptions from this design were standard bipolar construction.

### The Diodes

Each input had a Schottky barrier diode to ground to provide protection for the input against negative voltage spikes. The construction was quite similar to that in the transistors, forming what was actually a p-n junction - Schottky barrier hybrid diode. A cross-sectional diagram (not to scale) of the construction of the input structure is shown in Figure 9, with a top view shown in Figure 10. References 1 and 2 describe the theory and advantages of such a structure.

### The Resistors

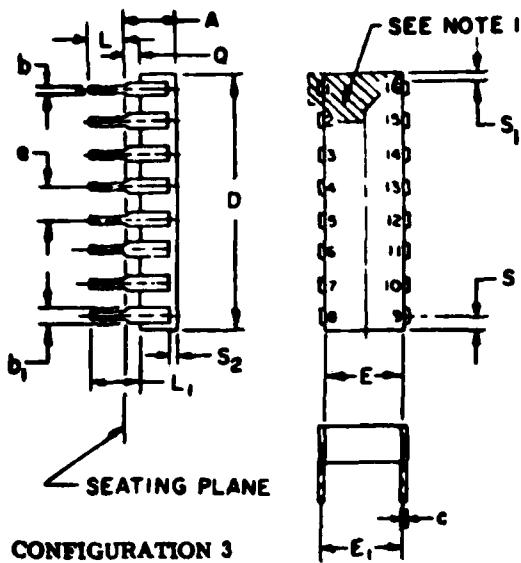
P-type base diffusion was used for most of the resistors. This diffusion had a resistivity of about  $1,000\Omega/\square$ . The diffusion depth was measured to be about  $1.3 \mu\text{m}$  ( $51 \mu\text{inches}$ ). A few of the resistors were made by contacting part of the epitaxial region. These are not well defined, and, according to the vendor, can vary as much as 100% from their nominal values.

### Conclusions

The construction and workmanship of this device appear to be sound and in keeping with military specification with one exception. One of the devices which was received for construction analysis packaged as an LS191 was actually an LS174A. Other than this discrepancy, no weaknesses in construction or workmanship were noted.

References:

1. RADC-TR-76-292, Reliability Evaluation of Schottky Barrier Diode Microcircuits, Raytheon Company, Sept. 1976, Appendix B, p. 158.
2. R.A. Zettler and A.M. Cowley, "p-n Junction-Schottky Barrier Hybrid Diode" IEEE Transactions on E.D., Vol. ED-16, No. 1, January 1969.



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		.200		5.08	
b	.014	.023	.36	.58	8
b <sub>1</sub>	.030	.070	.76	1.78	2, 8
c	.008	.015	.20	.38	8
D		.840		21.34	4
E	.220	.310	5.59	7.87	4
E <sub>1</sub>	.290	.320	7.37	8.13	7
E <sub>2</sub>	.100		2.54		
E <sub>3</sub>	.050		1.27		
e	.100 BSC		2.54 BSC		5, 9
L	.125	.200	3.18	5.08	
L <sub>1</sub>	.150		3.81		
Q	.015	.060	.38	1.32	3
Q <sub>1</sub>	.020		.51		
S		.080		2.03	8
S <sub>1</sub>	.005		.13		8
S <sub>2</sub>	.005		.13		
α	0°	15°	0°	15°	

NOTES:

1. Index areas; a notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The minimum limit for dimension b<sub>1</sub> may be .020 (.51 mm) for leads number 1, 8, 9 and 16 only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is .100 (2.54 mm) between centerlines. Each pin centerline shall be located within ±.010 (.25 mm) of its exact longitudinal position relative to pins 1 and 16.
6. Applies to all four corners (leads number 1, 8, 9, and 16), and 40.5 shall apply.
7. Lead center when α is 0. E<sub>1</sub> shall be measured at the centerline of the leads (see 40.4 of this appendix).
8. All leads - Increase maximum limit by .003 (.08 mm) measured at the center of the flat, when lead finish A is applied.
9. Fourteen spaces.
10. If this configuration is used, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.

Figure 1: Package outline and dimensions specified for 16-lead ceramic dual-in-line package (CERDIP).

<u>Designation</u>	<u>Measured Value</u>
A	3.99 (.157)
b	0.48 (.019)
b <sub>1</sub>	1.52 (.060)
C	0.28 (.011)
D	19.6 (.773)
E	6.30 (.248)
E <sub>1</sub>	7.37 (.290)
E <sub>2</sub>	-
E <sub>3</sub>	-
e	2.54 (.100)
L	3.56 (.140)
L <sub>1</sub>	4.32 (.170)
Q	0.76 (.030)
Q <sub>1</sub>	-
S	0.76 (.030)
S <sub>1</sub>	0.38 (.015)
S <sub>2</sub>	1.52 (.060)

Note: Values outside parentheses are in millimeters.  
 Values within parentheses are in inches.

Figure 2: Package Dimensions

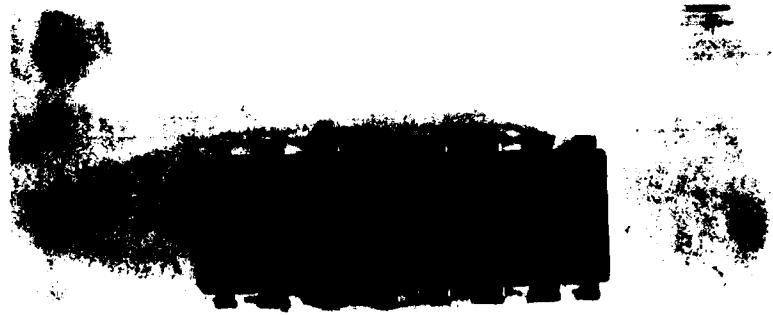


Figure 3: External view of device as received  
showing package markings Mag: ~3X

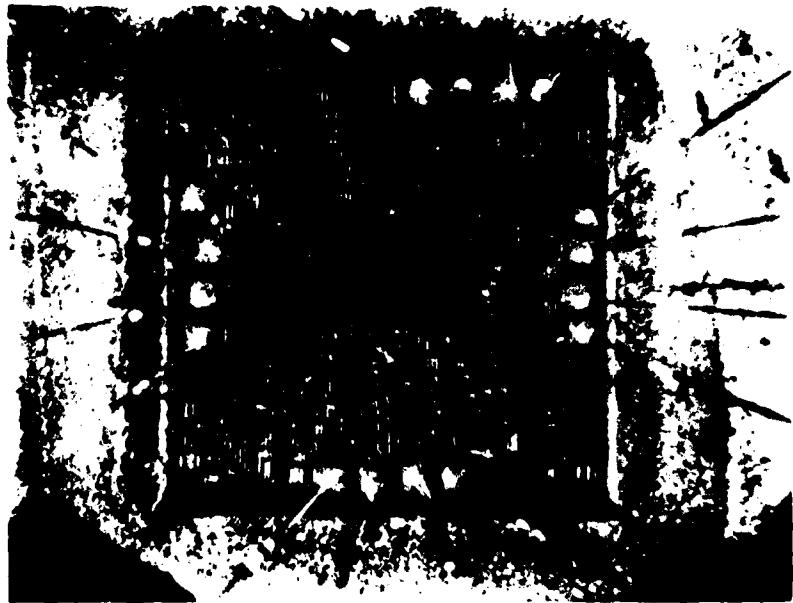
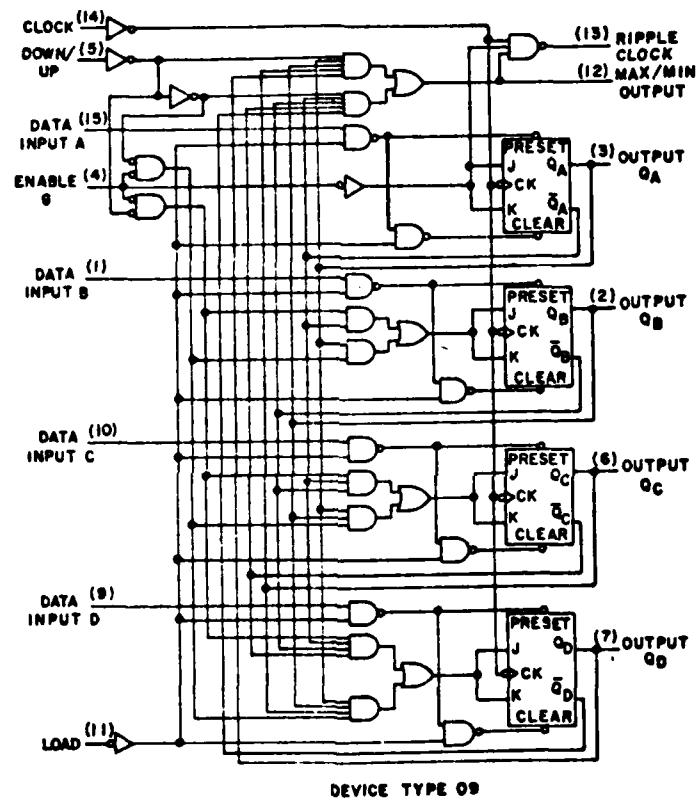
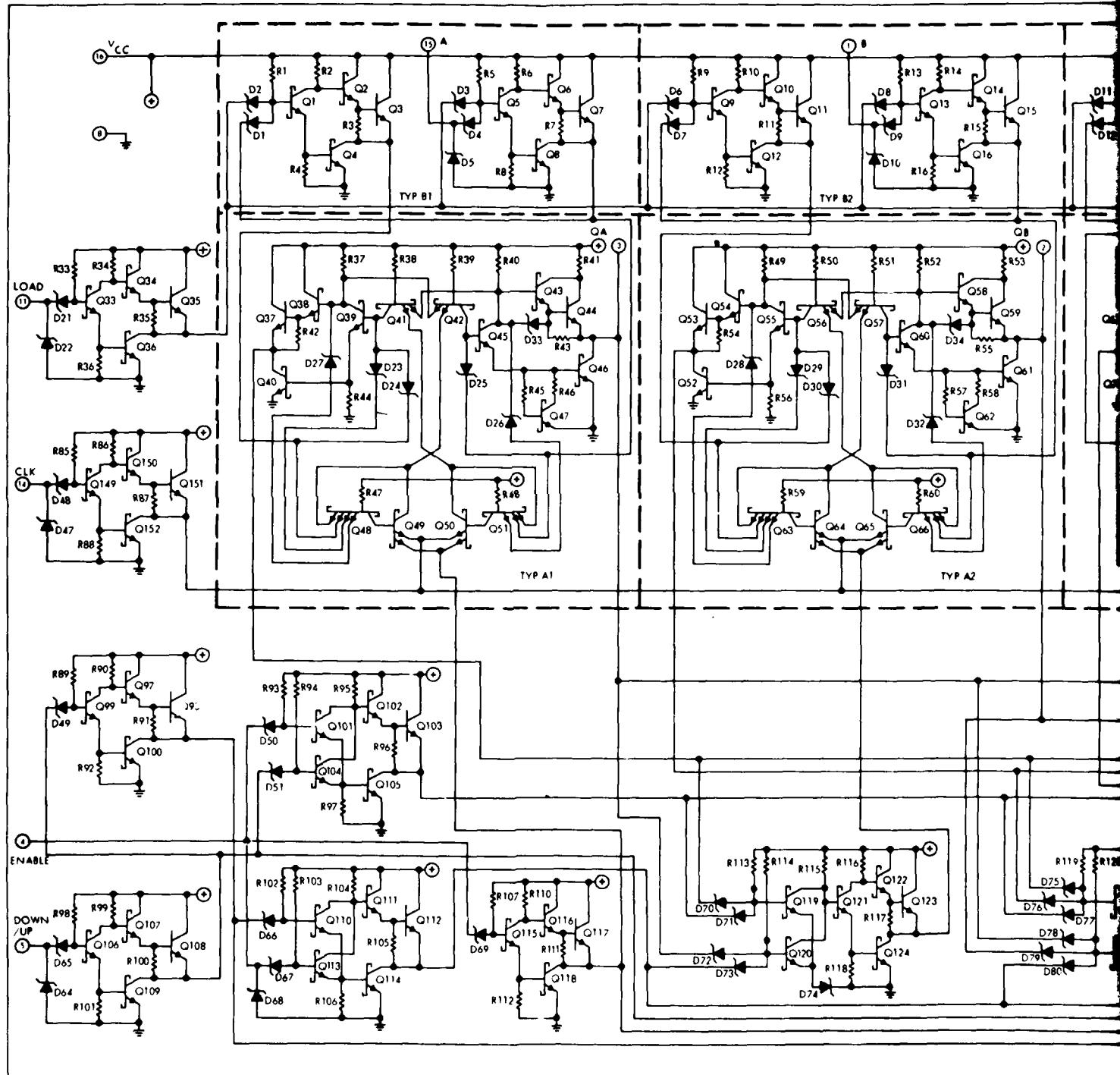


Figure 4: Overall view of chip Mag: ~35X



DEVICE TYPE 09

Figure 5: Logic diagram of the device



H-10

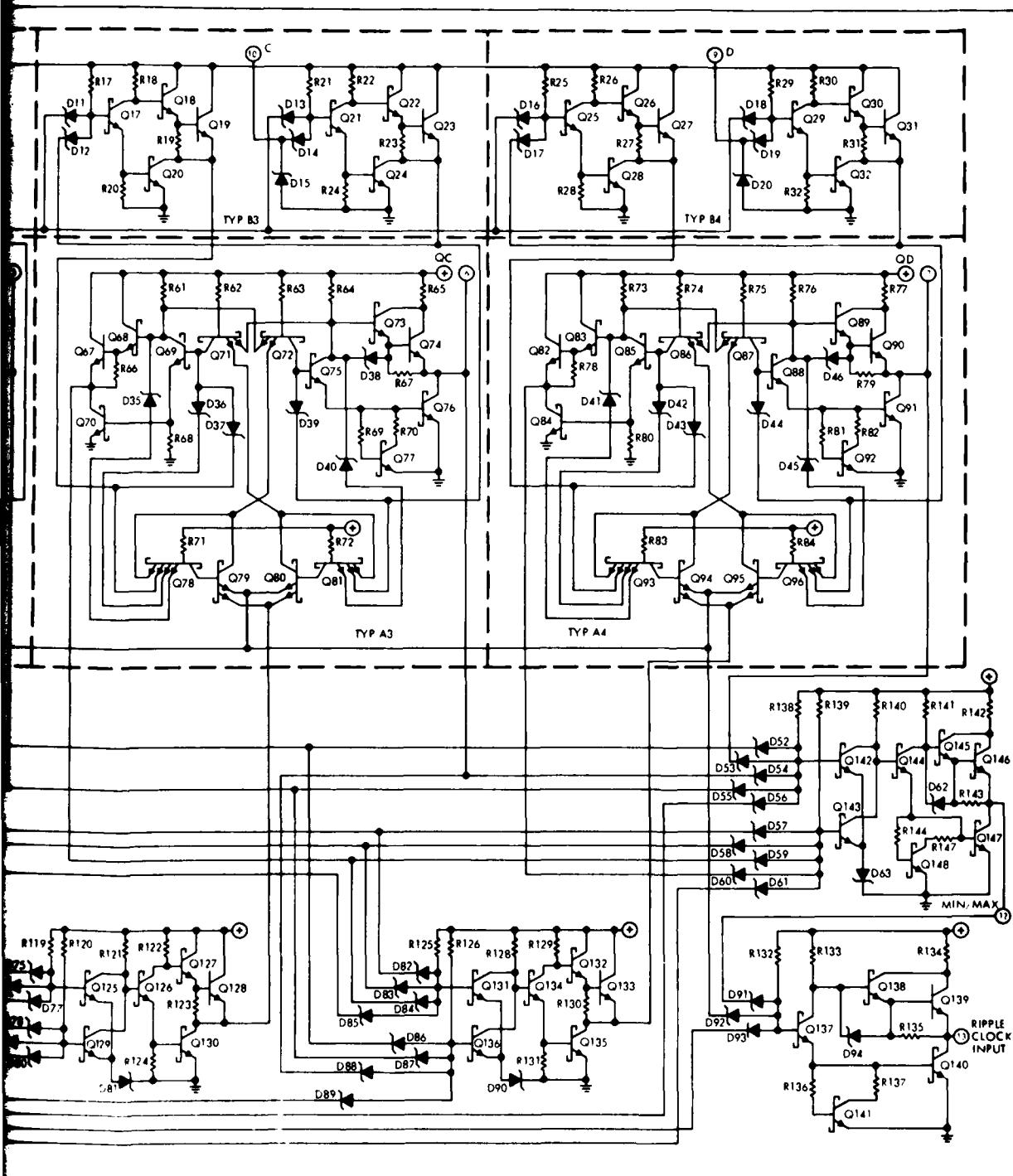


Figure 6: Detailed schematic of the device.

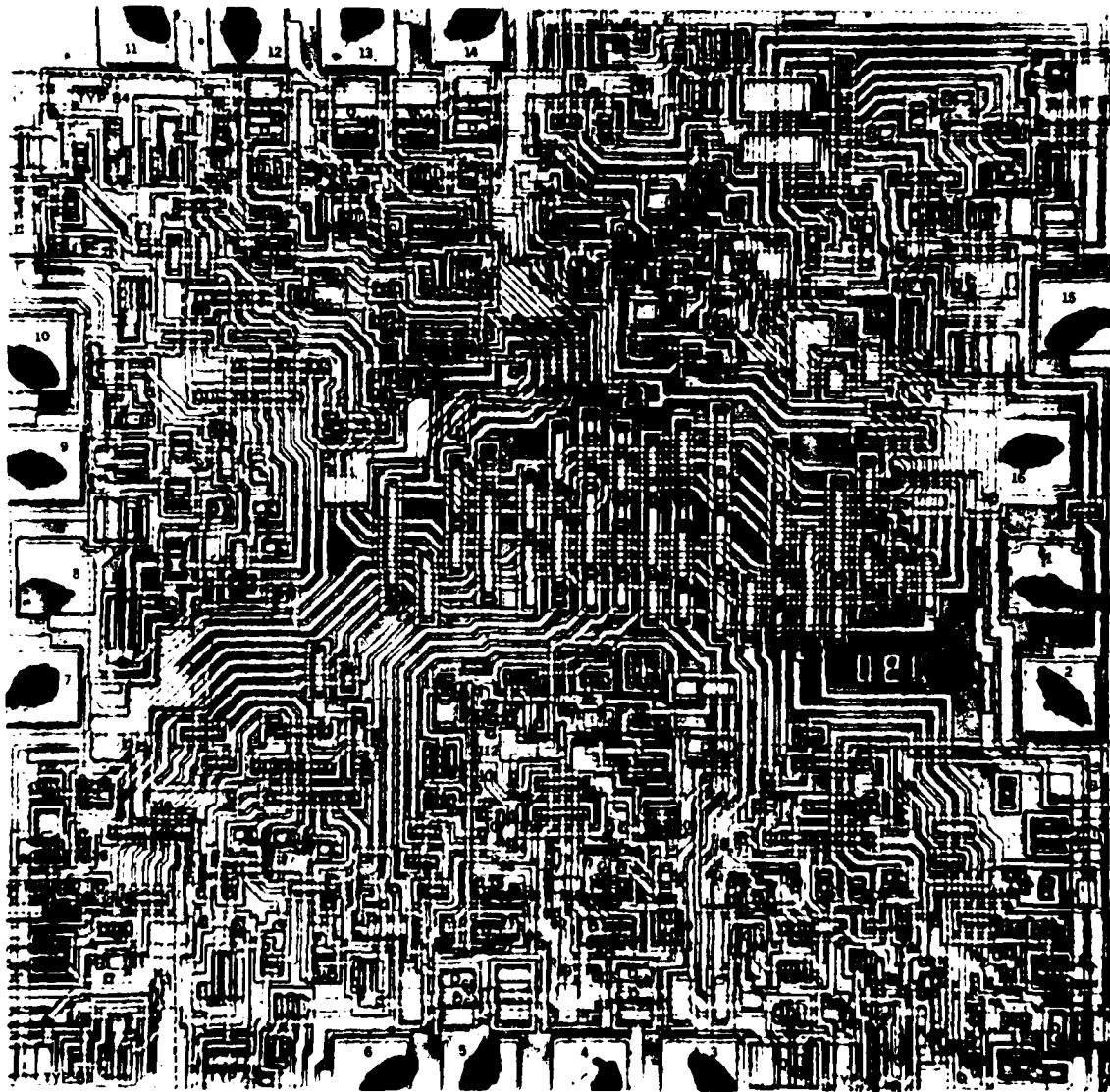
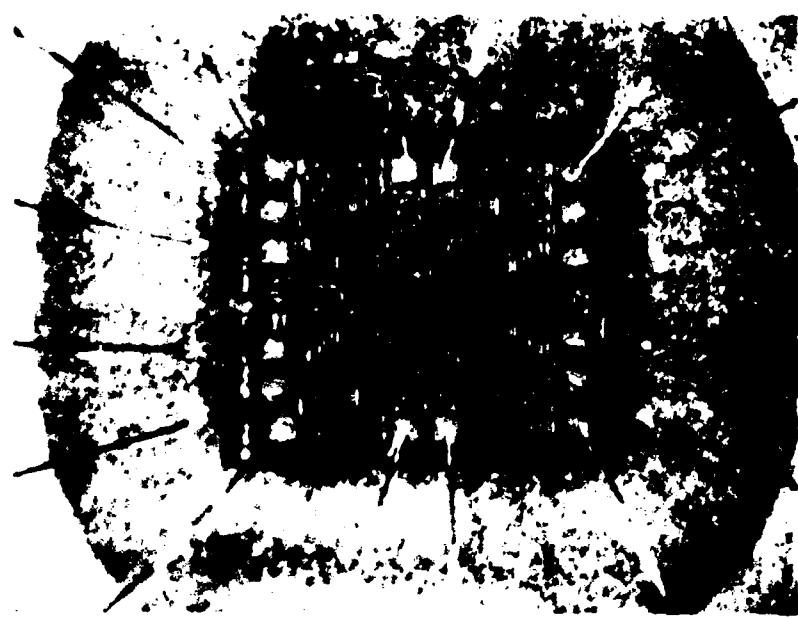


Figure 7: Detailed map of the chip with component labels corresponding to those in Figure 6  
Mag: ~100X (Reversed image)

THIS PAGE IS BEST QUALITY PRACTICABLE  
FROM COPY FURNISHED TO DDC

H-11



**Figure 8:** Overall view of LS174A chip which was received packaged as an LS191, with package markings as shown in Figure 3  
Mag: ~35X

THIS PAGE IS OF THE ORIGINAL  
AND ONLY ONE COPY IS MAILED

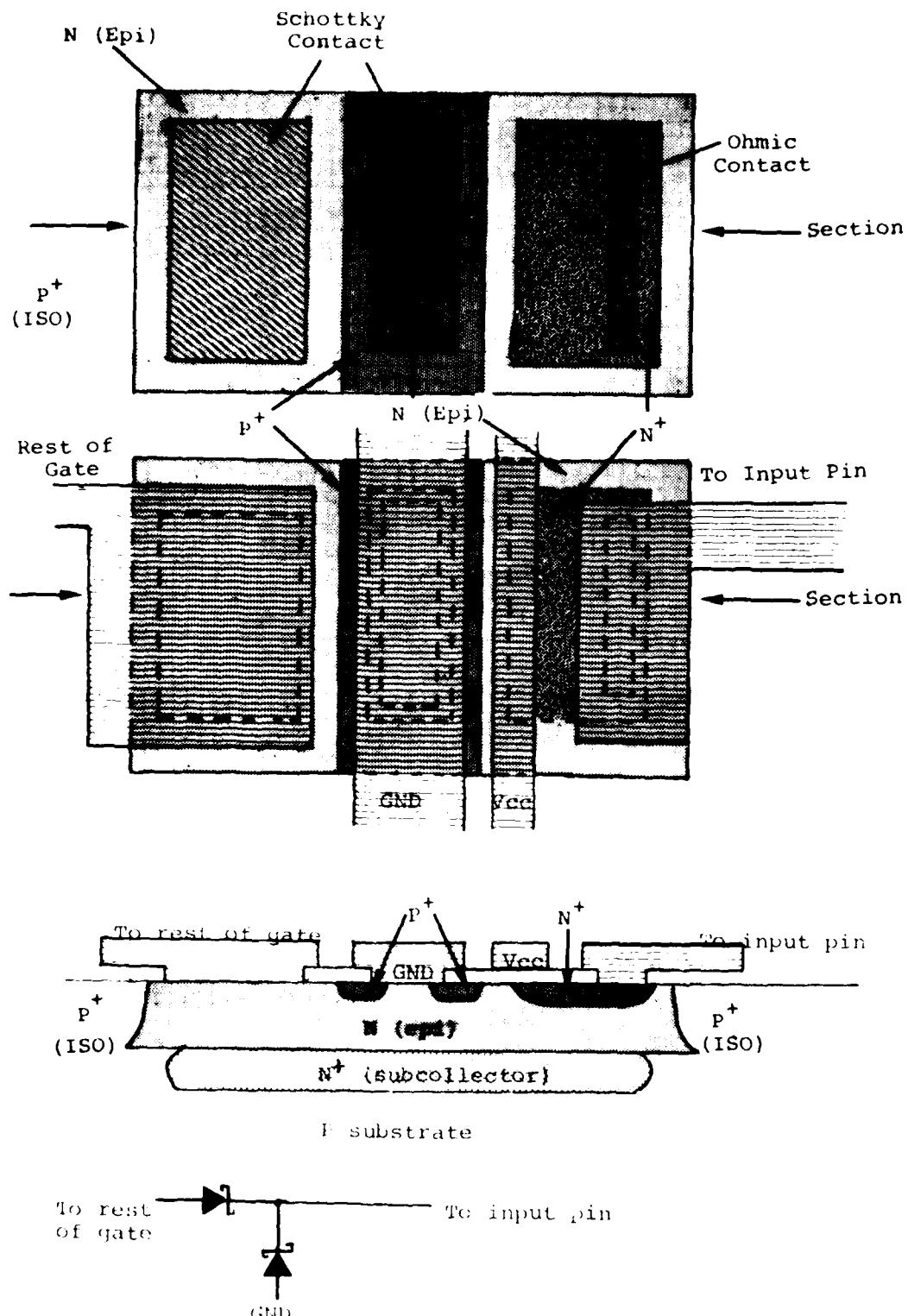
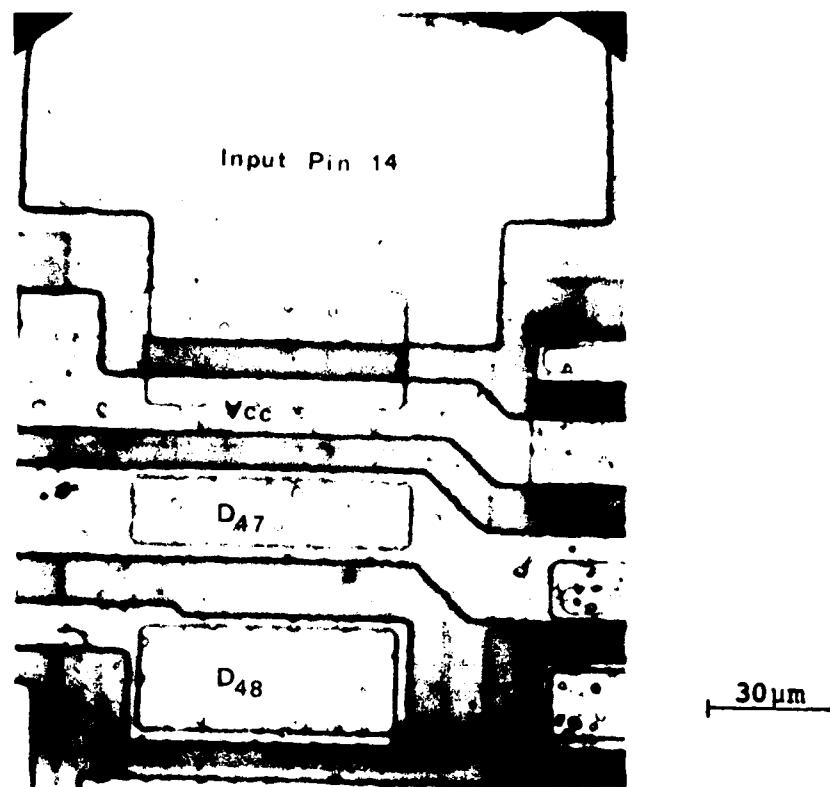


Figure 9: Schematic diagram showing cross-sectional view of input structure (not to scale).



**Figure 10:** Top view of input structure at pin 14

APPENDIX I  
CONSTRUCTION ANALYSIS OF VENDOR C 27LS00  
STANDARD SCHOTTKY TTL INTEGRATED CIRCUIT IN CERAMIC DIP

Abstract

A Vendor C 256-bit RAM, AM27LS00, was subjected to a detailed construction analysis. The device is a fully decoded 256-bit random access memory organized as a 256-word by 1-bit array with an 8-bit address field and separate data in and data out lines. The device has three active low chip select inputs and a three state output. Low power Schottky technology is employed in the device fabrication.

Two devices were received packaged in standard 16 pin ceramic dual-in-line packages (CERDIP's) date coded 7744. The leads were tin plated Kovar; the internal wires were 1 mil aluminum, having better than adequate pull-strengths. Each level of the two level chip metallization was vapor deposited Al over sputtered Ti-W over Pt<sub>x</sub>Si<sub>y</sub> in the contact areas. The chip was entirely covered with vapor deposited PSG for scratch protection and passivation. Several foreign particles were present on the chip even after a thorough cleaning.

The input and output structures of the device were TTL, but the internal logic was ECL. Hence compatibility with other TTL devices and faster logic have been achieved, the latter in exchange for greater power consumption.

No other weaknesses in construction or workmanship were noted.

## Introduction

This analysis was performed as part of an evaluation of this device for Rome Air Development Center (RADC). The analysis was designed to document the construction details and materials used in these units and to identify shortcomings in the design or defects in workmanship, if any.

## Results

### The Package

The units were packaged in 16-lead ceramic dual-in-line packages (CERDIP). Both lid and base were of smooth alumina, with a fritted glass seal. The leads were embedded in the seal and consisted of tin plated Kovar. The thickness of the tin plating was measured to be 8.9 $\mu\text{m}$  (350 $\mu\text{inches}$ ). The package dimensions were found to be within the limits specified in MIL-M-38510D and are shown in Figure 2; the case outline drawing and specification for dimensions are shown in Figure 1. The package markings were as shown in Figure 3.

The internal area of the lead frame which is used for bonding pads for the aluminum wires was clad with aluminum. This is rolled on prior to assembly of the package, and was measured to be 7.0 $\mu\text{m}$  (276 $\mu\text{inches}$ ) thick.

### The Chip

The lid was removed by applying a mechanical stress to it and forcing a chisel edge into the seal in a controlled manner until the seal fractured. An overall view of the chip is shown in Figure 4. The chip was measured to be 2.10 x 3.17 x 0.34 mm (82.7 x 124.8 x 13.4 mils). The volume of the cavity was 0.034 cm<sup>3</sup> including the recess in the package lid. The chip was mounted using a silicon-gold eutectic approximately 9.5 $\mu\text{m}$  (0.37 mils) thick with a thick film gold paste providing the gold. This thick film gold paste also contains minute glass particles which are fired into the ceramic at 920°C, thus providing the adhesion to the ceramic substrate. Away from the chip the gold metallization which lined the bottom of the cavity was measured to be 5.1 $\mu\text{m}$  (0.20 mils) thick. Thermal resistances were measured to be  $\theta_{\text{junction-to-air}} = 104.8^{\circ}\text{C/W}$  and  $\theta_{\text{junction-to-case}} = 11.5^{\circ}\text{C/W}$ .

The internal wires were ultrasonically bonded, 1 mil diameter aluminum. Microbond-pull testing of 8 of the 16 wires yielded a range in pull strength from 2.5 to 4.0 grams-force,

with an average of 3.2. These wires exceed the minimum pull-strength of 2.0 gm-f specified in MIL-STD-883B, Method 2011.2, although typically higher bond strengths are achieved with 1 mil Al wires using current technology. No failures occurred at the bond itself, and no bond defects were noted.

The chip metallization was a two level interconnection scheme which in each level used aluminum 1.5 $\mu$ m (59 $\mu$ inches) thick over Ti-W approximately 4,000 Å thick. The presence of the Ti-W layer provides good adhesion to the Si and Si<sub>3</sub>N<sub>4</sub> and is a diffusion barrier to the aluminum. The platinum-silicide in the contact areas gives good contact for base (P) and emitter (N+) diffusions and Schottky barrier contacts for collectors (N). The above thicknesses were measured in an angle cross-section. The aluminum layer was vapor deposited and the Ti-W was sputter deposited in an undisclosed ratio. The Pt<sub>x</sub>Si<sub>y</sub> is formed in the contact areas, followed by blanket etching to remove the Pt elsewhere. A phosphosilicate glass layer about 1.1 $\mu$ m (43 $\mu$ inches) thick covered the entire chip as passivation and protection against scratching during handling.

The highest current density was found to exist in the collector metallization run of Q64. Here the current is 16mA maximum and the smallest metallization width is  $9.8 \times 10^{-4}$  cm. The metallization thickness of  $1.5 \times 10^{-4}$  cm results in a minimum cross-sectional area of  $1.5 \times 10^{-7}$  cm<sup>2</sup> which yields a maximum current density of  $1.1 \times 10^5$  A/cm<sup>2</sup>. Over an oxide step the current density could reach  $1.6 \times 10^5$  A/cm<sup>2</sup>, since the metallization thins to about 2/3 its thickness as it goes over an oxide step. This is within the specification of  $5 \times 10^5$  A/cm<sup>2</sup> found in MIL-M-38510 as a maximum current density for Al to avoid an unacceptable level of electromigration failures, but by such a narrow margin as to cause concern that it might present a reliability hazard.

The chip was photographed and mapped to identify the components. Figure 5 shows the logic layout of the device. Figure 6 shows detailed schematics of the output (A) and input (C) structures of the device, with that of a memory cell shown in Figure 6B. Note that the inputs are pnp transistors, the base-emitter junctions of which replace the commonly used input diodes. Figure 7 shows the chip with regions labelled corresponding to those given in Figure 5. Figure 8 shows detailed views of these regions.

Visual inspection of the chip was performed using Method 2010.3 of MIL-STD-883B as a guide. The only workmanship weakness found was the presence of several foreign particles on the surface of the chip. These particles remained even after a thorough cleaning of the chip. While they were not seen as a reliability hazard, they did indicate that the vendor's inspection procedures need reviewing.

### The Components

The substrate was P-type. Subcollectors approximately  $6.2\mu\text{m}$  (0.24 mils) deep, consisting of low resistivity N-type diffusions, were made in positions corresponding to the transistors prior to the growth of the epitaxial layer. These provided high conductivity paths from the vicinity of the base-collector junctions to the collector contact diffusions. An N-type epitaxy about  $3.3\mu\text{m}$  (0.13 mils) thick was then grown.

After the growth of the epitaxial layer, P-type isolation diffusions approximately  $3.3\mu\text{m}$  (0.13 mils) deep were made, partitioning the epitaxial layer into individual collector regions and other components. The P-type base diffusion followed and the resistors were also made at this time. This diffusion was measured to be about  $1.8\mu\text{m}$  ( $71\mu\text{inches}$ ) deep. This also created the p-n junction guard rings for the input clamping diode to be discussed later. The N+ type diffusion, measured to be about  $0.7\mu\text{m}$  ( $28\mu\text{inches}$ ) deep, then created the emitters and the collector contact enhancement regions. This latter was necessary to achieve ohmic contact to the low-doped epitaxial layer.

### The Transistors

The output transistors utilized the Schottky design. The base regions of these Schottky transistors were annular, having a rectangular "hole" within a rectangular shaped diffusion. Hence a portion of the epitaxial region at the surface was surrounded by this annular ring. The contact hole in the base oxide exposed both part of the base region and all of the epitaxial region which was surrounded by the base ring. This latter was part of the collector. When the metallization was deposited within the contact hole, it created the ohmic contact to the base region and also created the Schottky diode between base and collector. This occurred because of the relative doping level of the base region (high doping yields ohmic contact) versus that of the epitaxial (collector) region (low doping yields rectifying Schottky contact). The other transistors were of standard bipolar construction.

### The Diodes

Each input had a Schottky barrier diode to ground to provide protection for the input against voltage spikes. The construction was quite similar to that in the transistors, forming what was actually a p-n junction - Schottky barrier hybrid diode. A cross-sectional diagram (not to scale) of the construction of the input structure is shown in Figure 9. Reference 1 and 2 describe the theory and advantages of such a structure.

### The Resistors

P-type base diffusion was used for all of the resistors. This diffusion had a resistivity of about  $1,000\Omega/\square$ . This sheet resistance was obtained by counting squares and comparing to values provided by the vendor. The diffusion depth was measured to be about  $1.8\mu\text{m}$  ( $71\mu\text{inches}$ ).

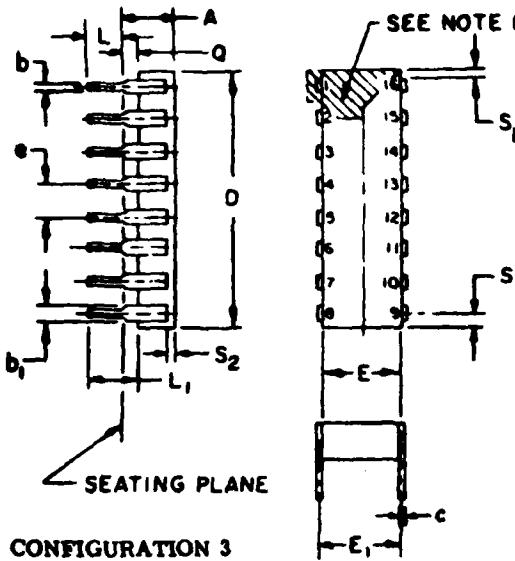
### Conclusions and Recommendations

In performing a construction analysis of Vendor C's 27LS00 three potential reliability hazards were identified. Several foreign particles were noted which could not be removed with cleaning. A review of the vendor's inspection procedures is recommended. Also, maximum current density was found to be only slightly below the  $2.0 \times 10^5 \text{ A/cm}^2$  maximum specified in MIL-M-38510 in order to avoid an unacceptable level of electromigration failures. A review of the vendor's design procedures is recommended. Finally, wire bond pull testing revealed strengths only slightly better than the  $2.0 \text{ gm-f}$  minimum specified in MIL-STD-883B, Method 2011.2, for 1 mil aluminum wires. A review of the vendor's bonding procedures is recommended.

### References

1. RADC-TR-292, Reliability Evaluation of Schottky Barrier Diode Microcircuits, Raytheon Company, Sept. 1976, Appendix B, P. 158.
2. R. A. Zettler and A. M. Cowley, "p-n Junction-Schottky Barrier Hybrid Diode" IEEE Transactions on E.D., Vol. ED-61, No. 1, January 1969.

THIS PAGE IS BEST QUALITY PRACTICABLE  
FROM COPY PROVIDED TO DDC



CONFIGURATION 3

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		.200		5.08	
I	.014	.023	.36	.58	8
I <sub>1</sub>	.030	.070	.76	1.98	2, 8
c	.008	.015	.20	.38	8
D	.840			21.34	4
E	.220	.310	5.59	7.87	4
E <sub>1</sub>	.290	.320	7.37	8.13	7
E <sub>2</sub>	.100		2.54		
E <sub>3</sub>	.050		1.27		
e	.100	BSC	2.54	BSC	5.9
L	.125	.200	3.18	5.08	
L <sub>1</sub>	.150		3.81		
Q	.015	.060	.38	1.52	3
Q <sub>1</sub>	.020		.51		
S		.080		2.03	8
S <sub>1</sub>	.005		.13		8
S <sub>2</sub>	.005		.13		
a	0"	15"	0"	15"	

NOTES:

- Index area; a notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
- The minimum limit for dimension b<sub>1</sub> may be .020 (.51 mm) for leads number 1, 8, 9 and 16 only.
- Dimension Q shall be measured from the seating plane to the base plane.
- This dimension allows for off-center lid, meniscus and glass overrun.
- The basic pin spacing is .100 (2.54 mm) between centerlines. Each pin centerline shall be located within  $\pm 0.010$  (.25 mm) of its exact longitudinal position relative to pins 1 and 16.
- Applies to all four corners (leads number 1, 8, 9, and 16), and 40.5 shall apply.
- Lead center when a is 0. E<sub>1</sub> shall be measured at the centerline of the leads (see 40.4 of this appendix).
- All leads - Increase maximum limit by .003 (.08 mm) measured at the center of the flat, when lead finish A is applied.
- Fourteen spaces.
- If this configuration is used, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.

Figure 1: Package outline and dimensions specified for 16-lead ceramic dual-in-line package (CERDIP).

Figure 2: Package Dimensions

<u>Designation</u>	<u>Measured Value</u>	
A	4.1	(0.16)
b	0.48	(0.019)
b <sub>1</sub>	1.5	(0.06)
e	0.25	(0.01)
D	19.1	(0.75)
E	6.8	(0.27)
E <sub>1</sub>	7.4	(0.29)
E <sub>2</sub>	-	-
E <sub>3</sub>	-	-
e	2.5	(0.10)
L	3.3	(0.13)
L <sub>1</sub>	3.8	(0.15)
Q	0.63	(0.025)
Q <sub>1</sub>	-	-
S	0.76	(0.03)
S <sub>1</sub>	0.51	(0.02)
S <sub>2</sub>	1.5	(0.06)

Note: Values outside parentheses are in millimeters.  
Values within parentheses are in inches.

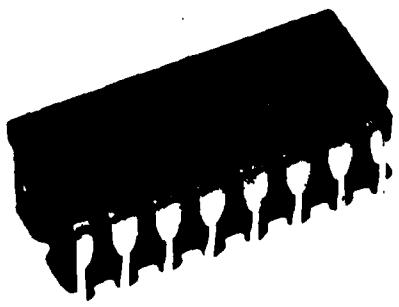


Figure 3: External view showing package markings  
of device as received. Magnification: 2.6X.

THIS PAGE IS BEST QUALITY PRACTICABLE  
FROM COPY FED FROM 10000

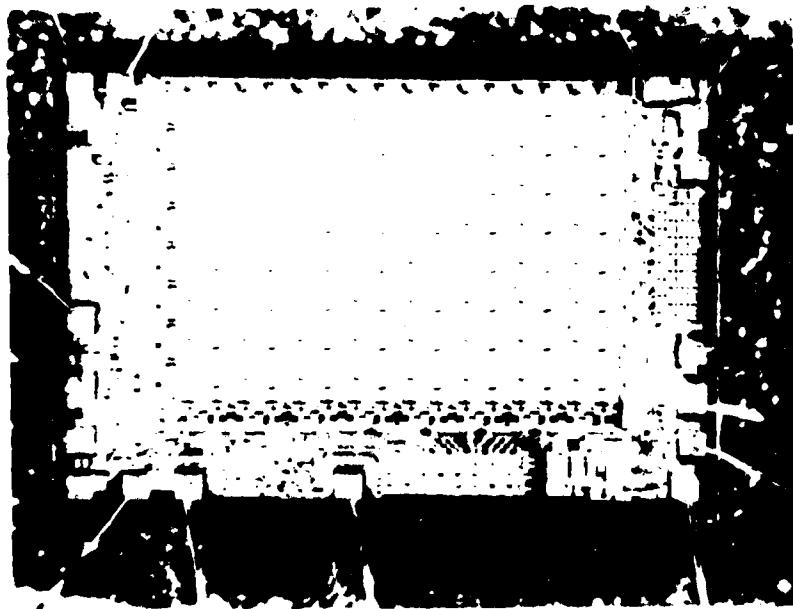


Figure 4: Interior view showing layout of chip.  
Magnification: 30X.

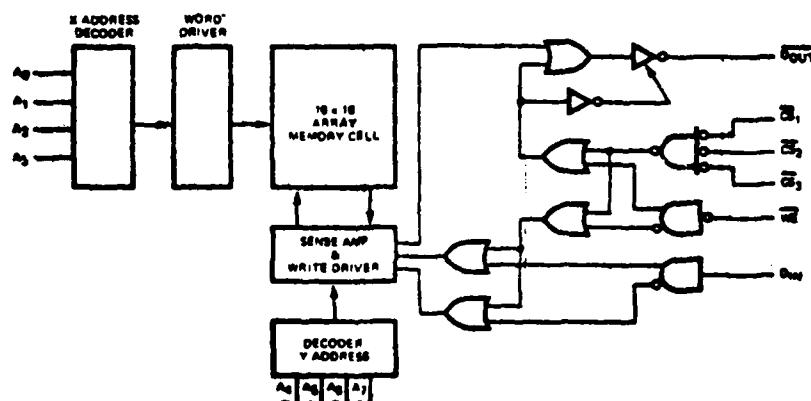


Figure 5: Logic diagram for the device.

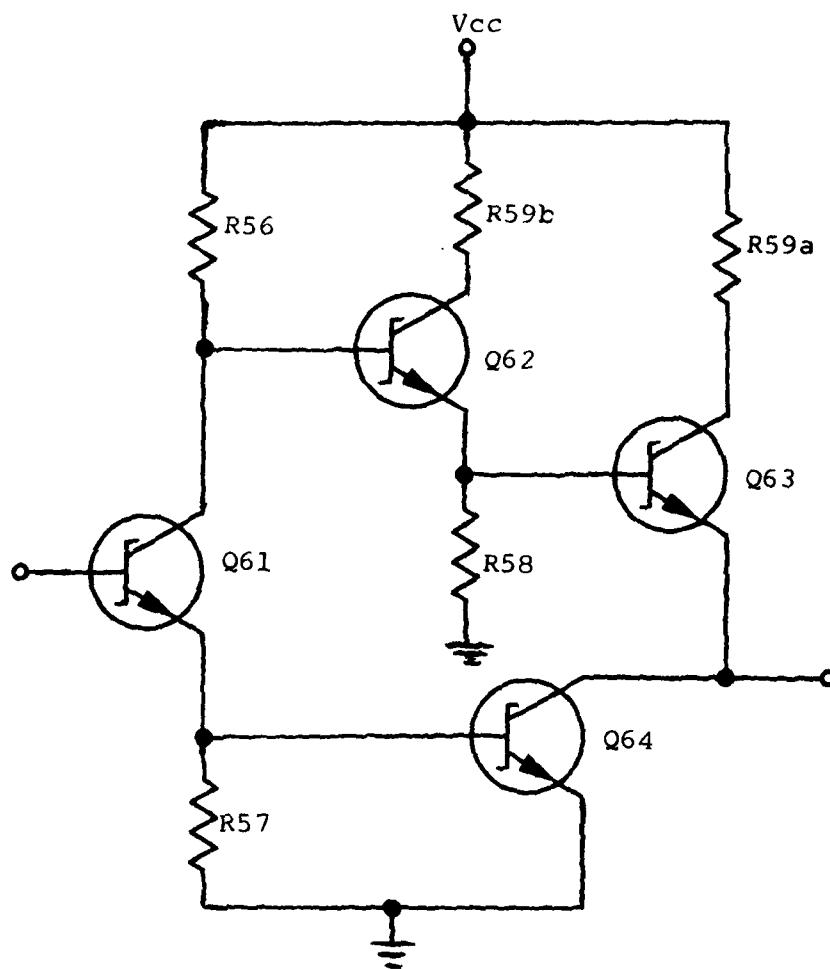


Figure 6A: Schematic for output of device.

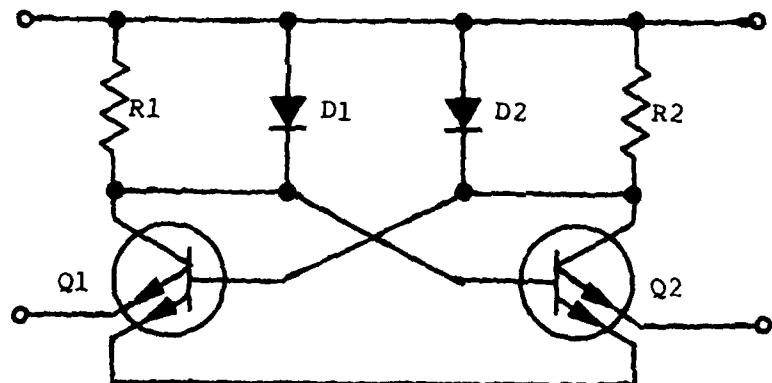


Figure 6B: Schematic for memory cell.

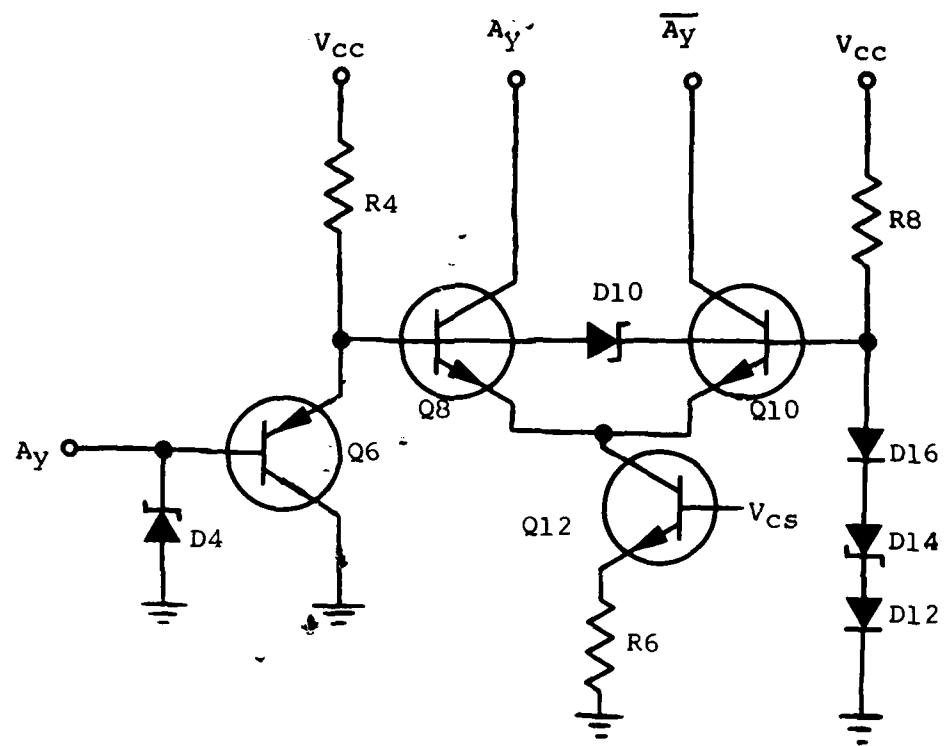
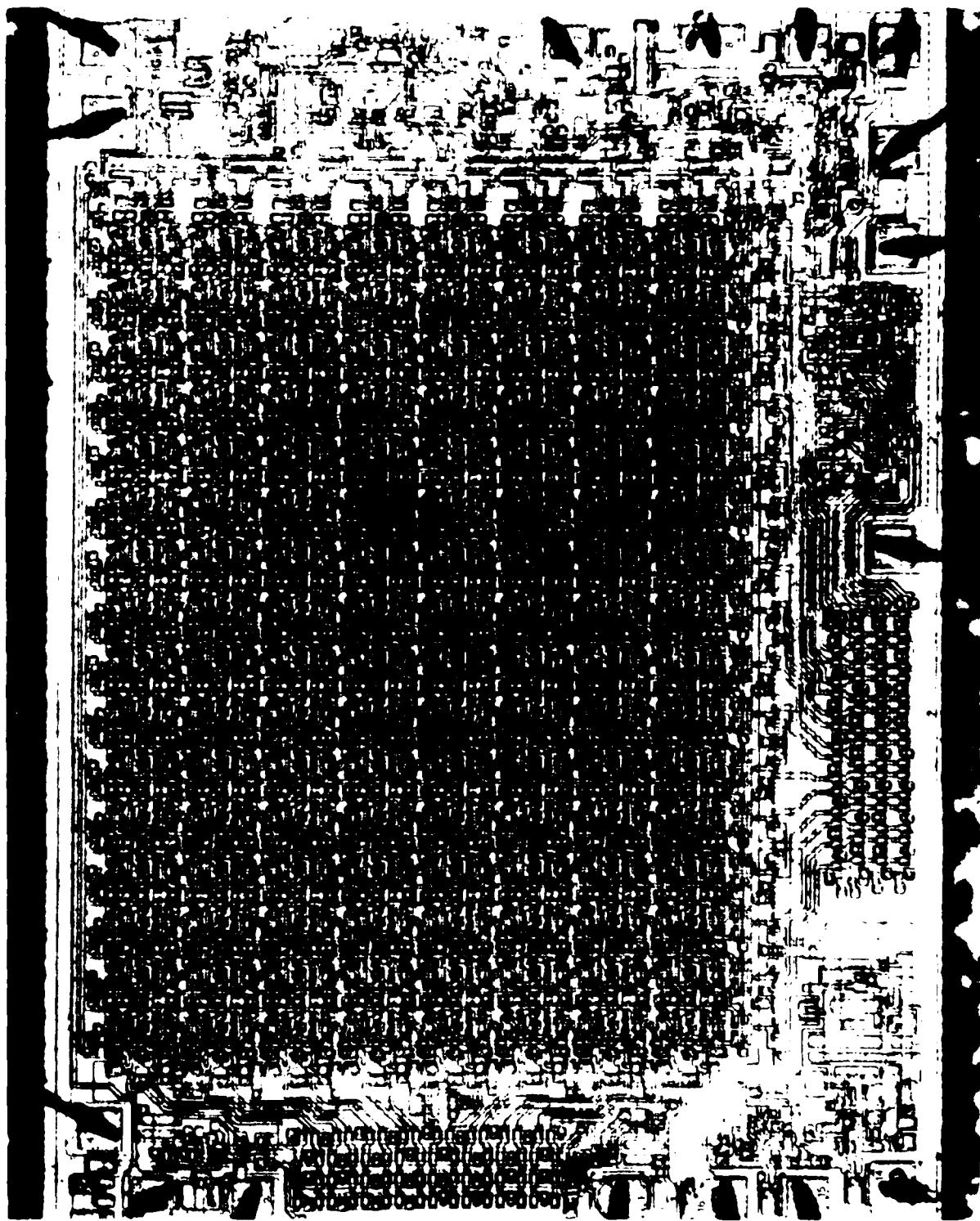


Figure 6C: Schematic for input of device.



100% of the time, the system will be able to identify the  
correct target, and 90% of the time, it will be able to do so  
within 10 seconds of the target appearing in the field of view.

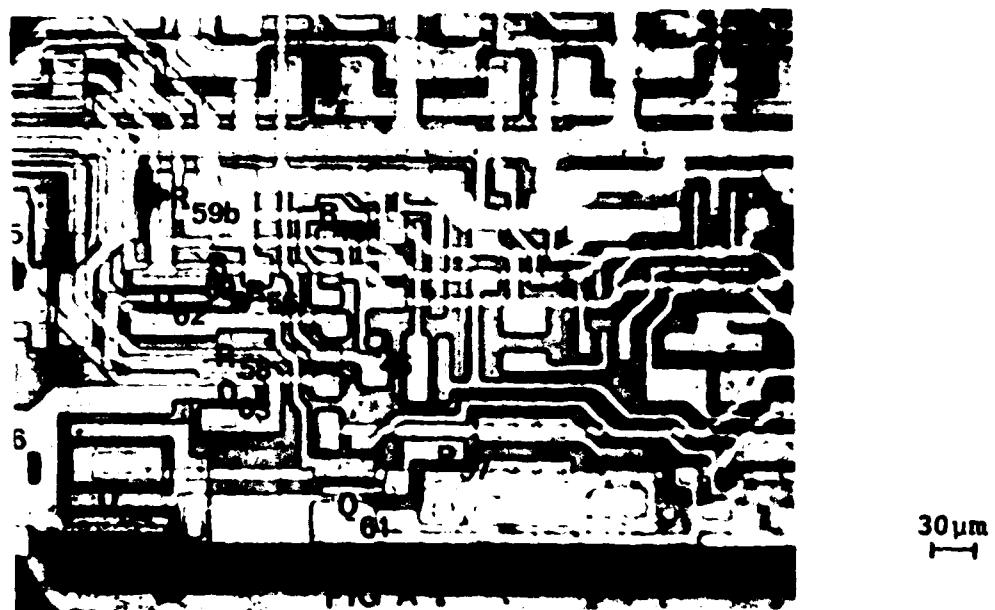


Figure 8A: Photomicrograph of output structure.

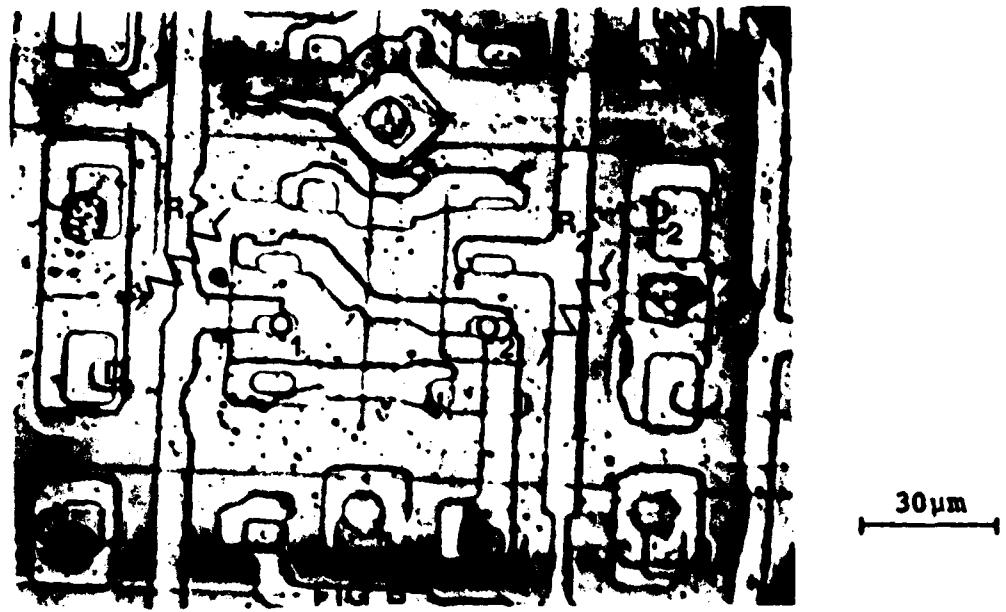
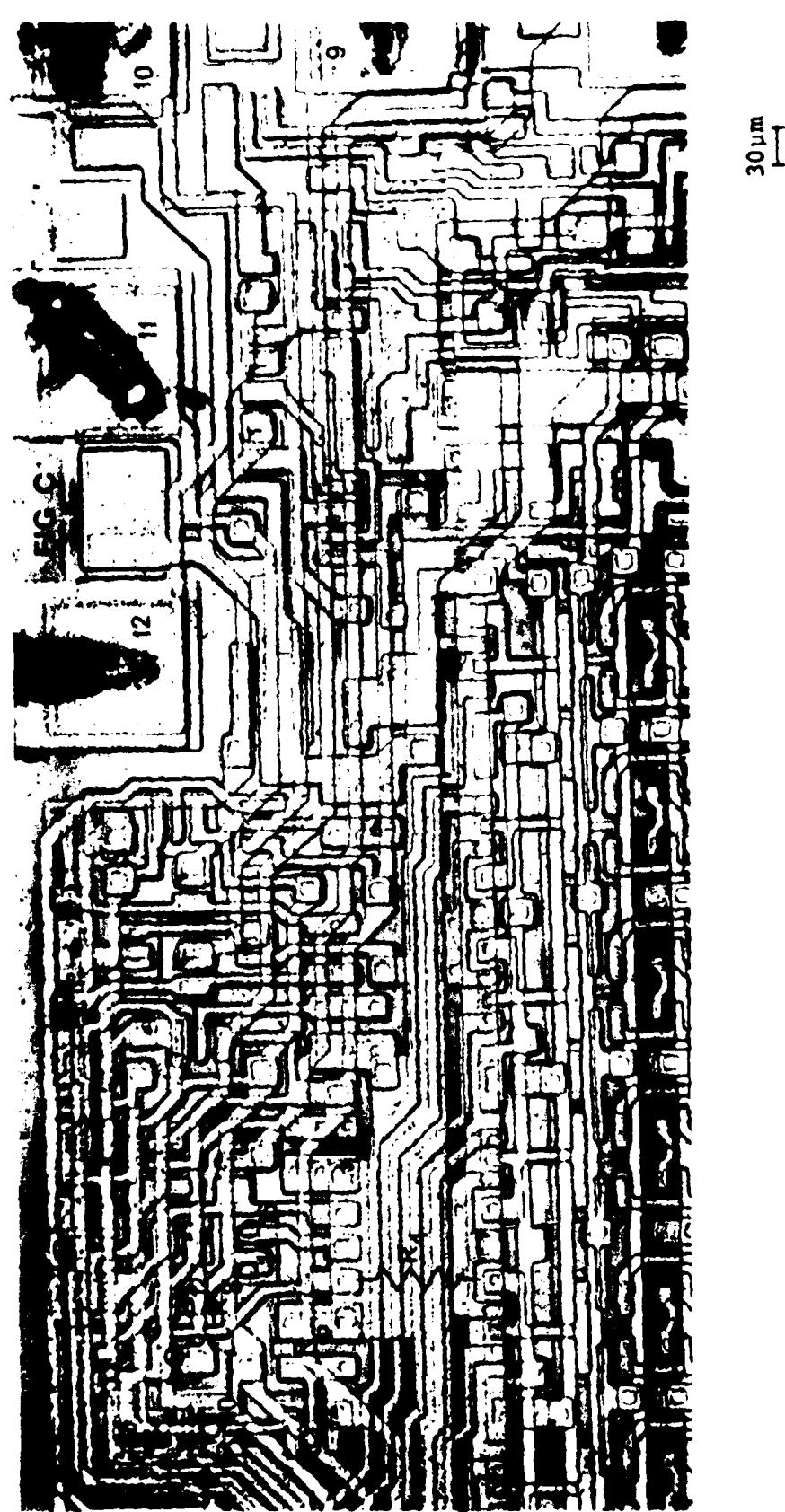


Figure 8B: Photomicrograph of memory cell.



30  $\mu$ m

I-14

Figure 8C: Photomicrograph of input structure.

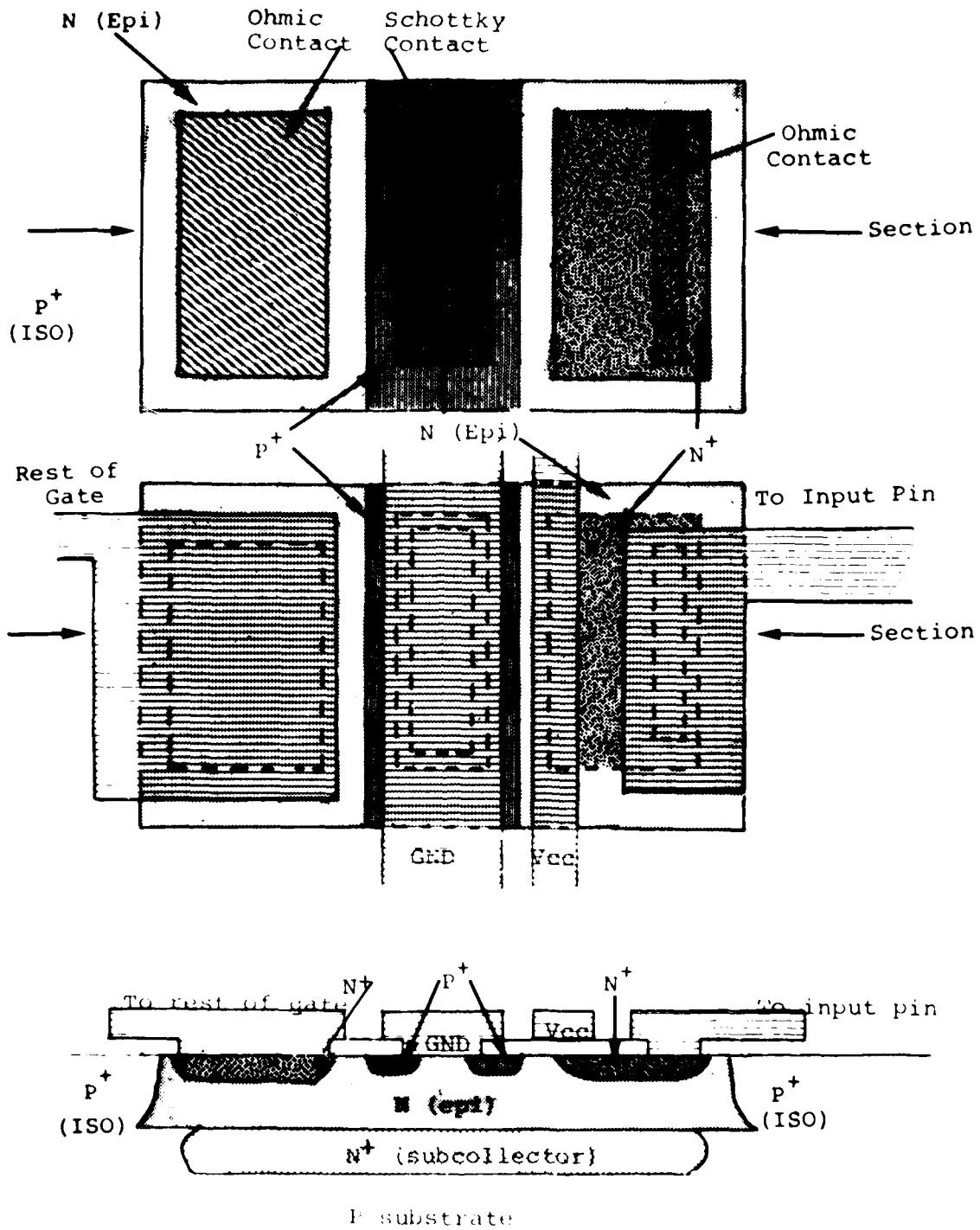


Figure 9. Schematic diagram showing cross-sectional view of input structure (not to scale).

## APPENDIX J

### CONSTRUCTION ANALYSIS OF VENDOR D L5531D

#### STANDARD SCHOTTKY TTL INTEGRATED CIRCUIT IN CERAMIC CHIP

##### Abstract

A Vendor D 256-Bit RAM, L5531D, was subjected to a detailed construction analysis. The device is a fully decoded 256-bit random access memory organized as a 256-word by 1-bit array with an 8-bit address field and separate data in and data out lines. The device has three active low chip select inputs and a three state output. Low power Schottky technology is employed in the device fabrication.

Two devices were received packaged in standard 16 pin ceramic dual-in-line packages (CERDIP's) date coded 7626. The leads were gold plated Kovar with no nickel underplating, which posed a reliability hazard due to the resultant lack of corrosion protection. The lid was gold plated Kovar, with no nickel underplating, so it too was a reliability hazard. The internal wires were 1 mil aluminum, having better than adequate pull-strengths. The chip metallization was vapor deposited Al with no barrier metal between it and the silicon. The absence of the barrier metal in the contact areas allowed for the silicon to diffuse into the aluminum, which would ultimately result in degradation of the Schottky junction, voids in the silicon, and possible shorting. The chip was entirely covered with vapor deposited SiO<sub>2</sub> for scratch protection and passivation. Several foreign particles were present on the chip even after a thorough cleaning.

No other weaknesses in construction or workmanship were noted.

##### Introduction

This analysis was performed as part of an evaluation of this device for Rome Air Development Center (RADC). The analysis was designed to document the construction details and materials used in these units and to identify shortcomings in the design or defects in workmanship, if any.

## Results

### The Package

The units were packaged in 16-lead ceramic dual-in-line packages (CERDIP). The base material was smooth alumina and the lid was gold plated Kovar (no nickel) with a solder seal. The gold plating was measured to be  $3.1 \mu\text{m}$  (120  $\mu\text{inches}$ ) thick. The leads were brazed to the side of the package and consisted of gold plated Kovar, with no nickel underplating. The thickness of the gold plating on the leads was measured to range from  $2.5$  to  $3.8 \mu\text{m}$  (100 to 150  $\mu\text{inches}$ ). Because of the absence of nickel plating, the Kovar base was not adequately protected against corrosion. The package dimensions were found to be within the limits specified in MIL-M-38510D and are shown in Figure 2; the case outline drawing and specification for dimensions are shown in Figure 1. The package markings were as shown in Figure 3.

The internal area of the lead frame which is used for bonding pads for the aluminum wires was  $7.7 \mu\text{m}$  (300  $\mu\text{inches}$ ) thick molybdenum, plated with  $7.7 \mu\text{m}$  (300  $\mu\text{inches}$ ) of gold over  $2.0 \mu\text{m}$  (80  $\mu\text{inches}$ ) of nickel.

### The Chip

The lid was removed by applying a hot soldering iron to it and forcing a chisel edge into the seal in a controlled manner until the lid slid off. An overall view of the chip is shown in Figure 4. The chip was measured to be  $2.40 \times 2.80 \times 3.08 \text{ mm}$  ( $94.5 \times 110.2 \times 15.0 \text{ mils}$ ). The volume of the cavity was  $0.035 \text{ cm}^3$ . The chip was mounted using a silicon-gold eutectic approximately  $3.0 \mu\text{m}$  (0.12 mils) thick with a thick film gold paste providing the gold. An underplating of nickel  $1.7 \mu\text{m}$  (67  $\mu\text{inches}$ ) thick was plated onto a base metallization of molybdenum  $6.7 \mu\text{m}$  (263  $\mu\text{inches}$ ) which provided the adhesion to the ceramic. This metallization scheme is seen in cross-section in Figure 5. Also shown is a void under one corner of the chip, but it is not large enough to cause it to be a reject. Thermal resistances were measured to be  $\theta_{\text{junction-to-air}} = 106.2^\circ\text{C/W}$  and  $\theta_{\text{junction-to-case}} = 11.1^\circ\text{C/W}$ .

The internal wires were ultrasonically bonded, 1 mil diameter aluminum. Microbond-pull testing of 8 of the 16 wires yielded a range in pull-strength from 4.5 to 5.0 grams-force, with an average of 4.6. These wires exceed the minimum pull-strength of 2.0 gm-f specified in MIL-STD-883B, Method 2011.2. No fracture occurred at the bond itself, and no bond defects were noted.

### The Chip (continued)

The chip metallization was a single level interconnection scheme which used aluminum  $1.3 \mu\text{m}$  (51.2  $\mu\text{inches}$ ) thick over Ti-W approximately  $5,000 \text{ \AA}$  thick. The presence of the Ti-W layer provides good adhesion to the Si and  $\text{SiO}_2$ , and is a diffusion barrier to the aluminum. The platinum-silicide in the contact areas gives good contact for base (P) and emitter ( $N^+$ ) diffusions and Schottky barrier contacts for collectors ('N). The above thicknesses were measured in an angle cross-section. The aluminum layer was vapor deposited and the Ti-W was sputter deposited in an undisclosed ratio. The  $\text{Pt}_x\text{Si}_y$  is formed in the contact areas, followed by blanket etching to remove the Pt elsewhere. A glass layer ( $\text{SiO}_2$ , no phosphorous) about  $1.7 \mu\text{m}$  (67  $\mu\text{inches}$ ) thick covered the entire chip as passivation and protection against scratching during handling.

The highest current density was found to exist in the emitter metallization run of Q30. Here the current is  $12\text{mA}$  maximum and the smallest metallization width is  $2.3 \times 10^{-3} \text{ cm}$ . The metallization thickness of  $1.3 \times 10^{-4} \text{ cm}$  results in a minimum cross-sectional area of  $3.0 \times 10^{-7} \text{ cm}^2$  which yields a maximum current density of  $4.0 \times 10^4 \text{ A/cm}^2$ . Over an oxide step, the current density could reach  $6.0 \times 10^4 \text{ A/cm}^2$ , since the metallization thins to about  $2/3$  its thickness as it goes over an oxide step. This is within the specification of  $5 \times 10^5 \text{ A/cm}^2$  found in MIL-M-38510 as a maximum current density for Al to avoid an unacceptable level of electromigration failures.

The chip was photographed and mapped to identify the components. Figure 6 shows the logic layout of the device, and Figure 7 shows the detailed schematic of the device. Note that the inputs are pnp transistors, the base-emitter junctions of which replace the commonly used input diodes. Figure 8 shows the chip with regions labelled corresponding to those given in greater detail in Figure 9. The components are labelled corresponding to the schematic symb's given in Figure 7.

Visual inspection of the chip was performed using Method 2010.3 of MIL-STD-883B as a guide. The only workmanship weakness found was the presence of several foreign particles on the surface of the chip. These particles remained even after a thorough cleaning of the chip. While they were not seen as a reliability hazard, they did indicate that the vendor's inspection procedures need reviewing.

### The Components

The substrate was P-type. Subcollectors approximately  $6.7 \mu\text{m}$  (0.26 mils) deep, consisting of low resistivity N-type diffusions, were made in positions corresponding to the transistors prior to the growth of the epitaxial layer. These provided high conductivity paths from the vicinity of the base-collector junctions to the collector contact diffusions. An N-type epitaxy about  $3.3 \mu\text{m}$  (0.13 mils) thick was then grown.

### The Components (continued)

After the growth of the epitaxial layer, diffusions approximately  $3.3 \mu\text{m}$  (0.13 mil) were made, partitioning the epitaxial layer into individual regions and other components. The P-type base diffusion resistors were also made at this time. This diffusion was measured to be about  $1.5 \mu\text{m}$  (59  $\mu\text{inches}$ ) deep. This also created the p-n junction guard rings for the input clamping diode to be discussed later. The N<sup>+</sup> type diffusion, measured to be about  $1.0 \mu\text{m}$  (39  $\mu\text{inches}$ ) deep, then created the emitters and the collector contact enhancement regions. This latter was necessary to achieve ohmic contact to the low-doped epitaxial layer.

### The Transistors

All but 28 of the transistors utilized the Schottky design. The base regions of these Schottky transistors were annular, having a rectangular "hole" within a rectangular shaped diffusion. Hence, a portion of the epitaxial region at the surface was surrounded by this annular ring. The contact hole in the base oxide exposed both part of the base region and all of the epitaxial region which was surrounded by the base ring. This latter was part of the collector. When the metallization was deposited within the contact hole, it created the Schottky diode between base and collector. This occurred because of the relative doping level of the base region (high doping yields ohmic contact) versus that of the epitaxial (collector) region (low doping yields rectifying Schottky contact). The 28 transistors mentioned above as exceptions from this design were of standard bipolar construction.

### The Diodes

Each input had a Schottky barrier diode to ground to provide protection for the input against voltage spikes. The construction was quite similar to that in the transistors, forming what was actually a p-n junction - Schottky barrier hybrid diode. A cross-sectional diagram (not to scale) of the construction of the input structure is shown in Figure 10. References 1 and 2 describe the theory and advantages of such a structure.

### The Resistors

P-type base diffusion was used for all of the resistors. This diffusion had a resistivity of about  $1,000 \Omega/\square$ . This sheet resistance was obtained by counting squares and comparing to values provided by the vendor. The diffusion depth was measured to be about  $1.5 \mu\text{m}$  (59  $\mu\text{inches}$ ).

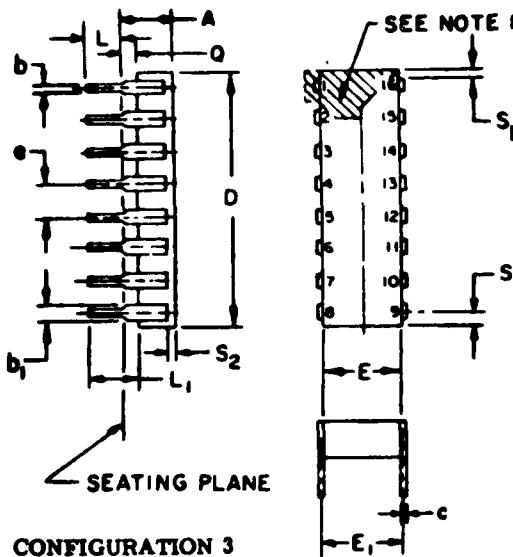
### Conclusions and Recommendations

In performing a construction analysis of Vendor D's L5531D, two potential reliability hazards were identified. Several foreign particles were noted which could not be removed with cleaning. A review of the vendor's inspection procedures is recommended. Also, plating analysis on the leads and lid revealed adequate gold plating, but no nickel underplating. It is recommended that the vendor's plating procedures be revised to include an electrolytic low stress nickel underplating. The chip metallization was single level aluminum, with no barrier metal between it and the silicon. This is seen as a reliability hazard, as the absence of a barrier metal in the contact areas allows for diffusion of the silicon into the aluminum, resulting in voids in the silicon, degradation of the Schottky junctions, and shorting. No other weaknesses in construction or workmanship were noted.

### References:

1. RADC-TR-292, Reliability Evaluation of Schottky Barrier Diode Microcircuits, Raytheon Company, Sept. 1976, Appendix B, P. 158.
2. R. A. Zettler and A. M. Cowley, "p-n Junction-Schottky Barrier Hybrid Diode" IEEE Transactions on E.D., Vol. ED-61, No. 1, January 1969.
3. R. S. Buritz, A. Fafarman, R. F. McGowen, and S. L. Webster, "Investigation of Microcircuit Surface Metallurgy", EEC Elec. Comp., 1969.

THIS PAGE IS BEST QUALITY PRACTICAL  
PRINTED ON 100% QUALITY PRACTICAL



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		.200		5.08	
b	.014	.023	.36	.58	8
b1	.030	.070	.76	1.78	2, 8
c	.008	.015	.20	.38	8
D	.040			1.04	4
E	.220	.310	5.59	7.87	4
E1	.290	.320	7.37	8.13	7
E2	.100		2.54		
E3	.050		1.27		
e	.100 BSC		2.54 BSC		5.9
L	.125	.200	3.18	5.08	
L1	.150		3.81		
Q	.015	.060	.38	1.02	3
Q1	.020		.51		
S		.080		2.03	6
S1	.005		.13		6
S2	.005		.13		
a	0°	15°	0°	15°	

**NOTES:**

- Index area; a notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
- The minimum limit for dimension  $b_1$  may be .020 (.51 mm) for leads number 1, 8, 9 and 16 only.
- Dimension Q shall be measured from the seating plane to the base plane.
- This dimension allows for off-center lid, meniscus and glass overrun.
- The basic pin spacing is .100 (2.54 mm) between centerlines. Each pin centerline shall be located within  $\pm 0.010$  (.25 mm) of its exact longitudinal position relative to pins 1 and 16.
- Applies to all four corners (leads number 1, 8, 9, and 16), and 40.5 shall apply.
- Lead center when  $a$  is 0.  $E_1$  shall be measured at the centerline of the leads (see 40.4 of this appendix).
- All leads - Increase maximum limit by .003 (.08 mm) measured at the center of the flat, when lead finish A is applied.
- Fourteen spaces.
- If this configuration is used, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.

**Figure 1:** Package outline and dimensions specified for 16-lead ceramic dual-in-line package (CERDIP).

Figure 2: Package Dimensions

<u>Designation</u>	<u>Measured Value</u>
A	2.1 (0.083)
b	0.45 (0.018)
b <sub>1</sub>	1.45 (0.055)
e	0.3 (0.012)
D	19.9 (0.78)
E	7.1 (0.28)
E <sub>1</sub>	7.6 (0.30)
E <sub>2</sub>	- -
E <sub>3</sub>	- -
e	2.6 (0.10)
L	3.2 (0.12)
L <sub>1</sub>	4.5 (0.18)
Q	1.3 (0.05)
Q <sub>1</sub>	- -
S	1.25 (0.05)
S <sub>1</sub>	1.0 (0.04)
S <sub>2</sub>	0.8 (0.03)

Note: Values outside parentheses are in millimeters.  
Values within parentheses are in inches.



Figure 3: External view  
showing package  
workings of device  
as received.  
Magnification: 3X.

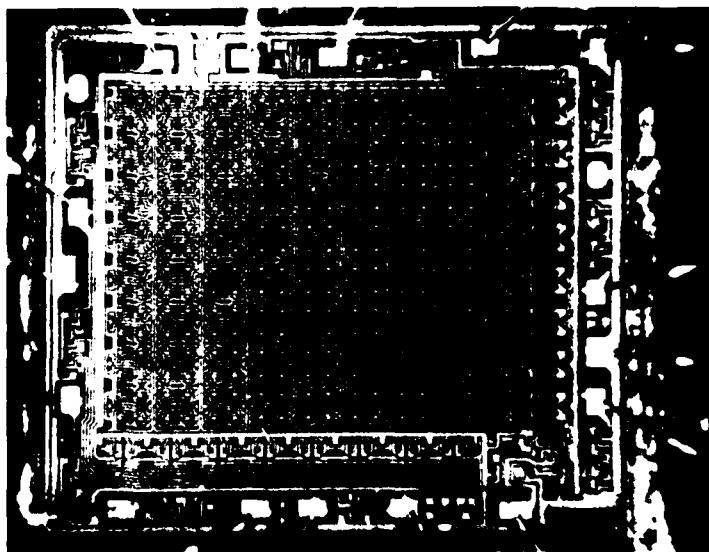
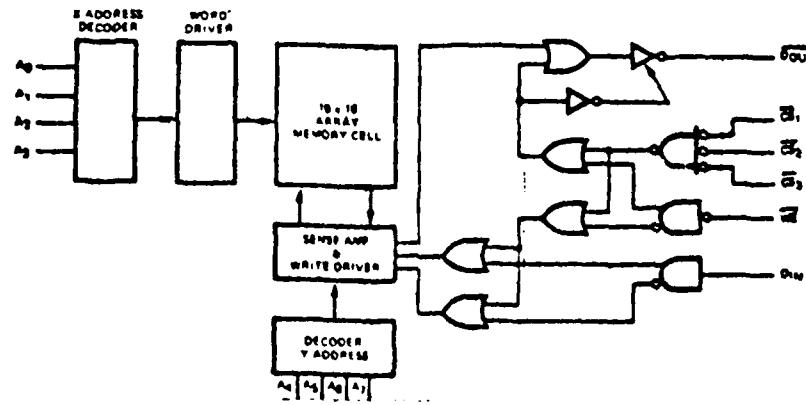


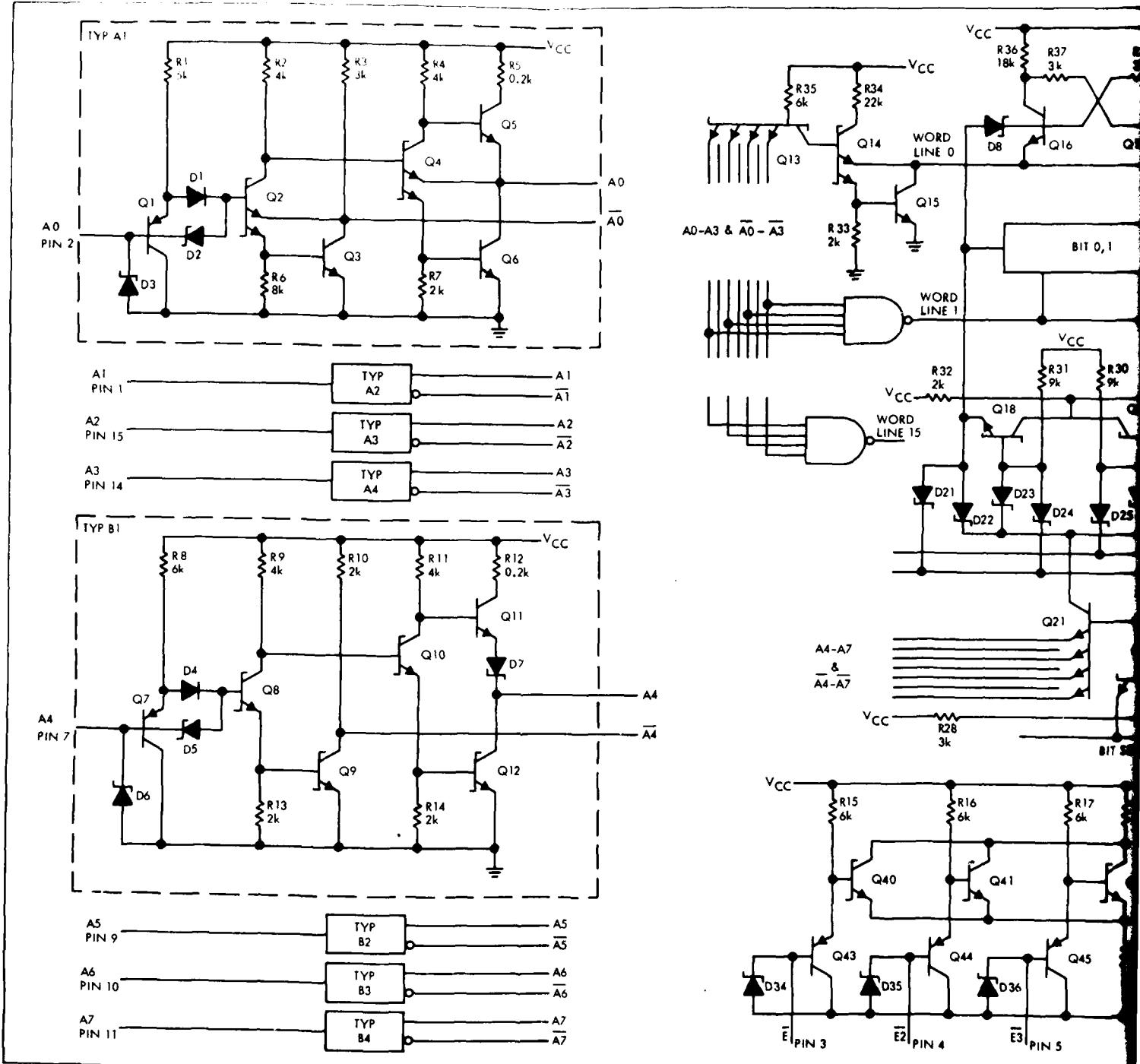
Figure 4: Interior  
view showing layout  
of chip. Mag: 35X.



**Figure 5:** Cross-sectional view of die attach area showing Au/Ni/Moly metallization scheme and void under one corner of chip.  
Magnification: 200X.



**Figure 6:** Logic diagram for the device.



J-10

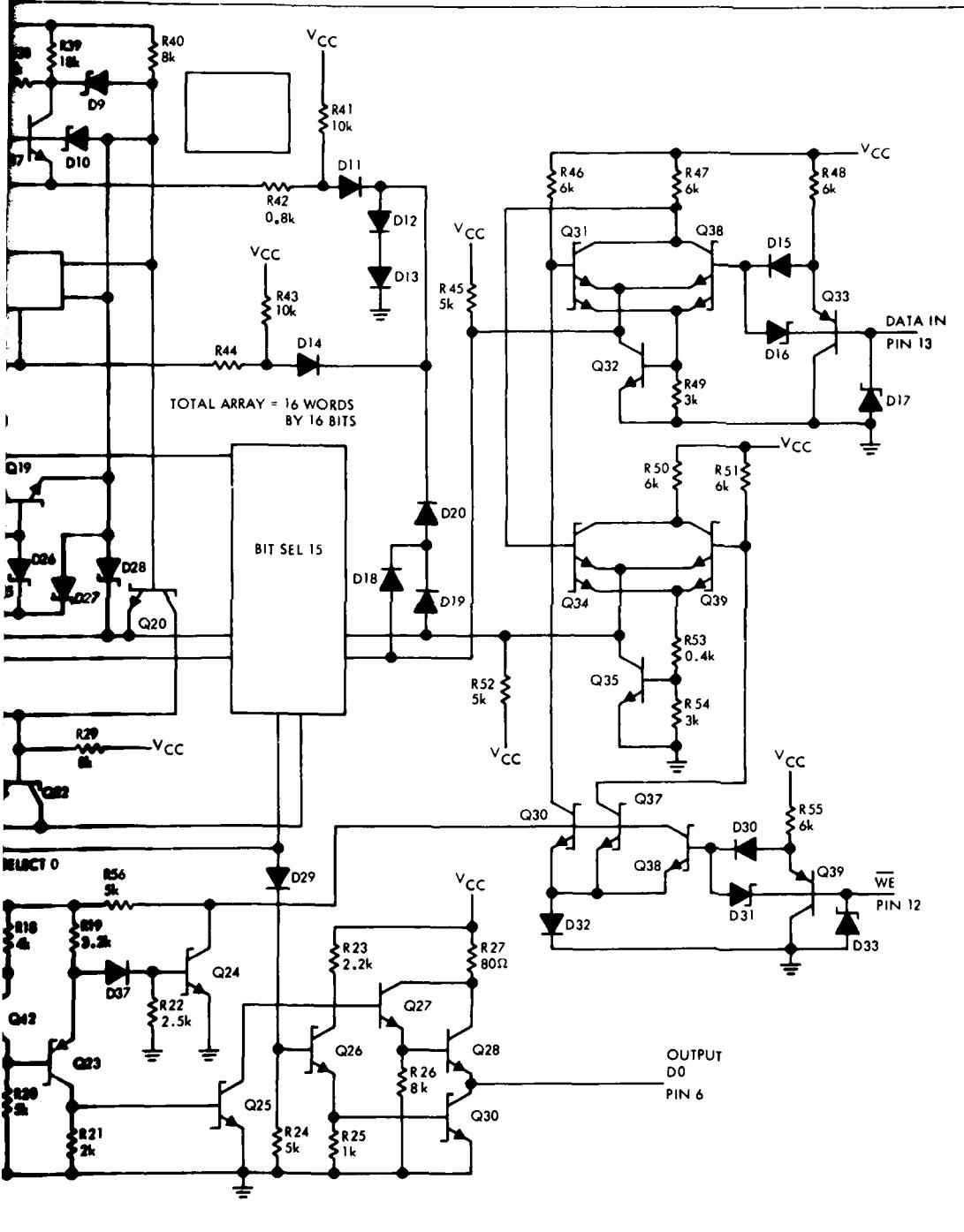


Figure 7: Detailed schematic of the device.

THIS PAGE IS NOT QUALITY PRACTICABLE  
FROM COPY 11. 11/20/60

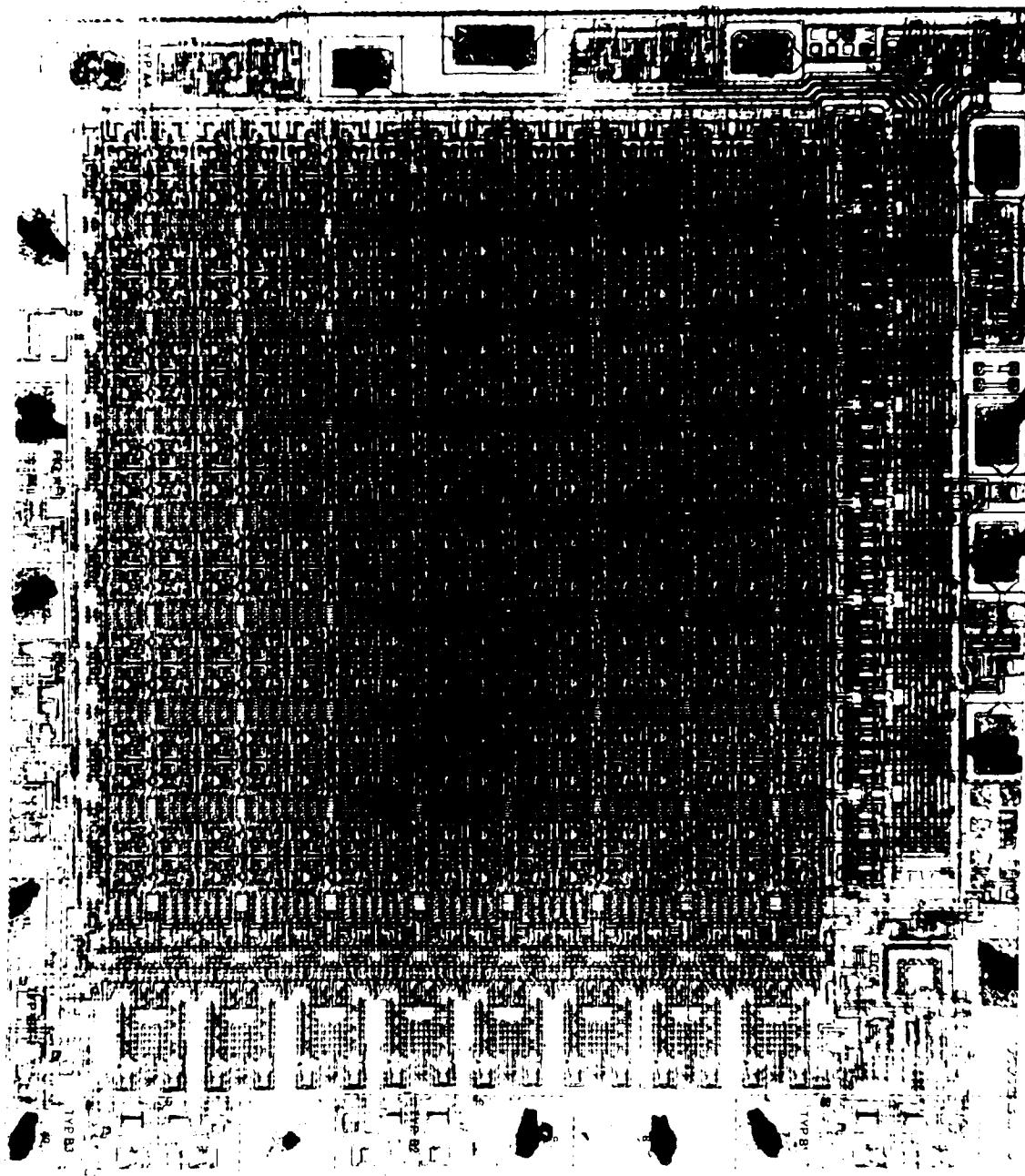
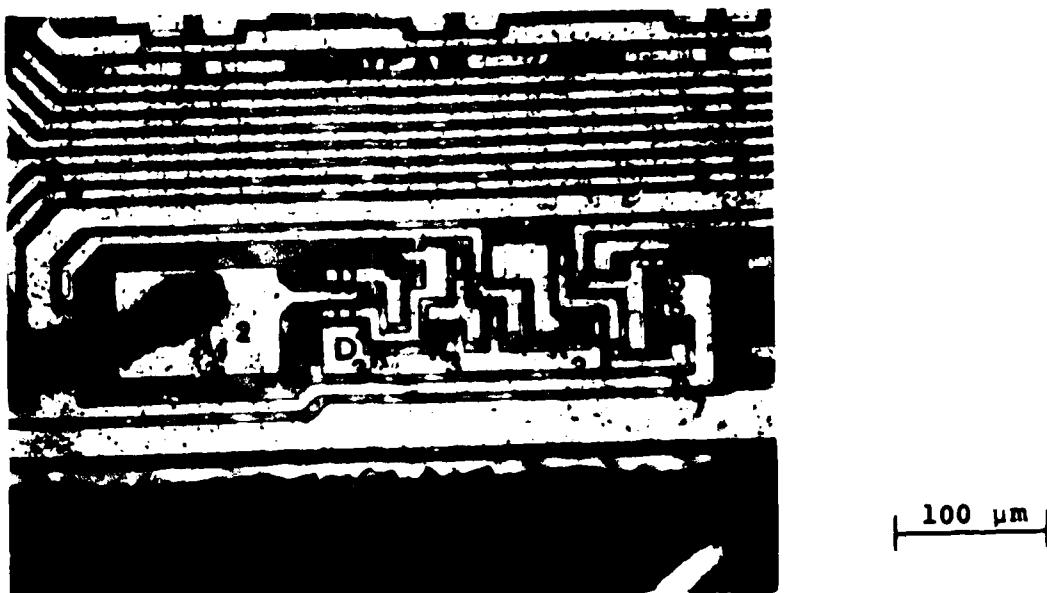
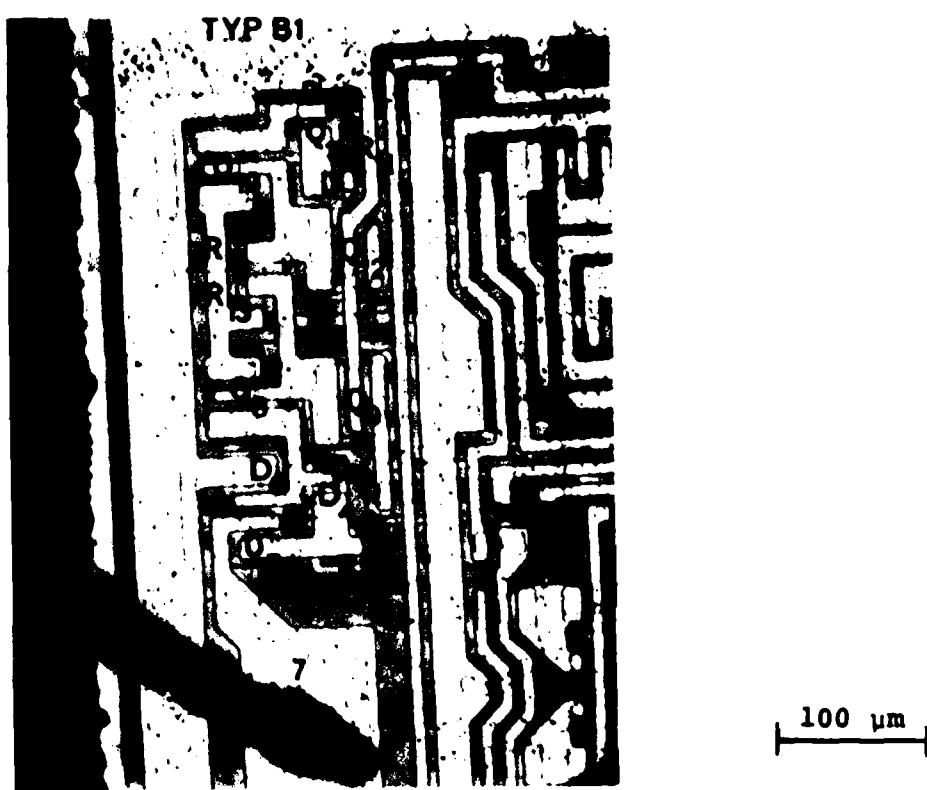


Figure 8. Photomicrograph of the chip showing regions given in greater detail in Figure 9. Magnification: 100X.



100  $\mu\text{m}$



100  $\mu\text{m}$

Figure 9: The two typical input structures corresponding to regions TYP A1 and TYP B1 of Figure 7.

THIS PAGE IS BEST QUALITY PRACTICABLE  
FROM COPY FURNISHED TO DDC

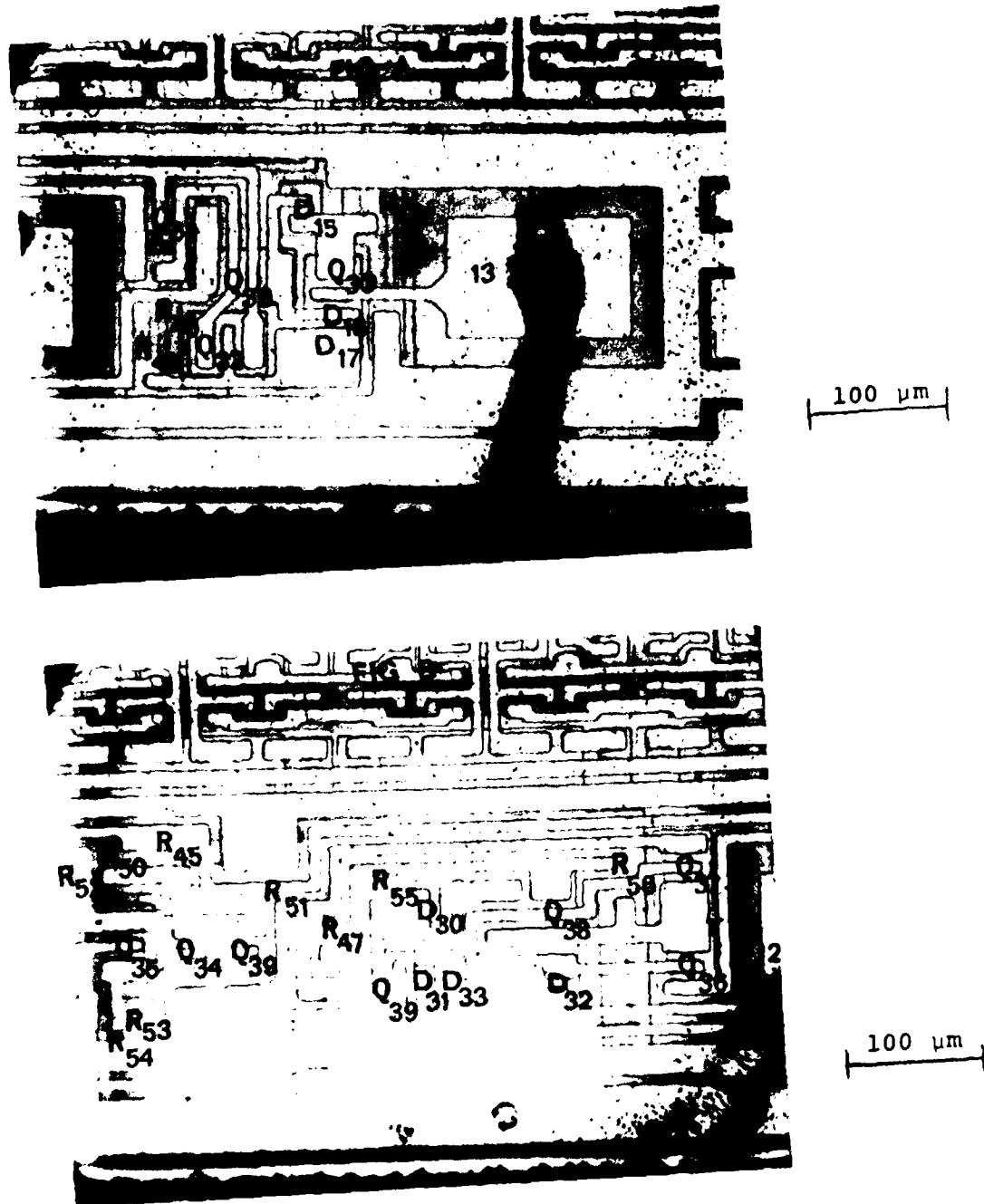


Figure 9 (cont'd): Detailed photomicrographs showing sections A and B corresponding to designations in Figure 8. Schematic symbols correspond to those in Figure 7.

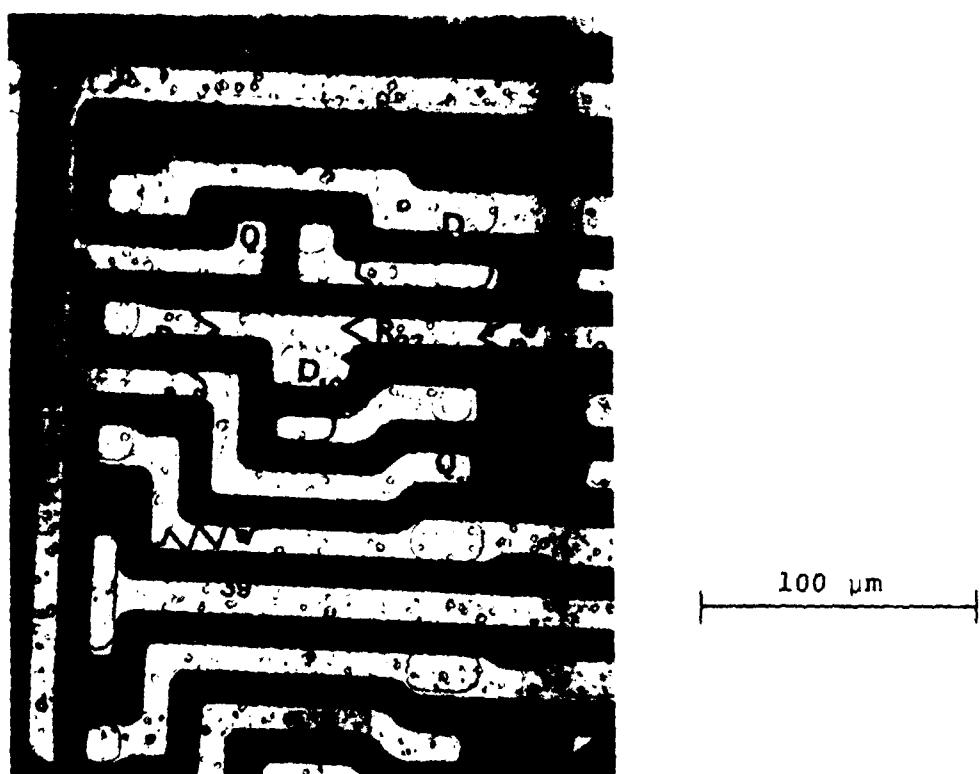
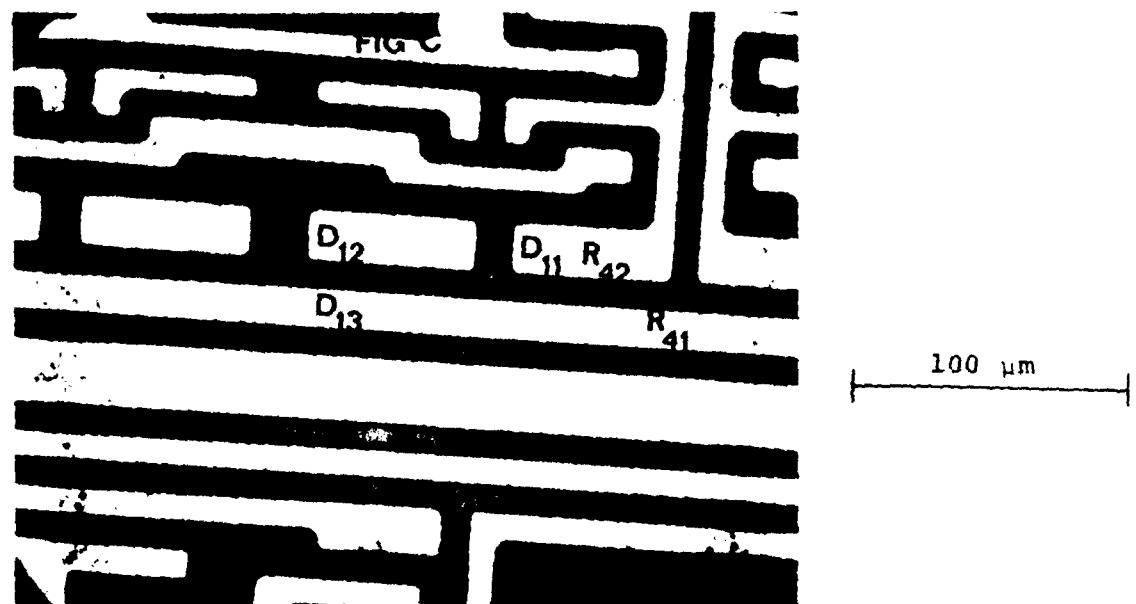


Figure 9 (cont'd) : Detailed photomicrographs showing sections C and D corresponding to designations in Figure 8. Schematic symbols correspond to those in Figure 7.

THEORY AND PRACTICALITY PRACTICABLE

FROM CIRCUIT TO CIRCUIT

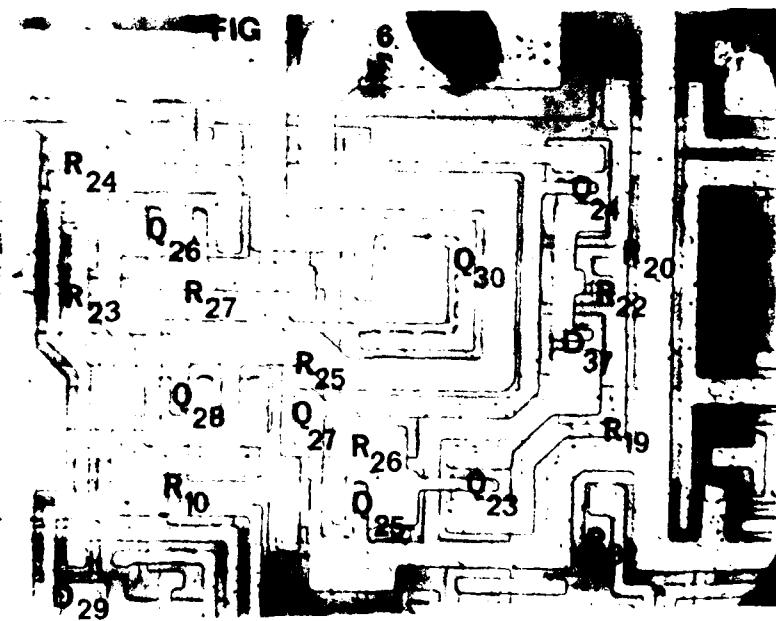
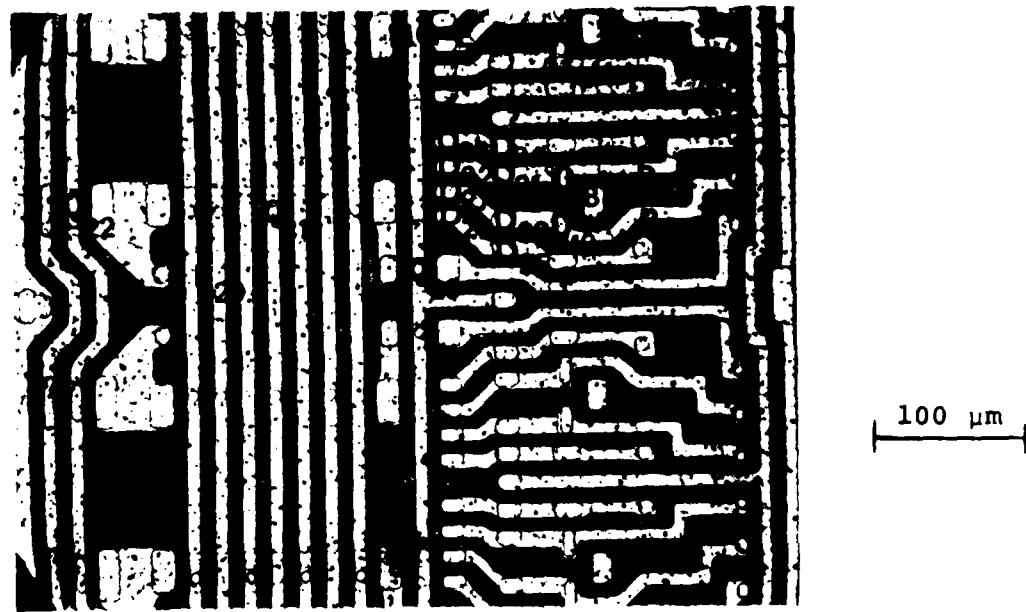


Figure 9 (Cont'd): Detailed photomicrographs showing sections E and F corresponding to designations in Figure 8. Schematic symbols correspond to those in Figure 7.

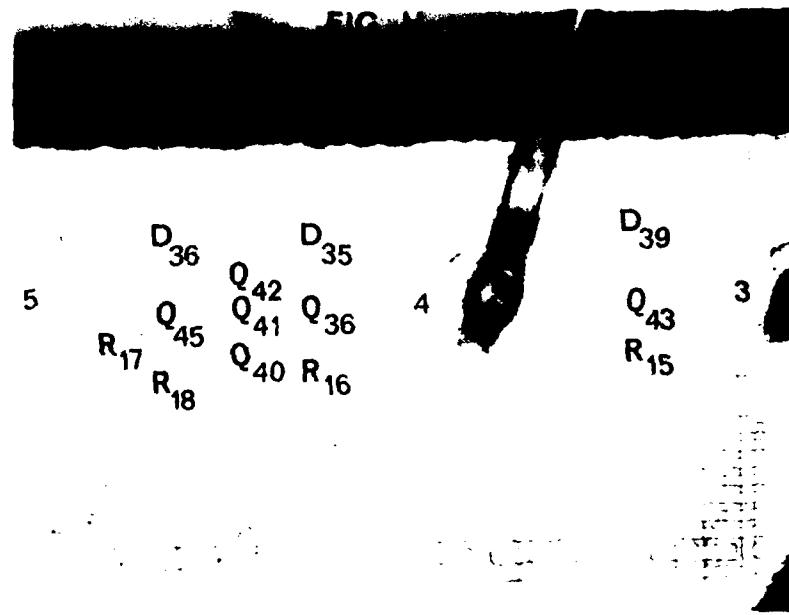
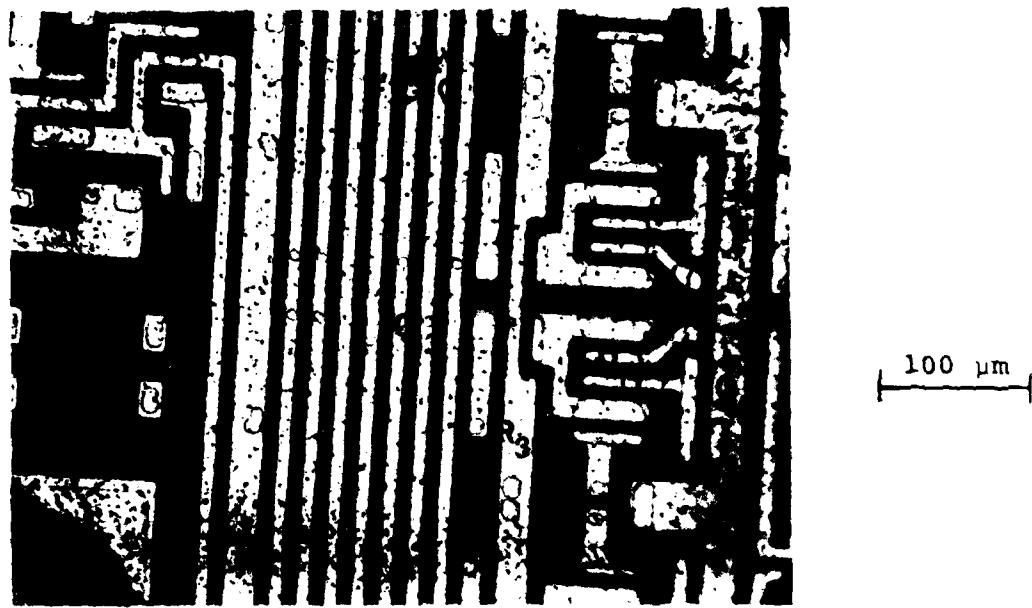


Figure 9 (Cont'd): Detailed photomicrographs showing sections G and H corresponding to designations in Figure 8. Schematic symbols correspond to those in Figure 7.

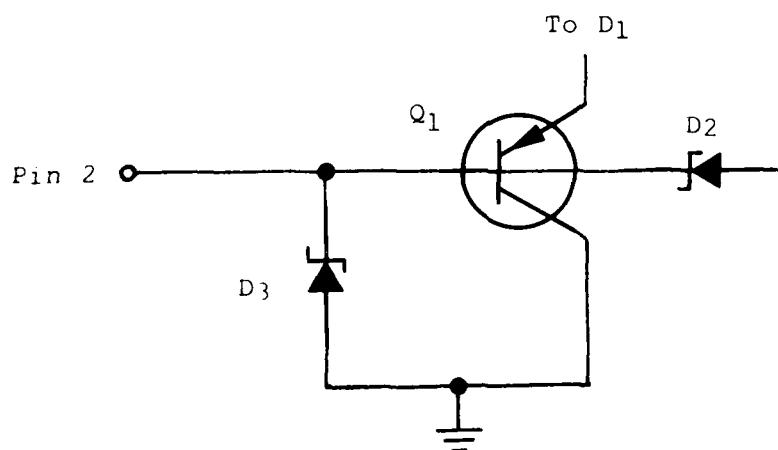
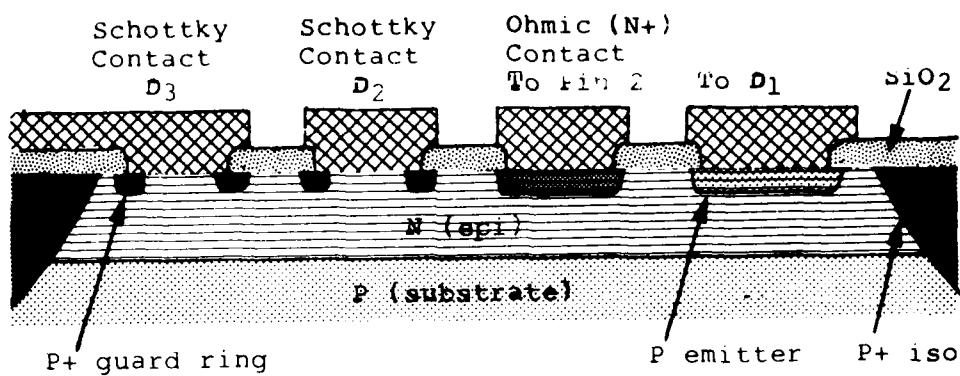
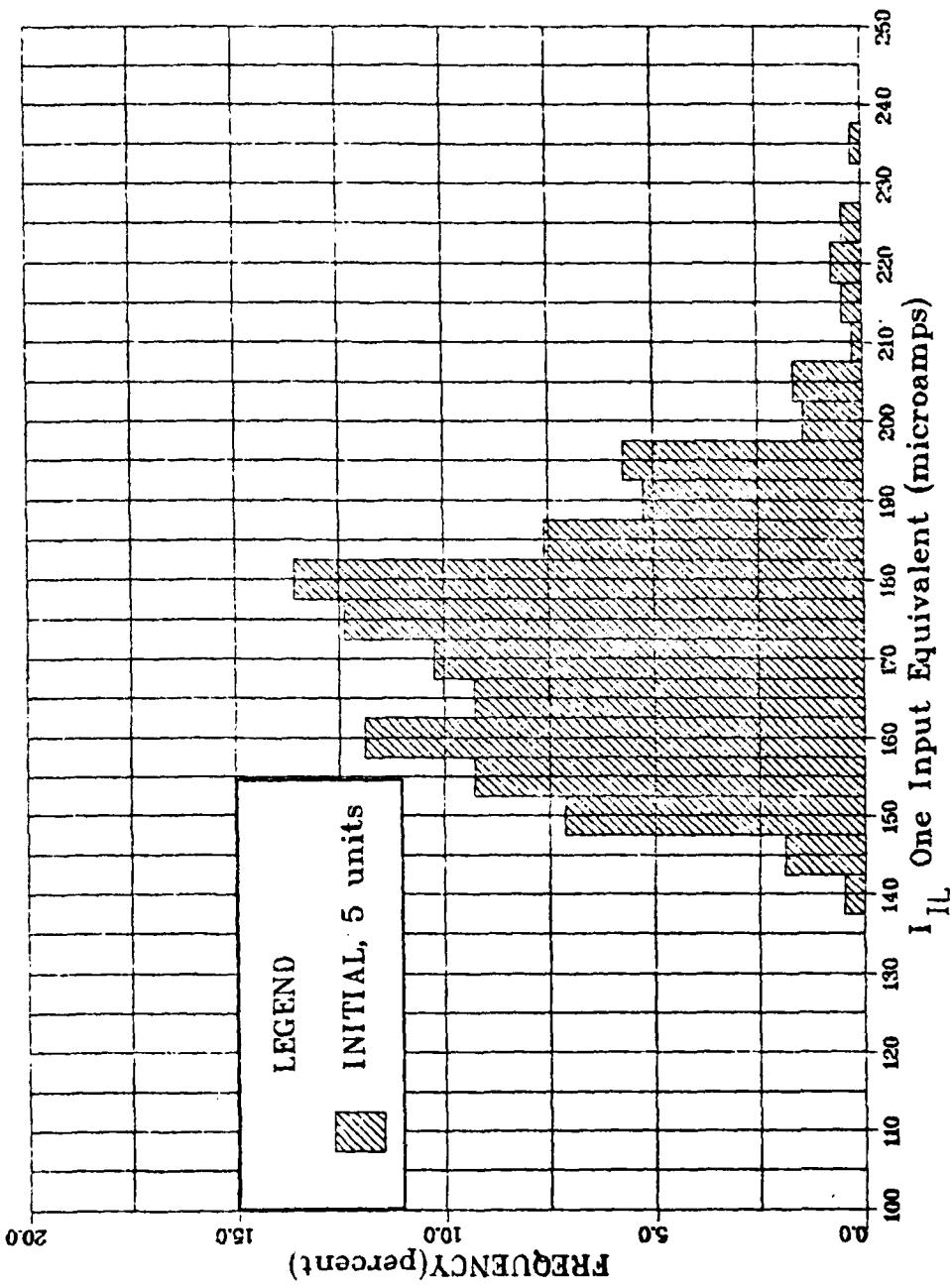


Figure 10: Schematic diagram showing cross-sectional view of input structure (not to scale).

## Low-Level Input Current Distribution

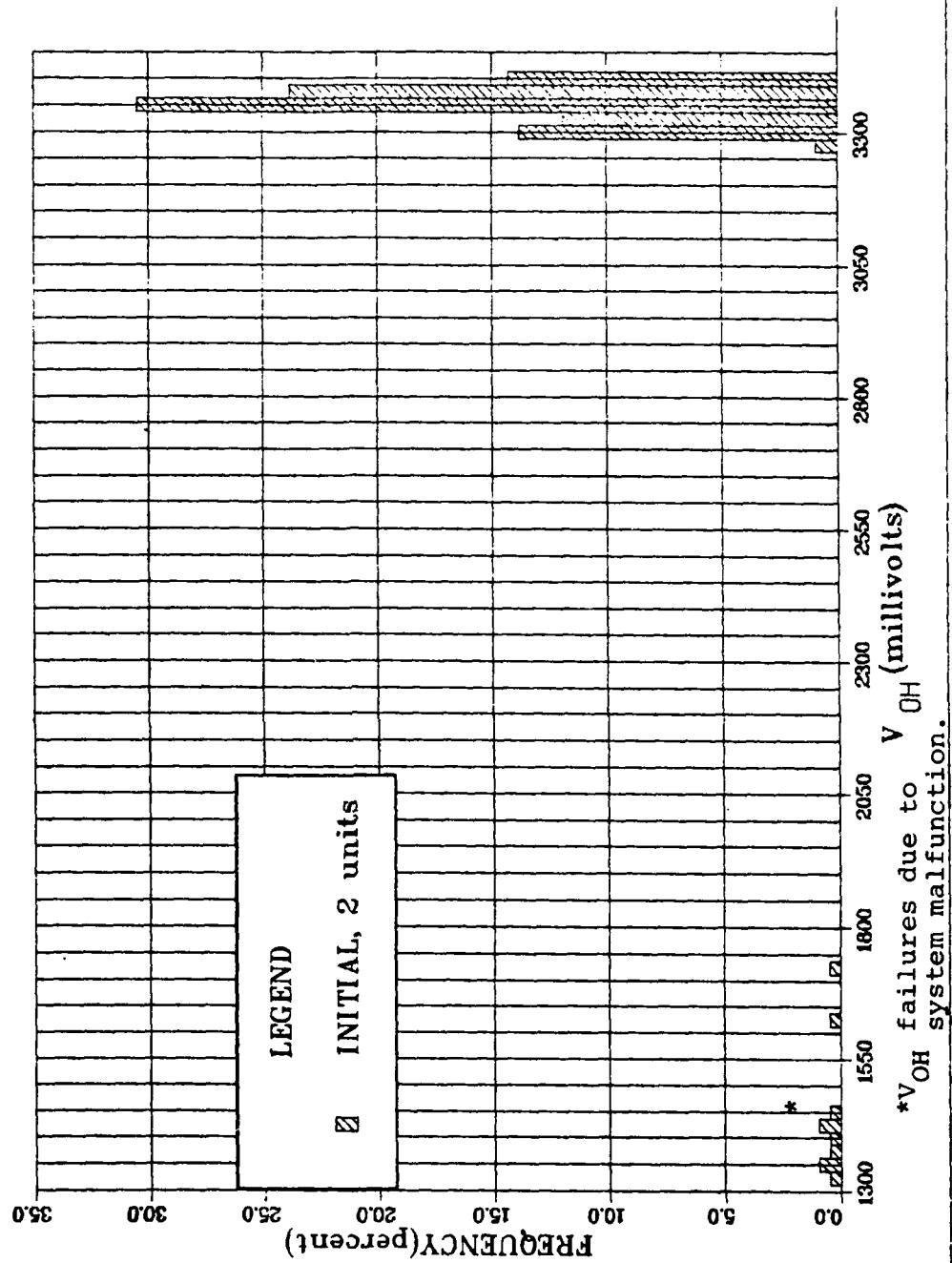
(Normalized)

Vendor A 54LS181  
All Inputs at +125°C



## High-Level Voltage Distribution

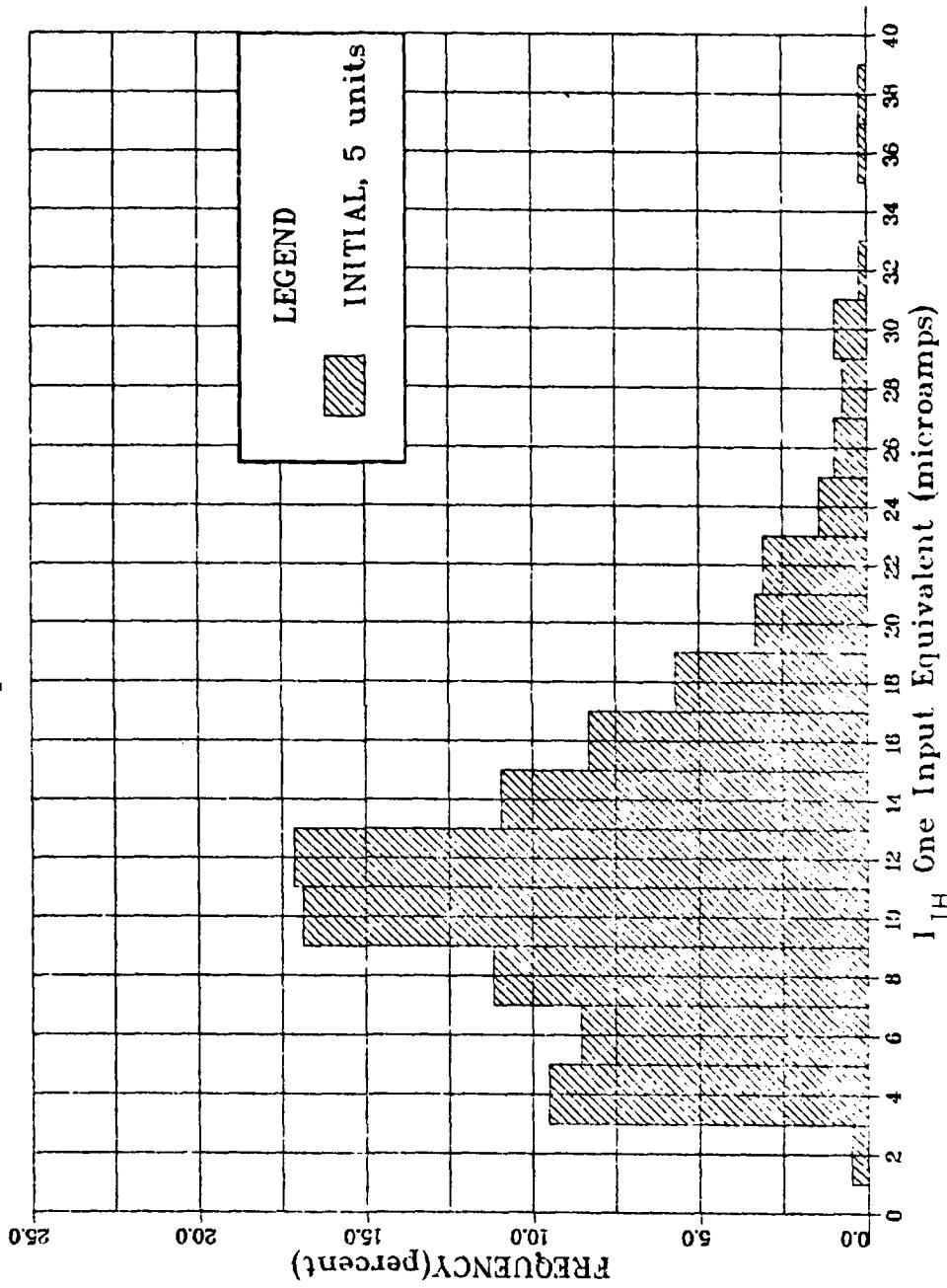
Vendor A 54LS181  
All Outputs at +125°C



\*V<sub>OH</sub> failures due to system malfunction.

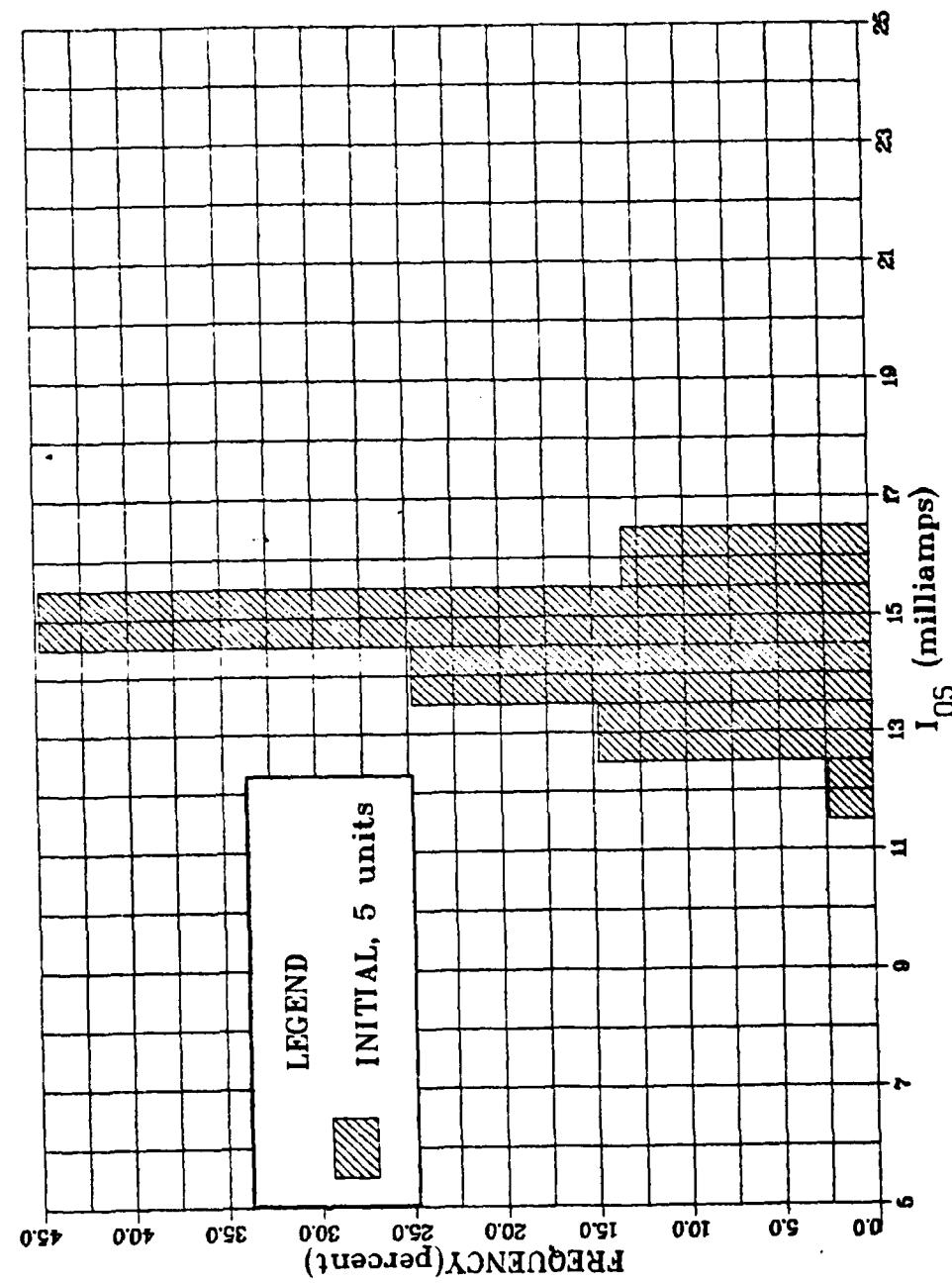
## High-Level Input Current Distribution

(Normalized)  
Vendor B 54LS181  
All Inputs at +125°C



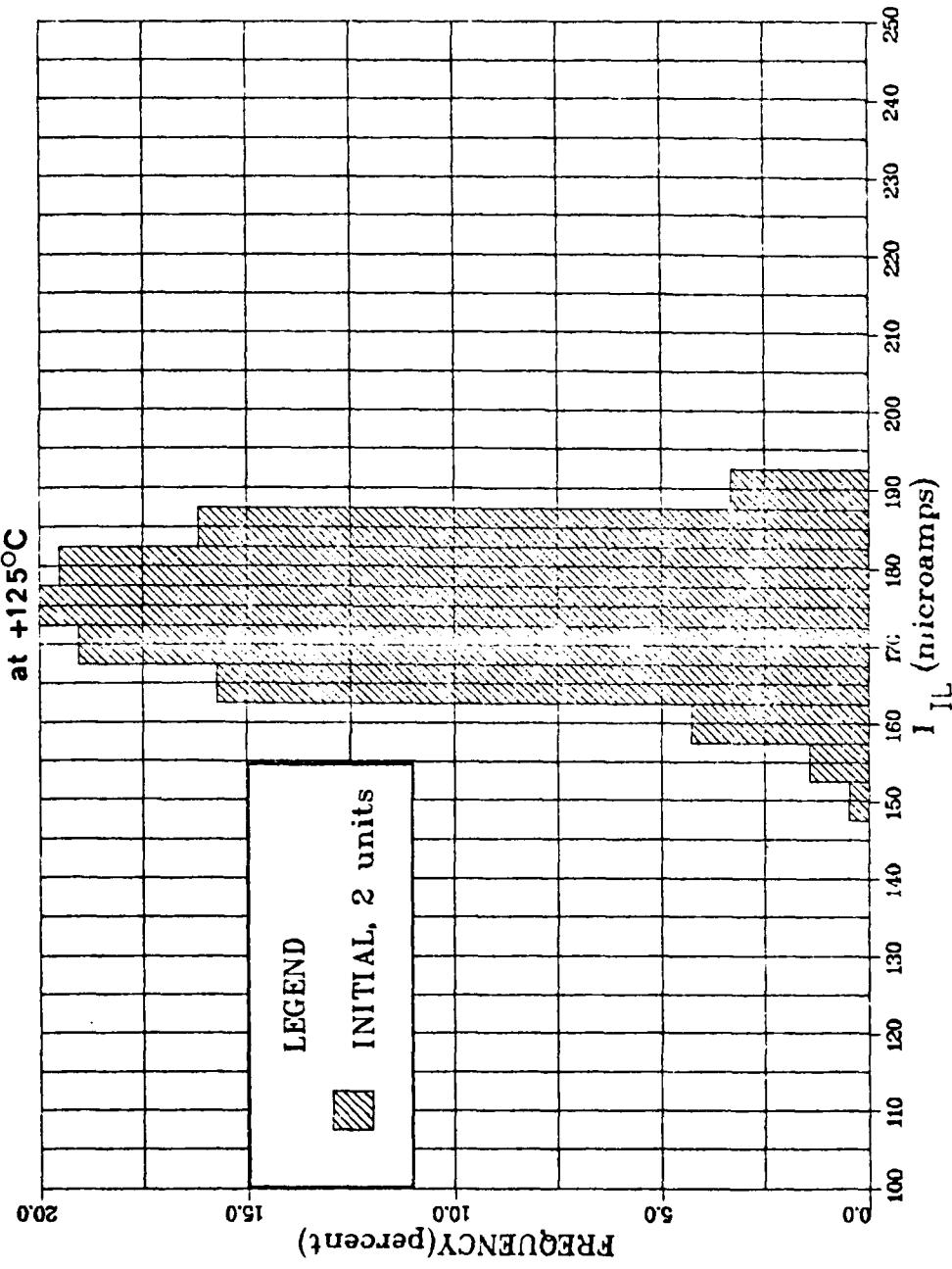
## Short Circuit Output Current Distribution

Vendor B 54LS181  
All Outputs at +125°C



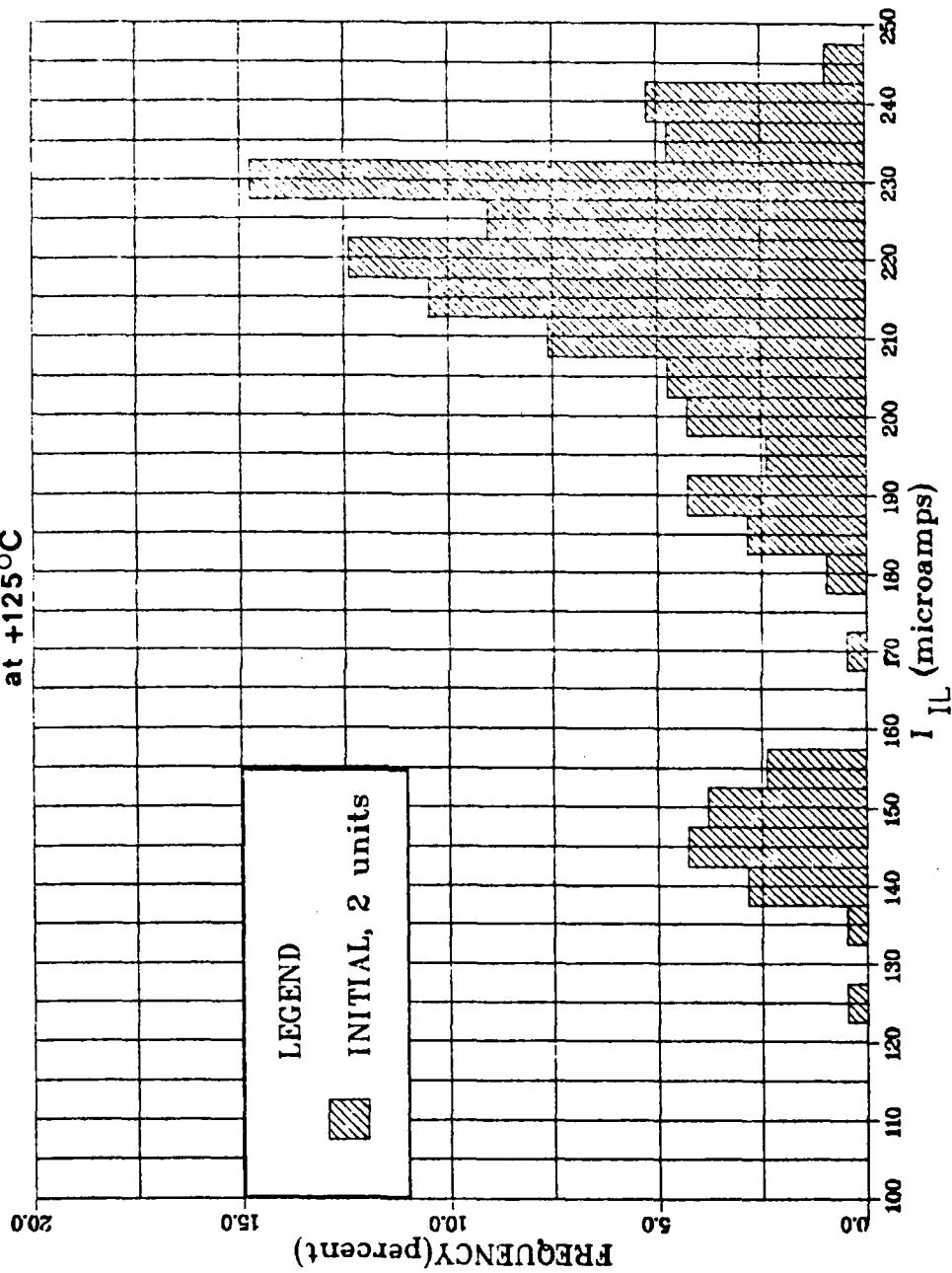
## Low-Level Input Current Distribution

Vendor A 541LS191  
All Inputs Except Pin 4  
at +12.5°C



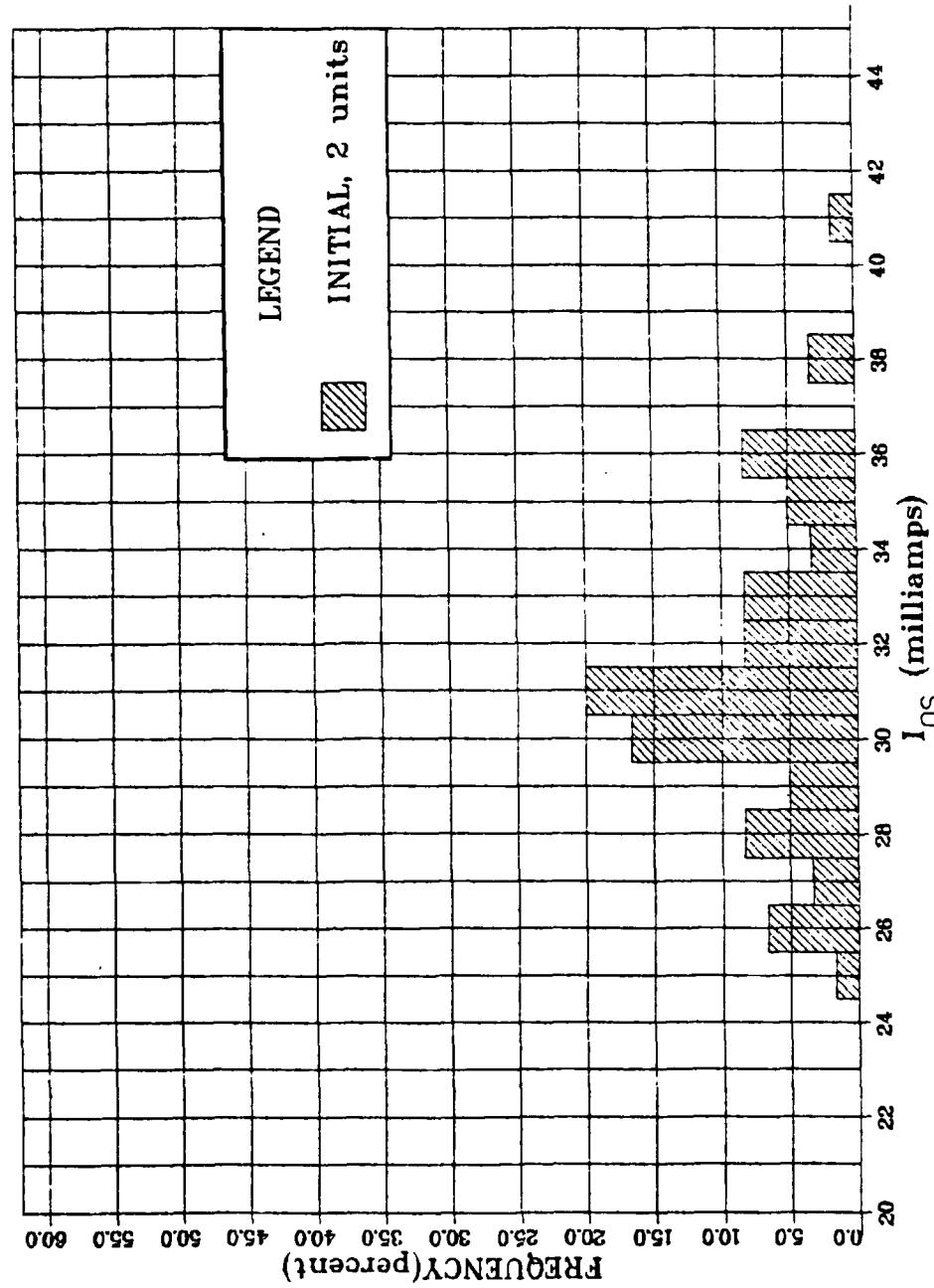
## Low-Level Input Current Distribution

Vendor B 54LS191  
All Inputs Except Pin 4  
at +125°C



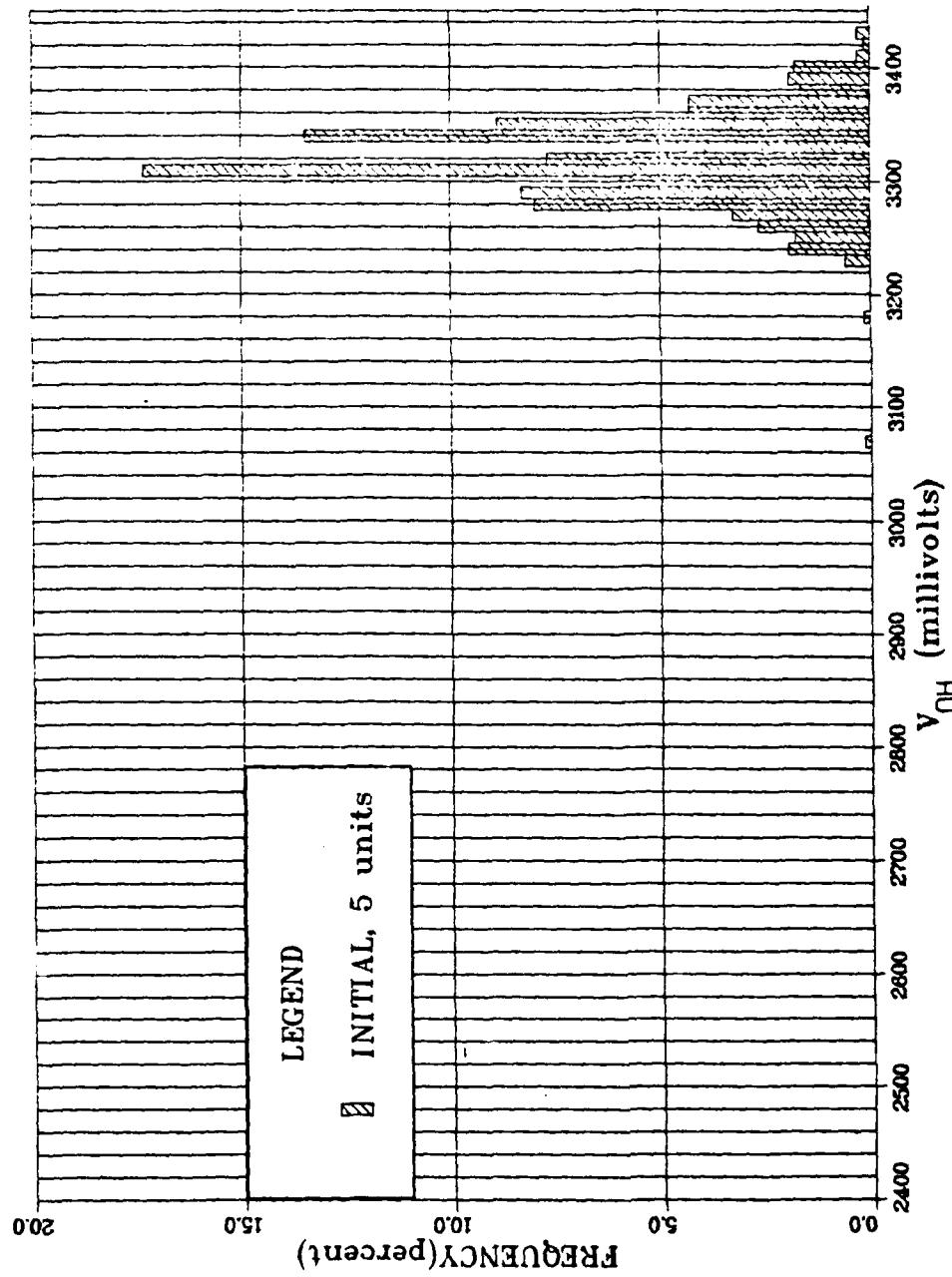
## Short Circuit Output Current Distribution

Vendor B 54LS251  
All Outputs at +125°C



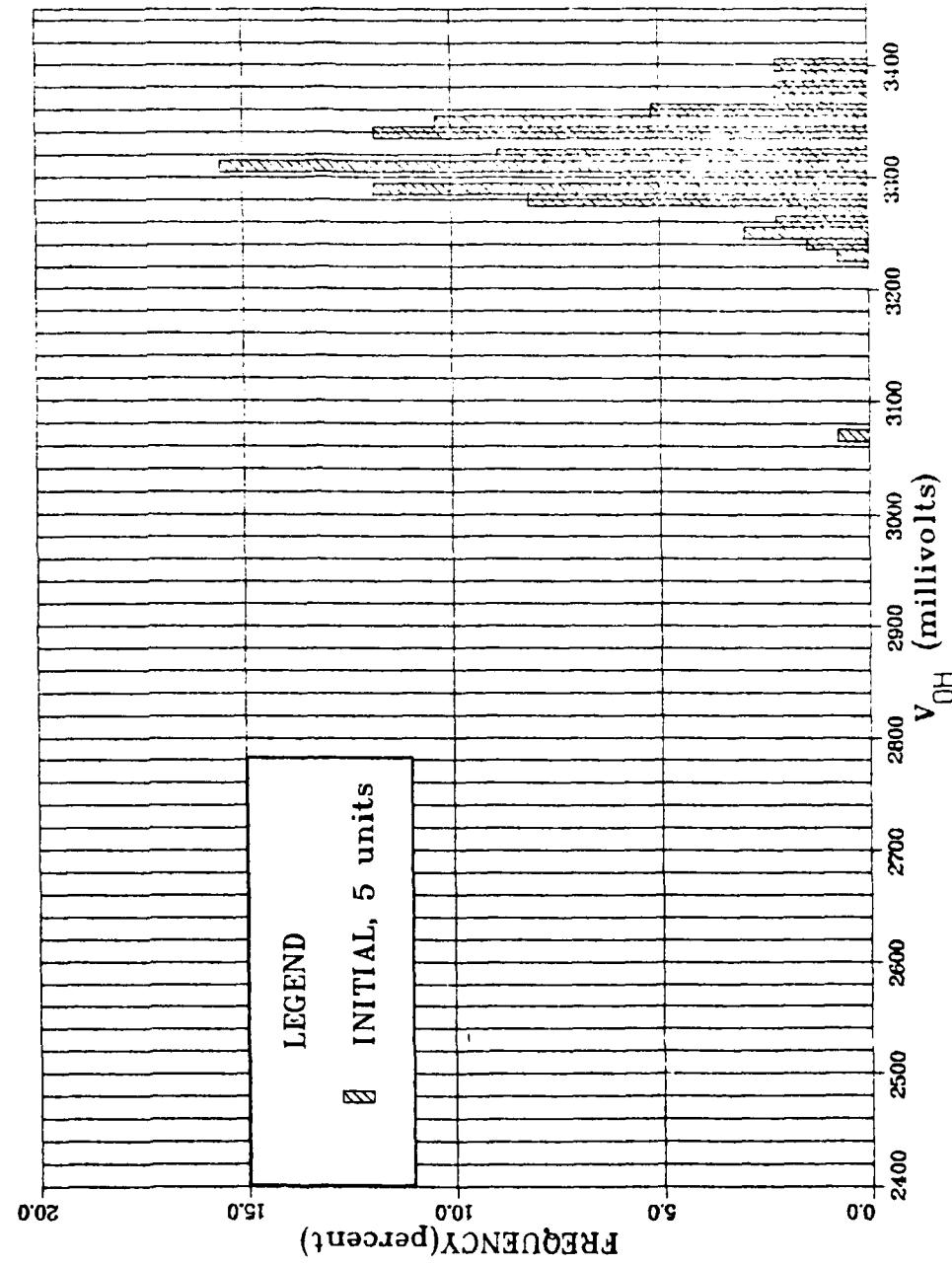
## High-Level Output Voltage Distribution

Vendor A 54LS283  
All Outputs at +125°C



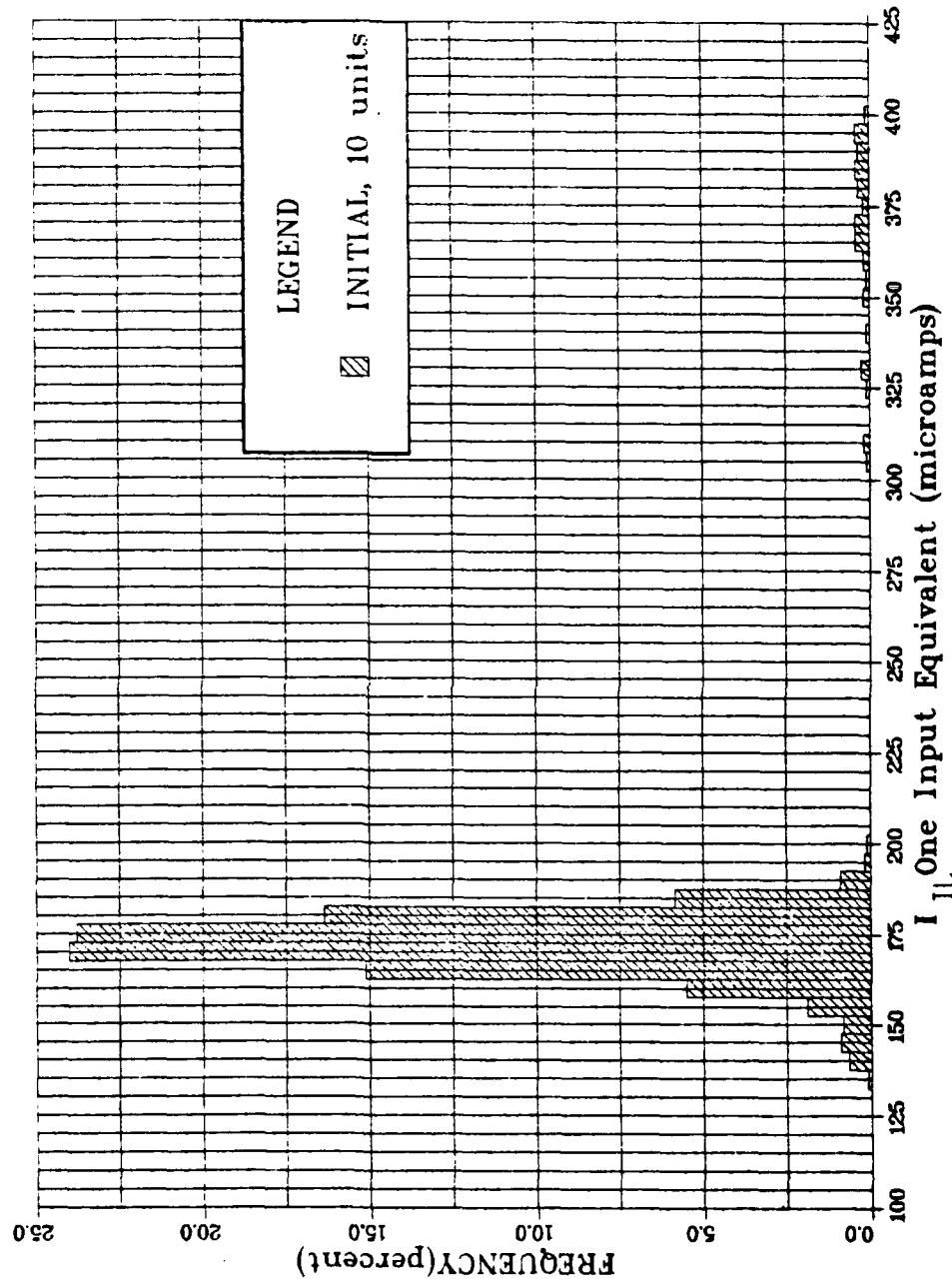
## High-Level Output Voltage Distribution

Vendor A 54LS283  
Output Pin 4 at +125°C



## Low-Level Current Distribution

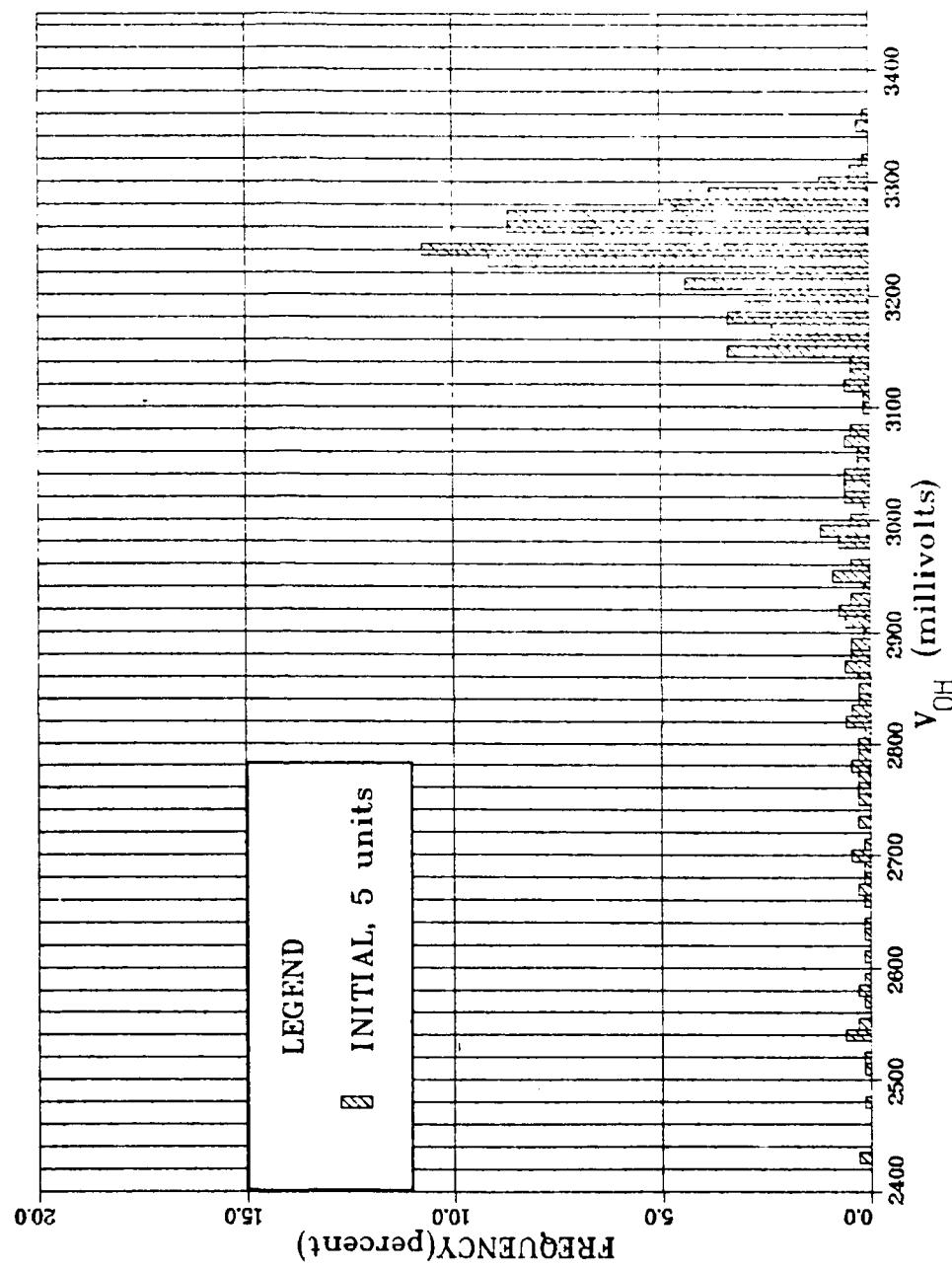
Vendor A 54LS283  
All Inputs at +125°C



K-10

## High-Level Output Voltage Distribution

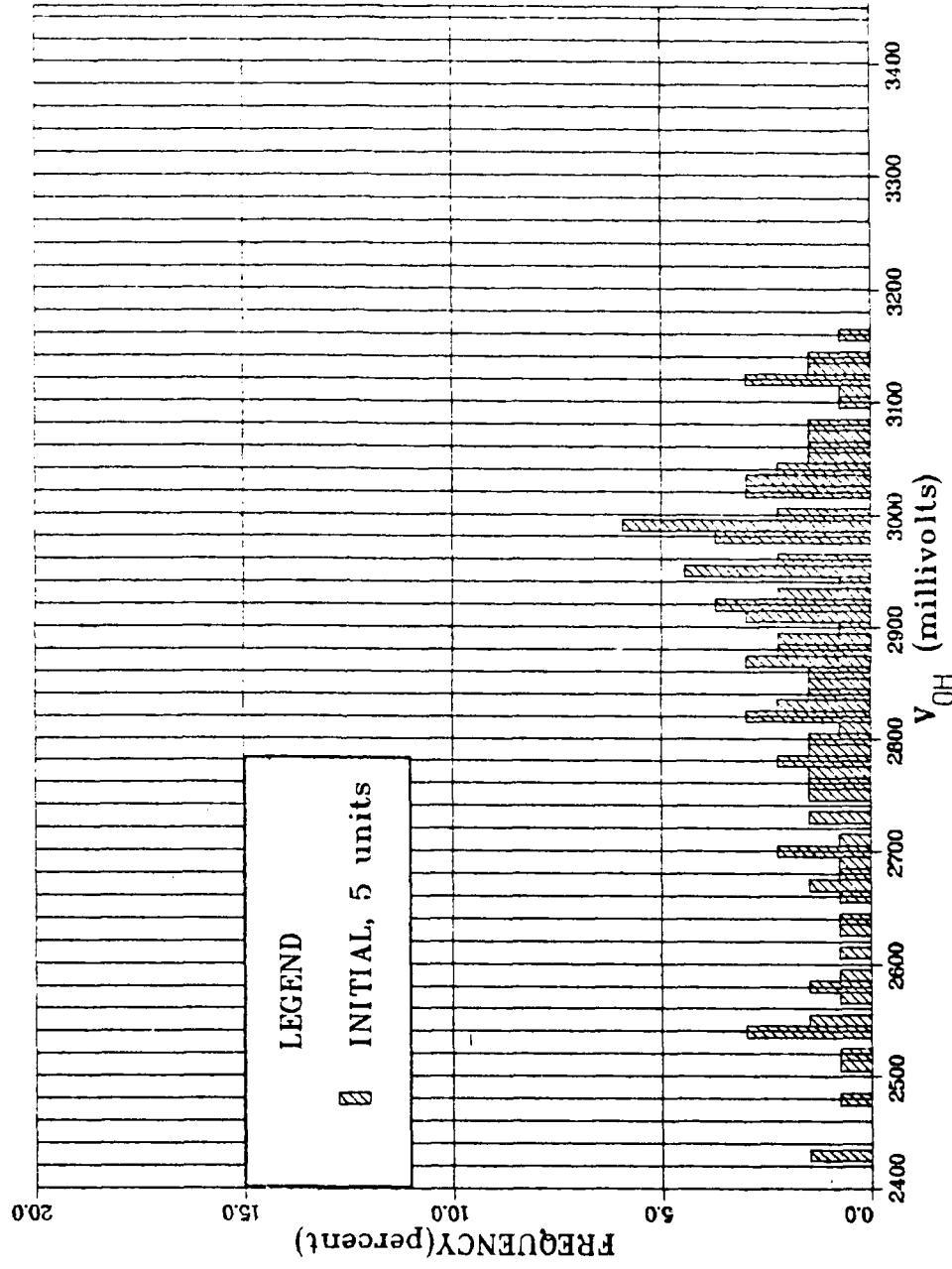
Vendor B 54LS283  
All Outputs at +125°C



## High-Level Output Voltage Distribution

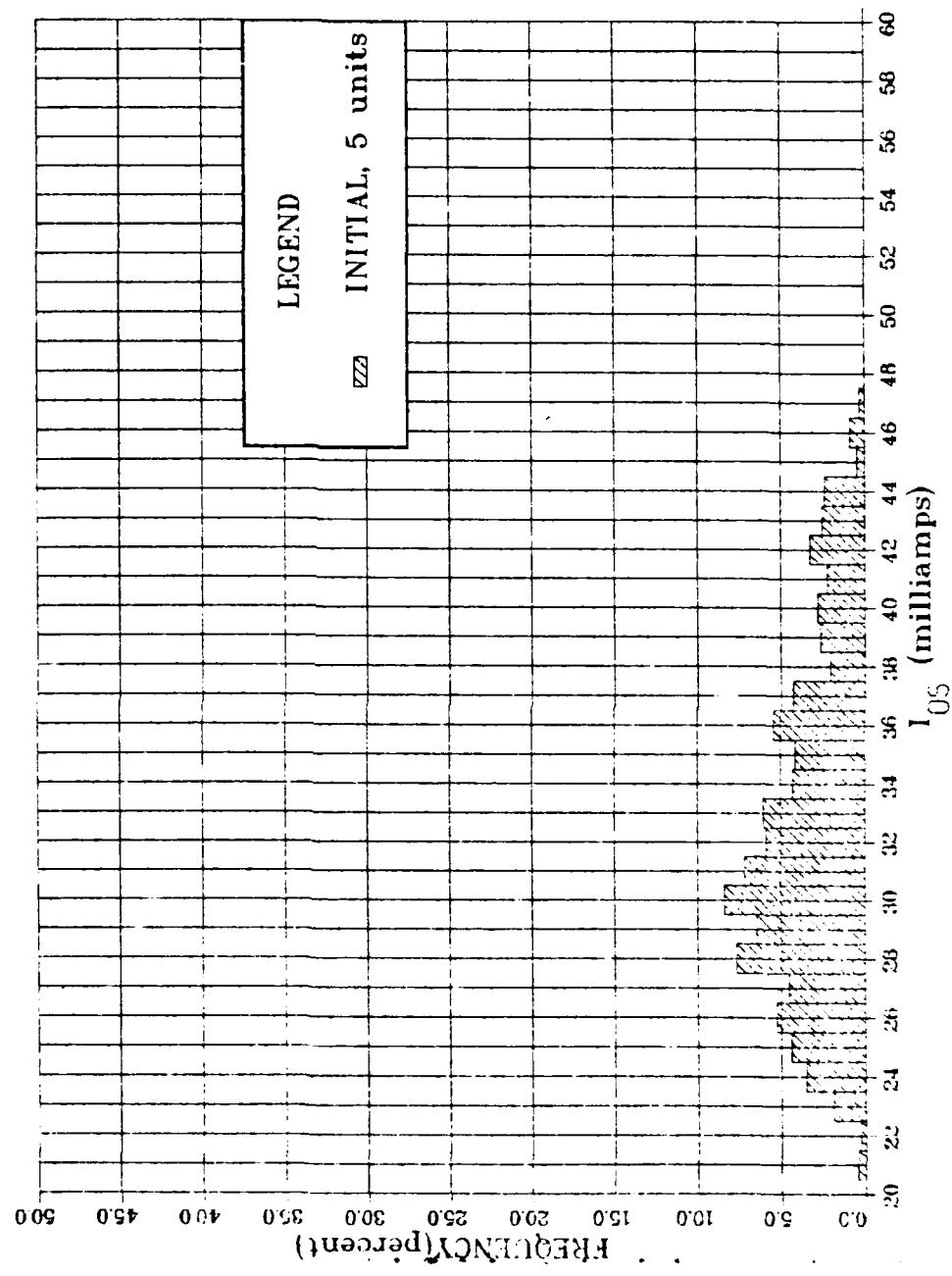
Vendor B 54LS283

Output Pin 4 at +125°C

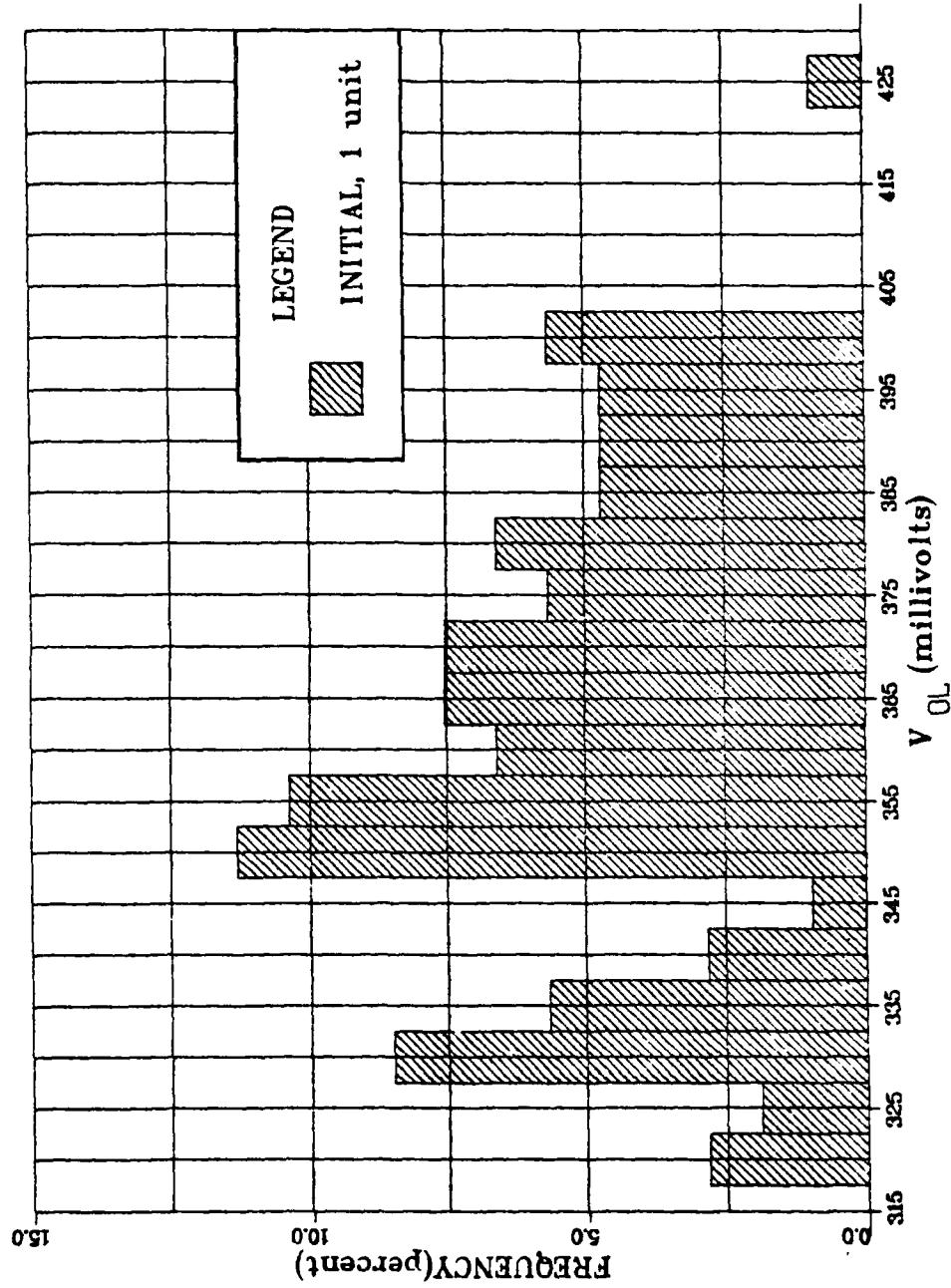


## Short Circuit Output Current Distribution

Vendor B 541S283  
All Outputs at +125°C

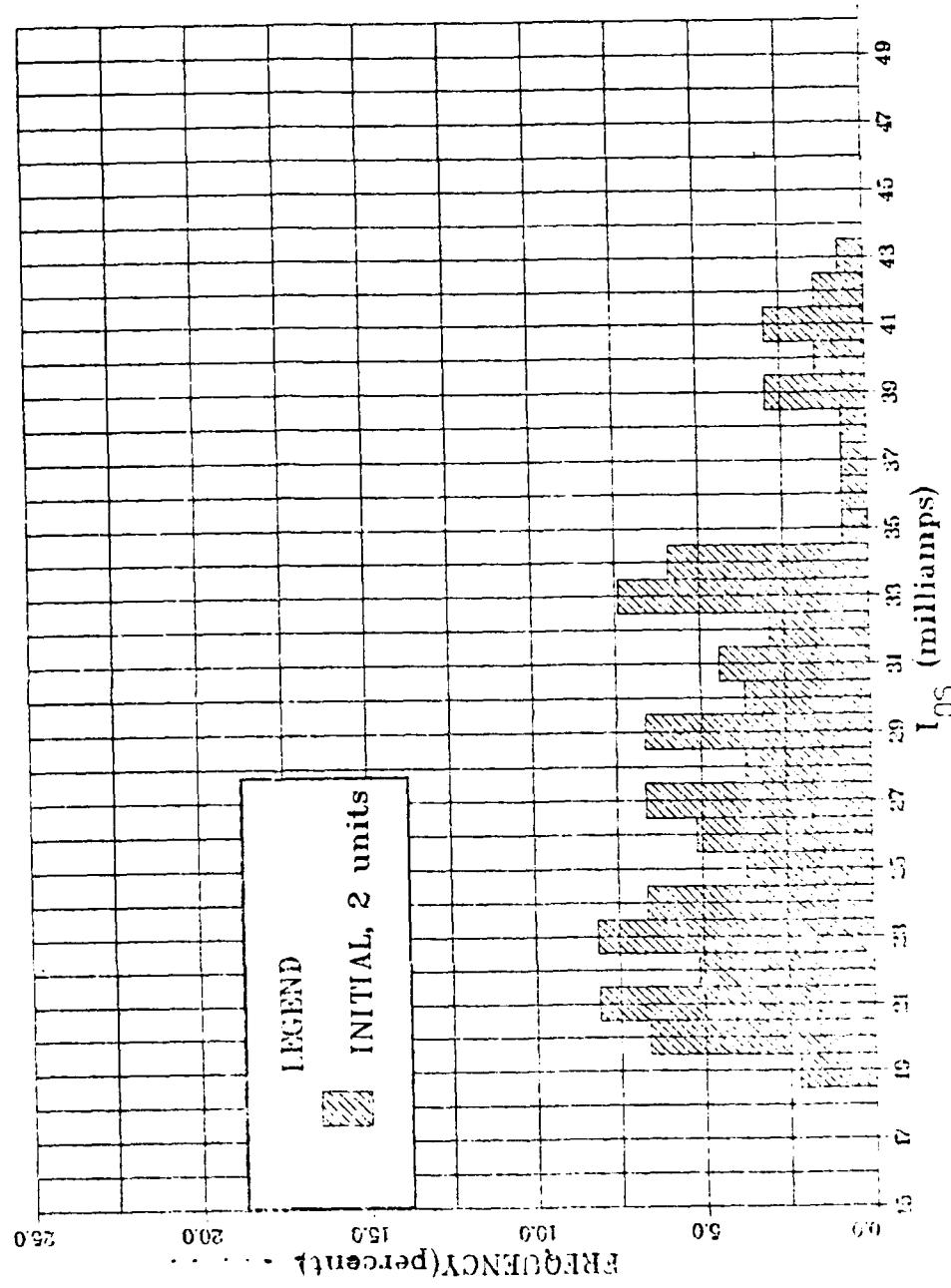


Low-Level Voltage Distribution  
Vendor C RAM  
Output Pin 6 at -55°C



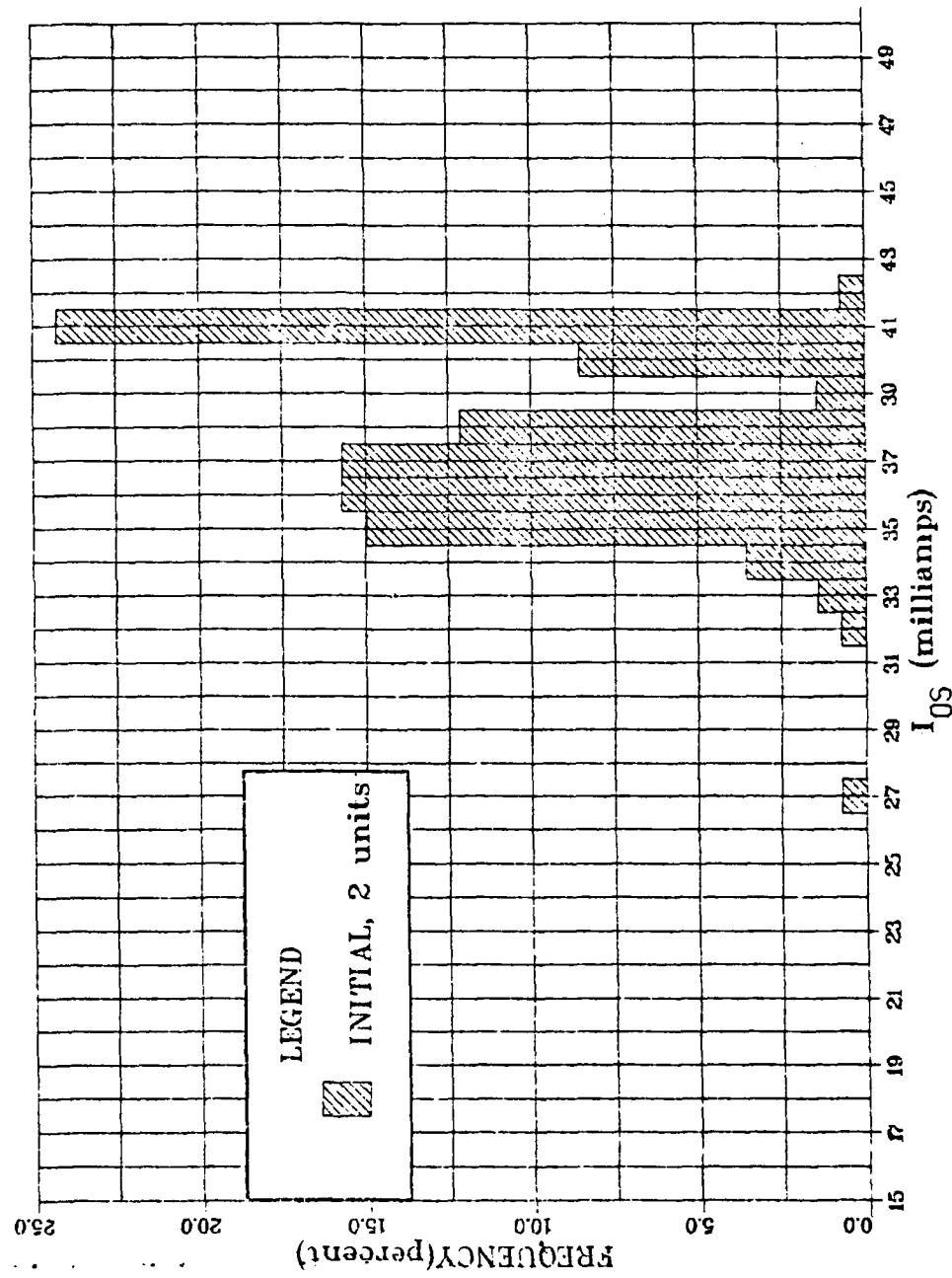
## Short Circuit Output Current Distribution

Vendor C RAM  
Output Pin 6 at -55°C



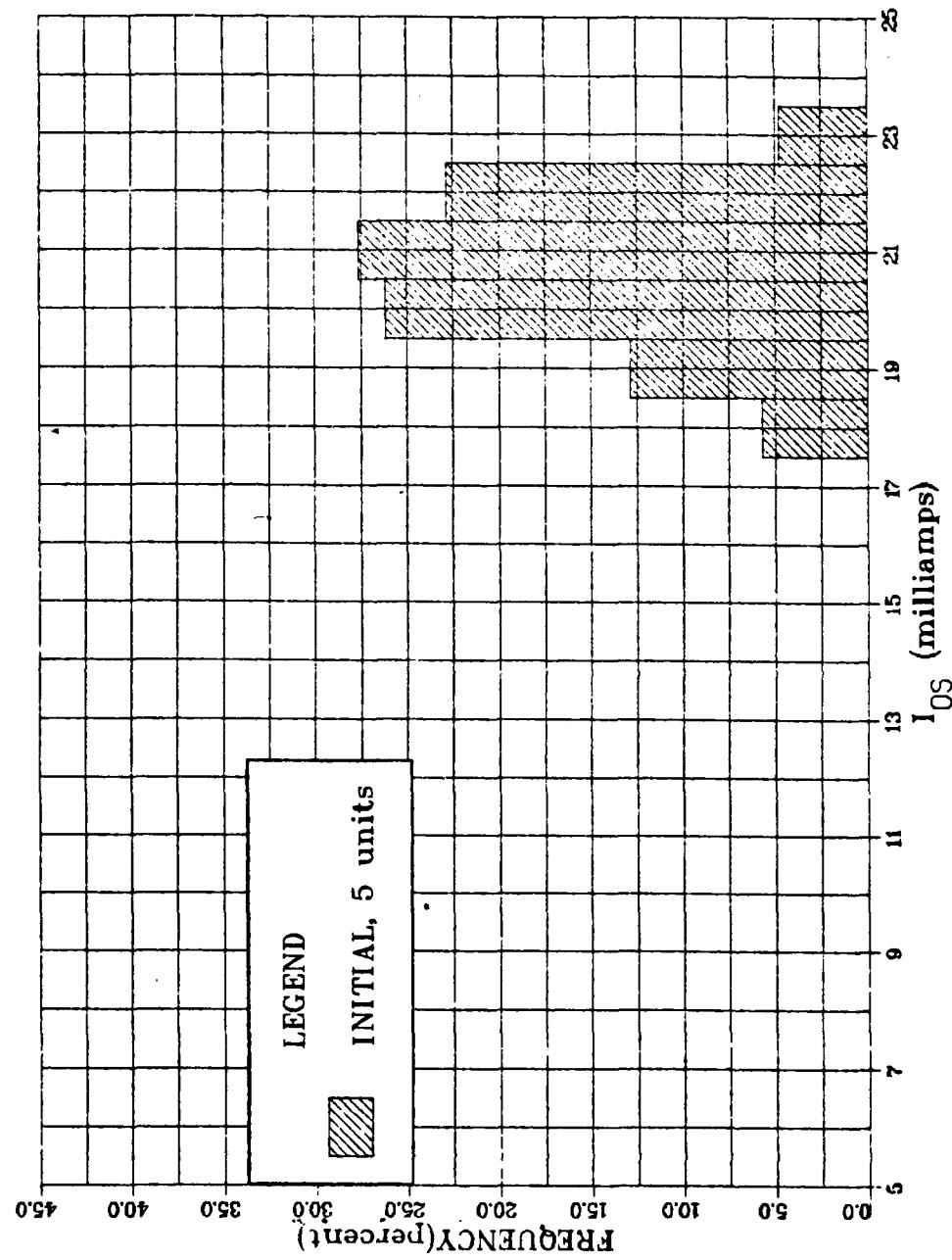
## Short Circuit Output Current Distribution

Vendor D RAM  
Output Pin 6 at -55°C



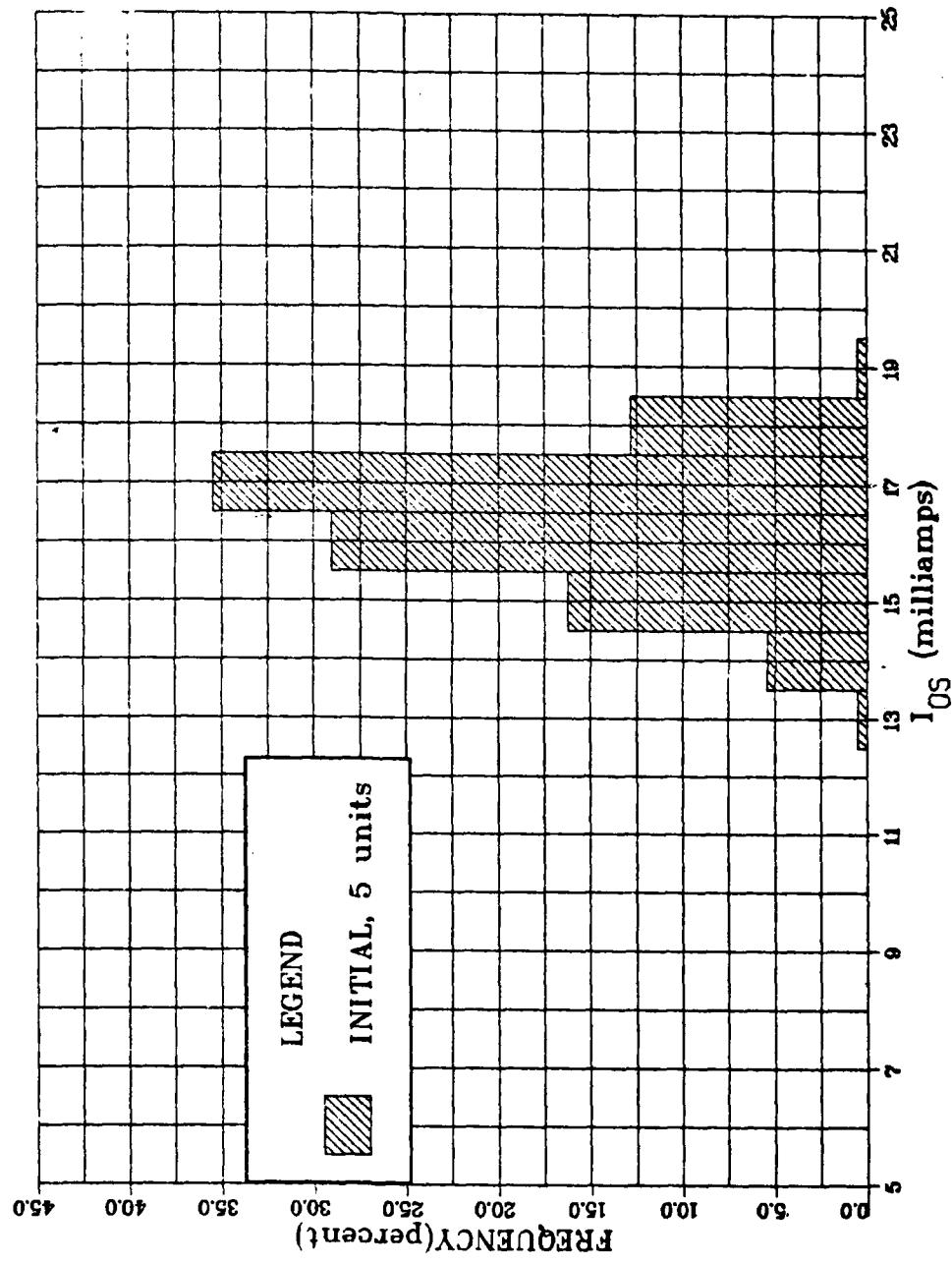
## Short Circuit Output Current Distribution

Vendor A 54LS181  
All Outputs at +25°C



## Short Circuit Output Current Distribution

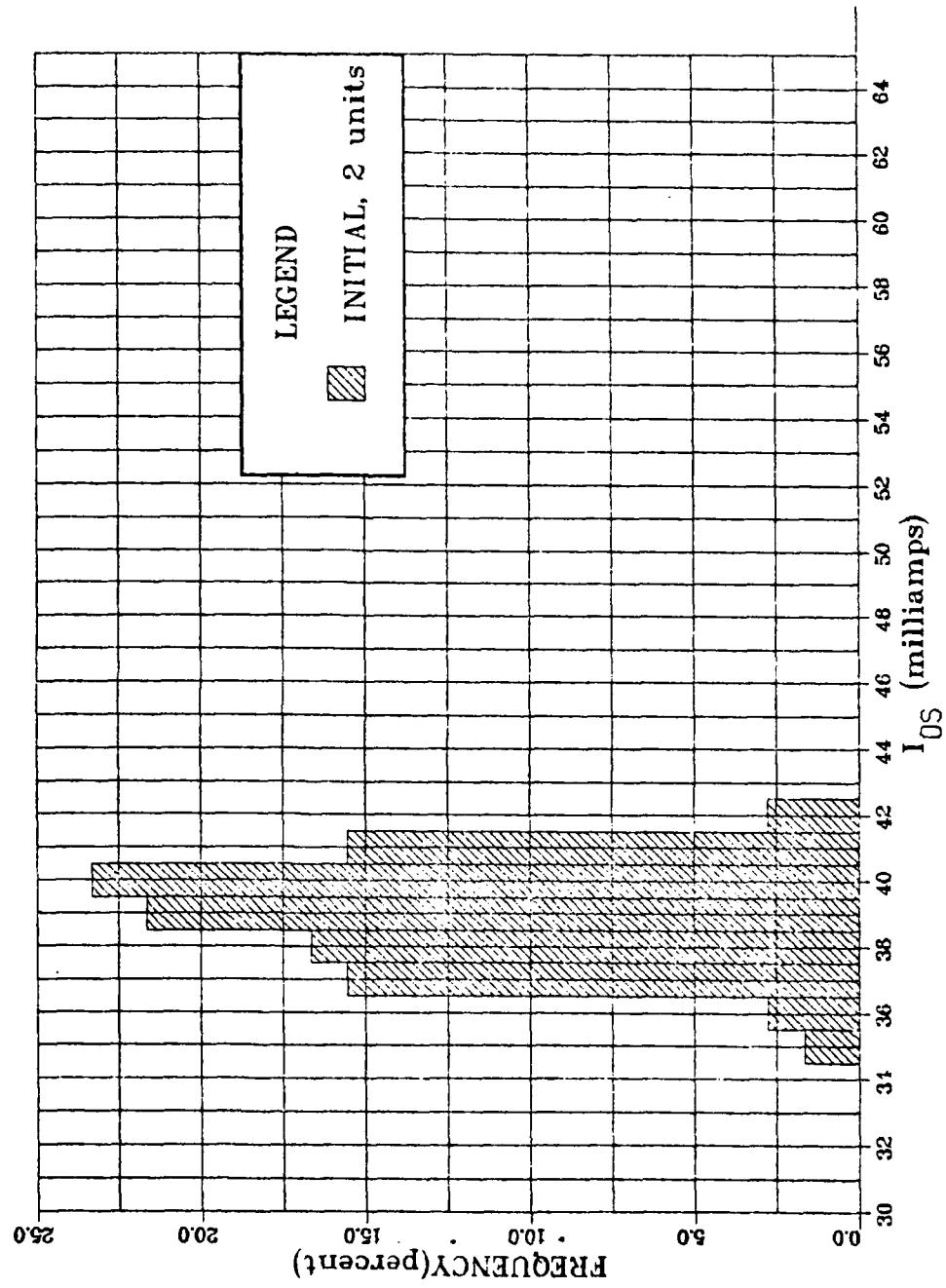
Vendor B 54LS181  
All Outputs at +25°C



## Short Circuit Output Current Distribution

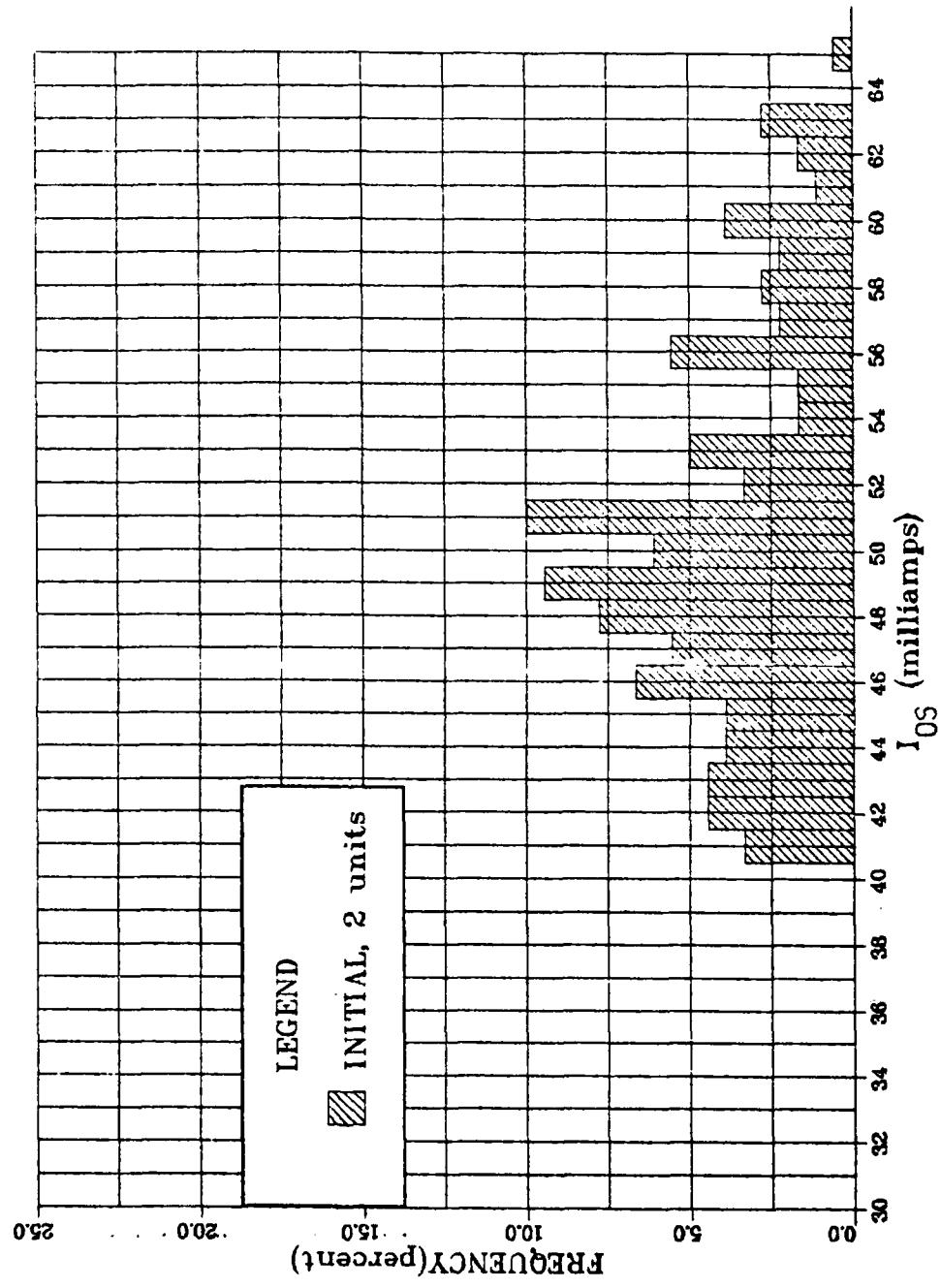
Vendor A 54LS191

All Outputs at +25°C



## Short Circuit Output Current Distribution

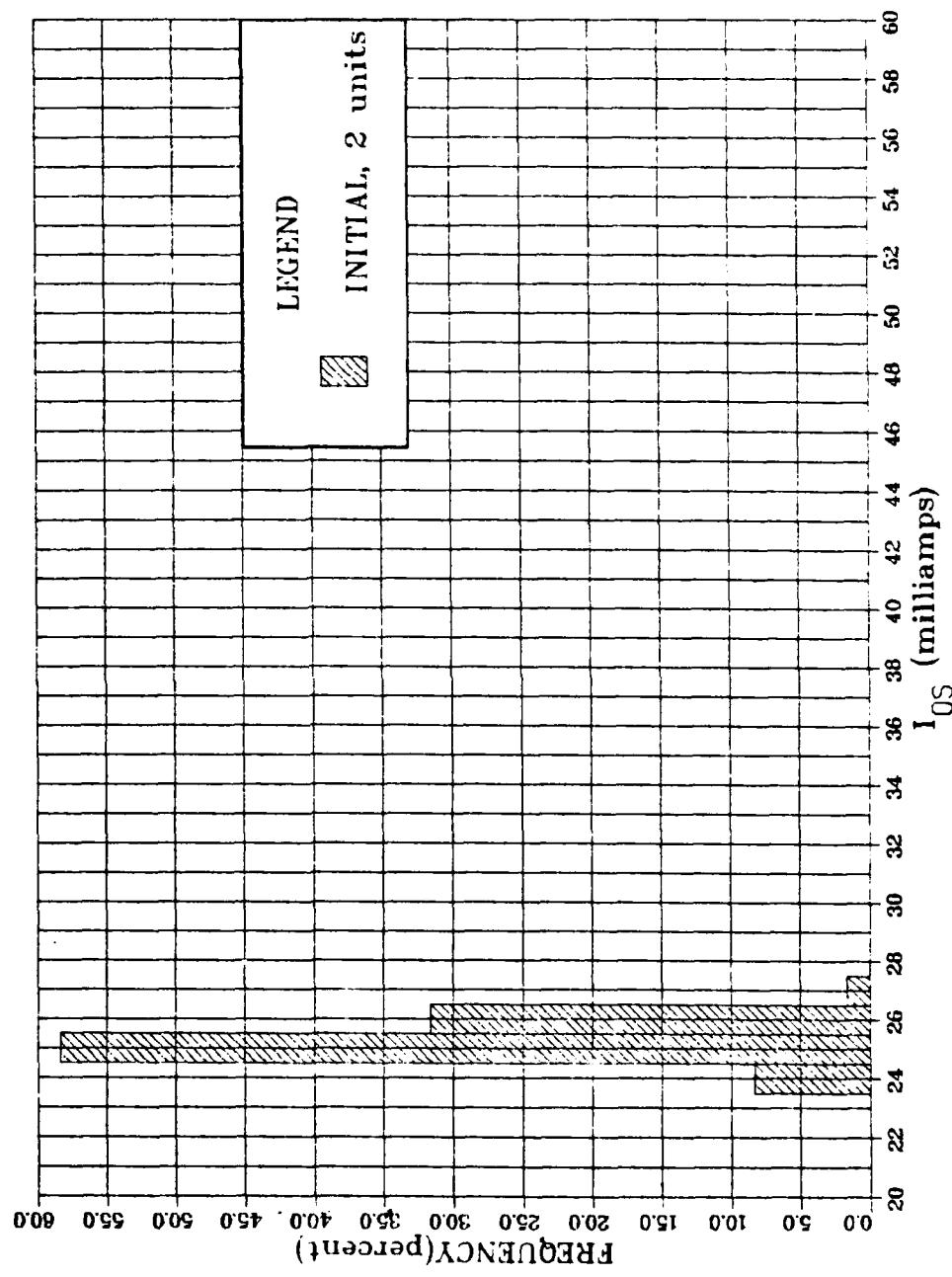
Vendor B 54LS191  
All Outputs at +25°C



## Short Circuit Output Current Distribution

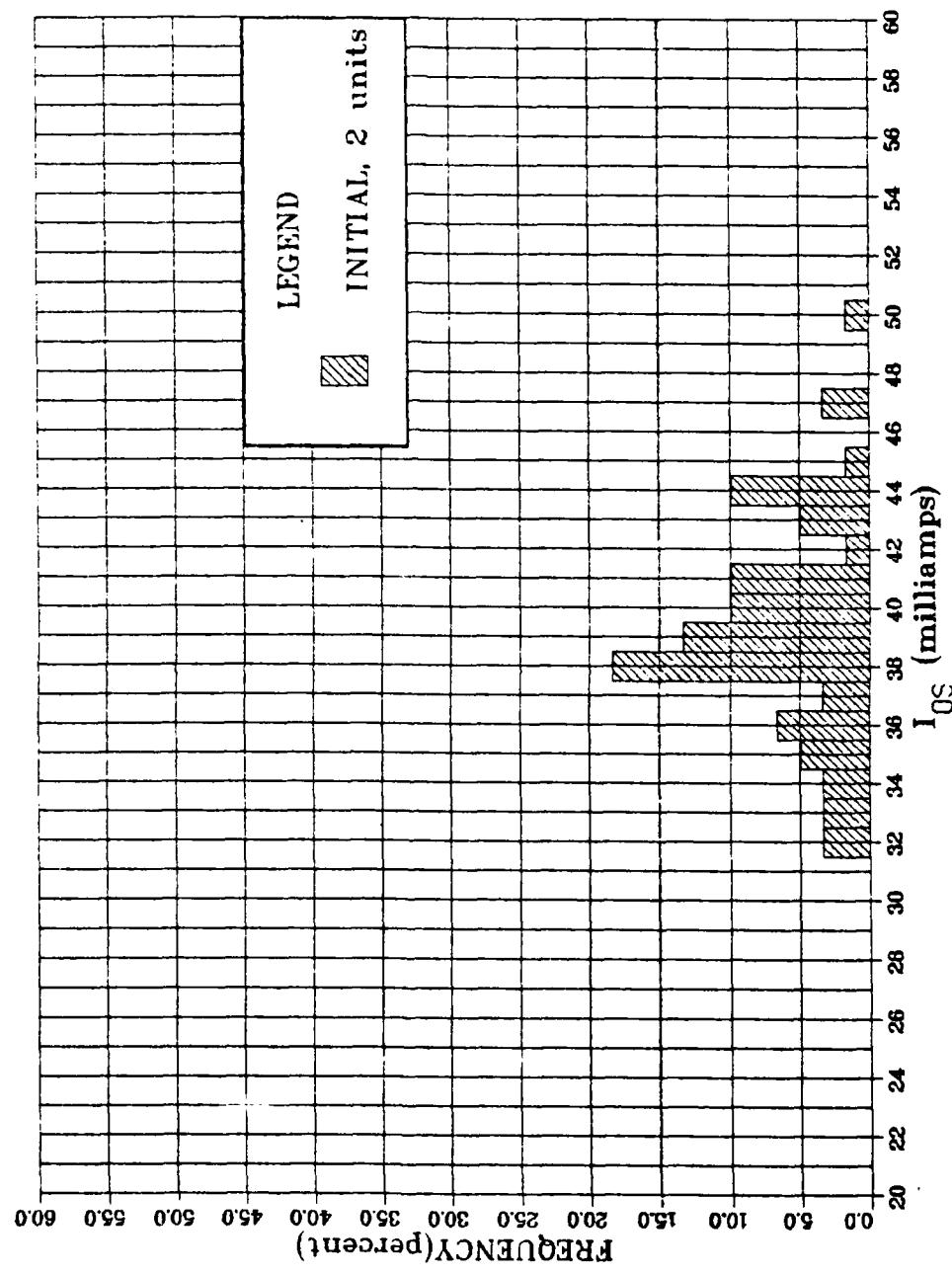
Vendor A 54LS251

All Outputs at +25°C



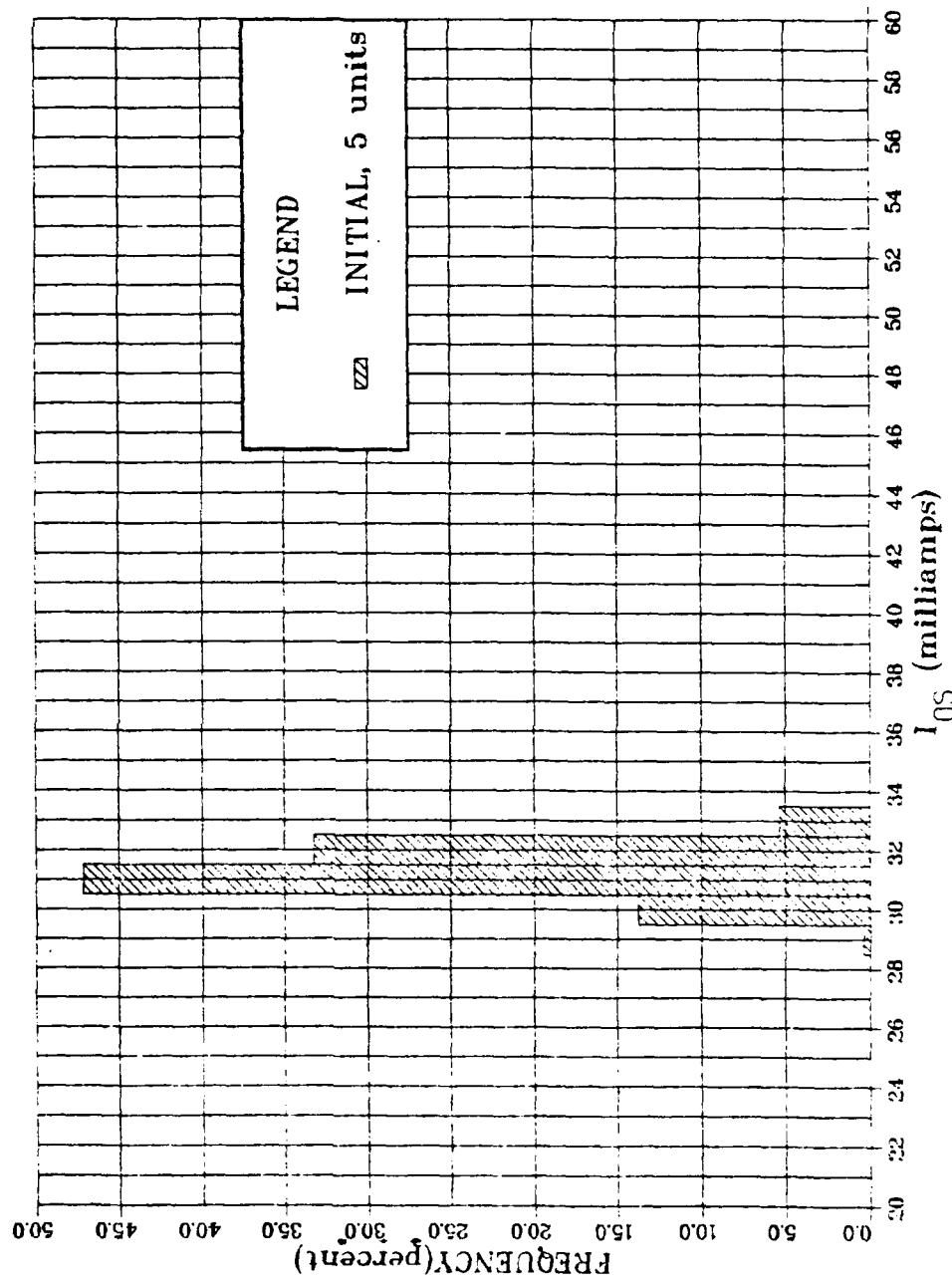
## Short Circuit Output Current Distribution

Vendor B 54LS251  
All Outputs at +25°C



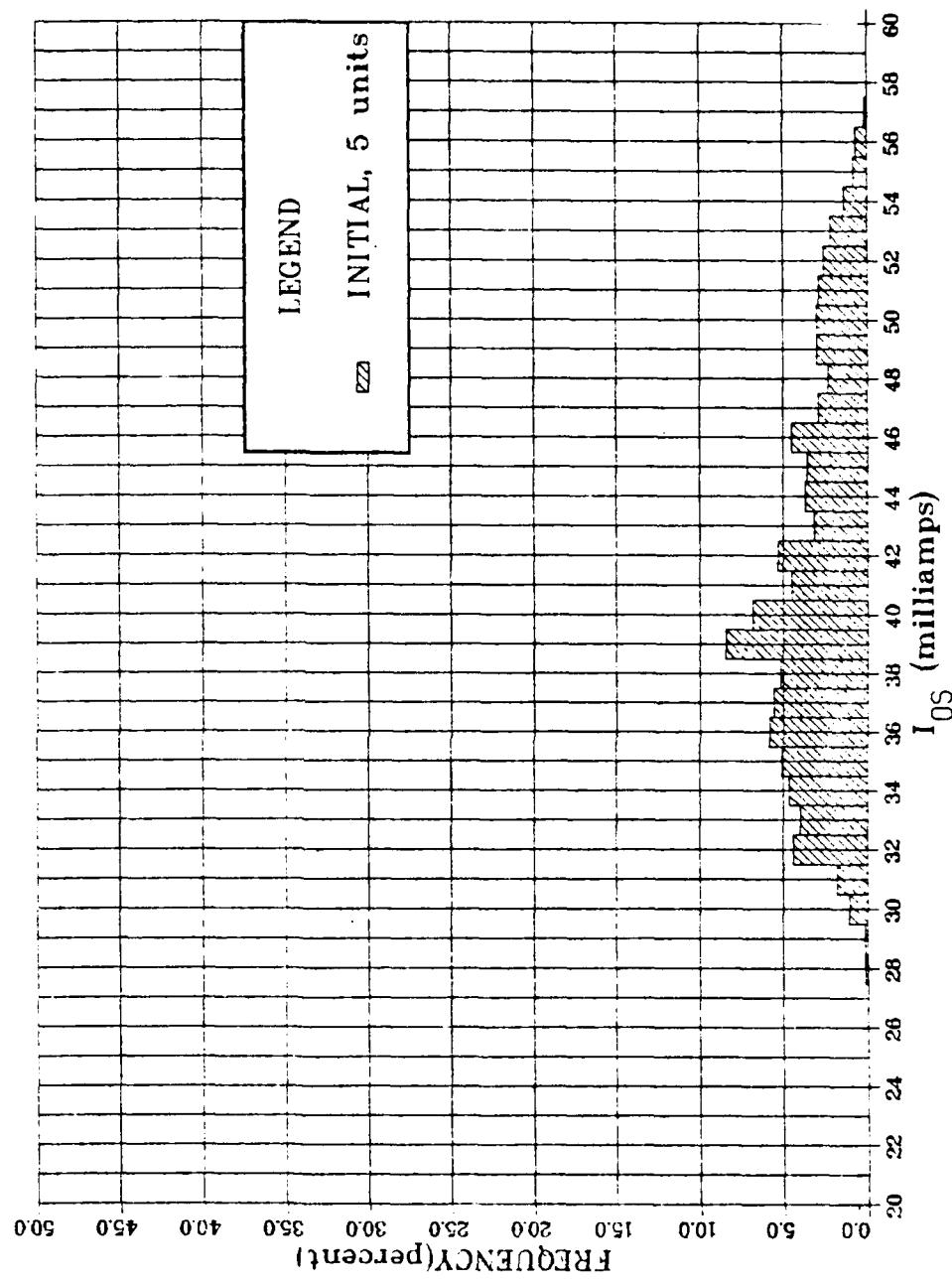
## Short Circuit Output Current Distribution

Vendor A 54LS283  
All Outputs at +25°C



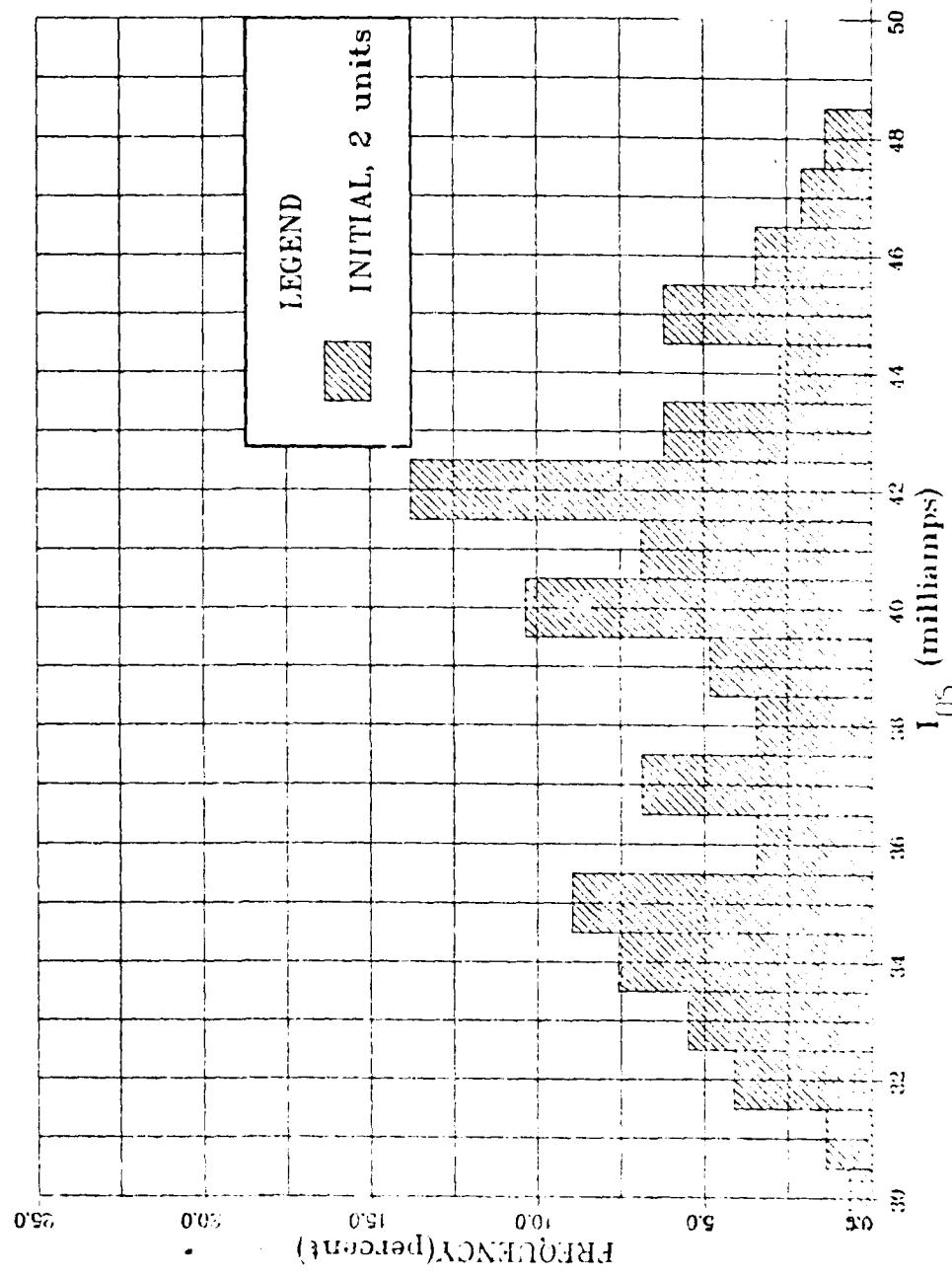
## Short Circuit Output Current Distribution

Vendor B 54LS283  
All Outputs at +25°C



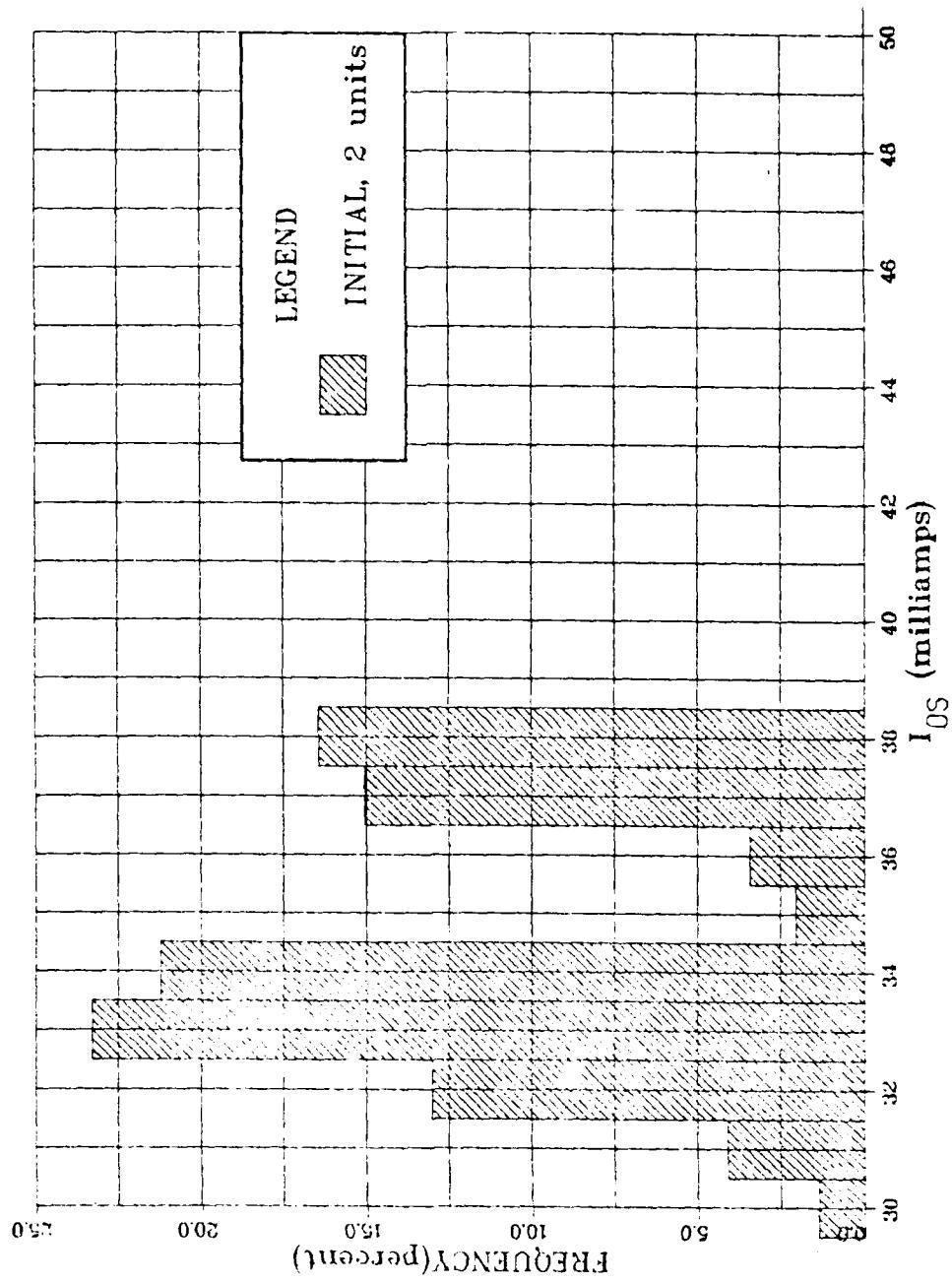
### Short Circuit Output Current Distribution

Vendor C RAM  
Output Pin 6 at +25°C



## Short Circuit Output Current Distribution

Vendor D RAM  
Output Pin 6 at +25°C

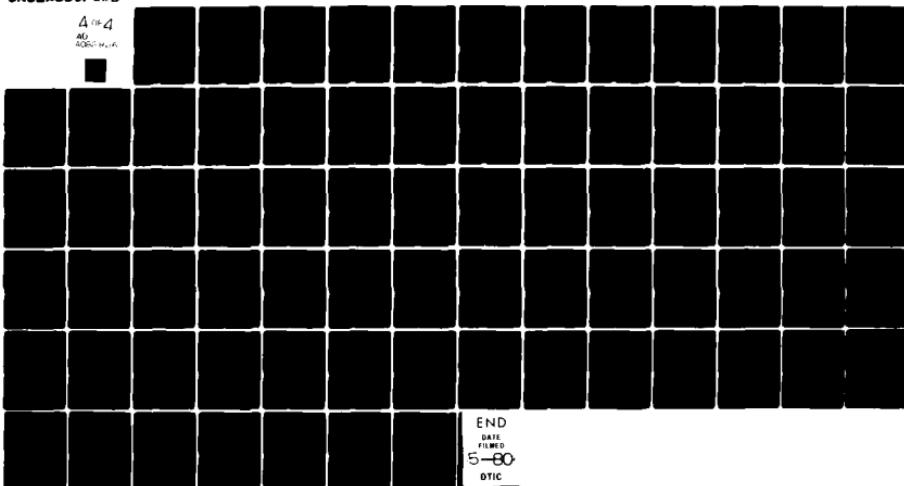


AD-A082 926

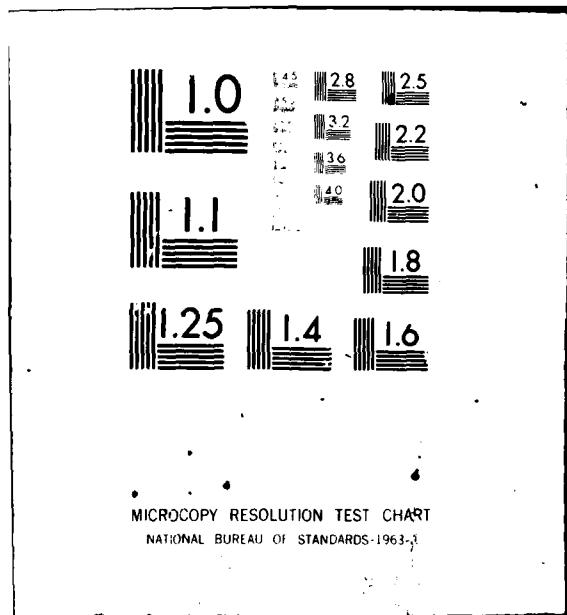
RAYTHEON CO BEDFORD MA MISSILE SYSTEMS DIV  
RELIABILITY EVALUATION OF LOW POWER SCHOTTKY CLAMPED MICROCIRCUIT--ETC(U)  
FEB 80 K B LASCH, D BARTELS, J J SPINALE F30602-77-C-0186  
RADC-TR-80-5 NL

UNCLASSIFIED

A or 4  
AU  
0200-14-16

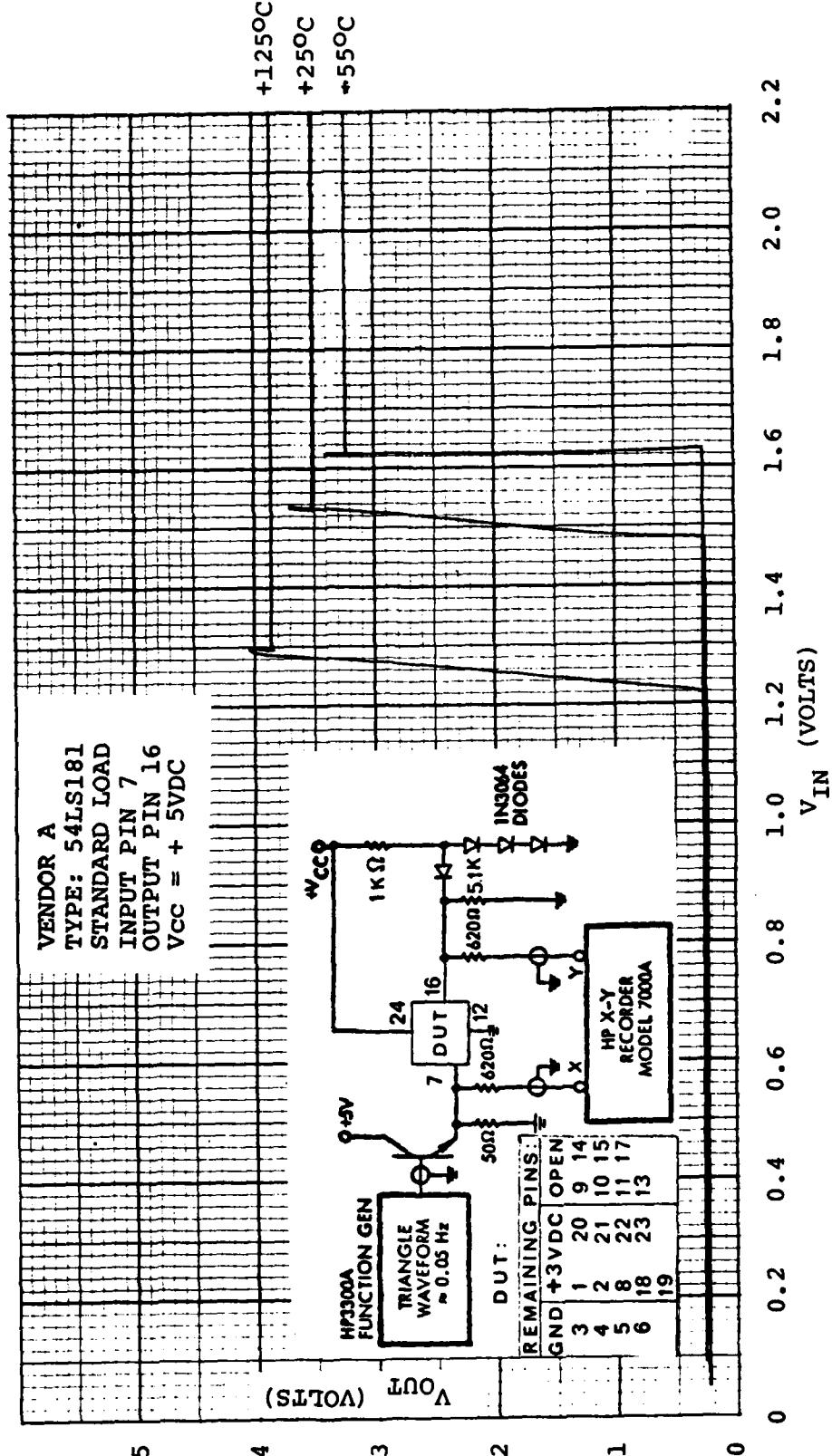


END  
DATE FILMED  
5-80  
DTIC

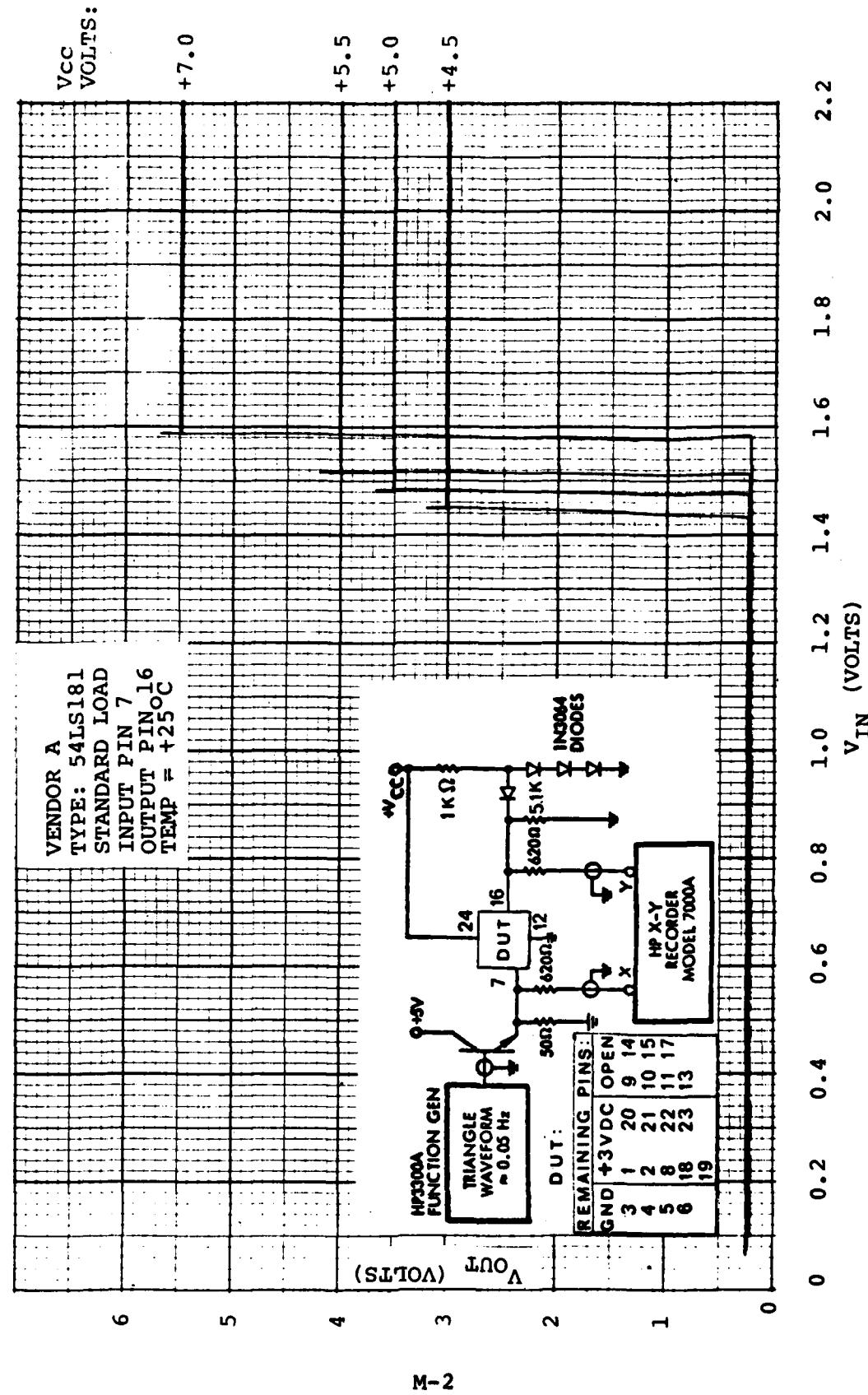


MICROCOPY RESOLUTION TEST CHART  
NATIONAL BUREAU OF STANDARDS-1963-1

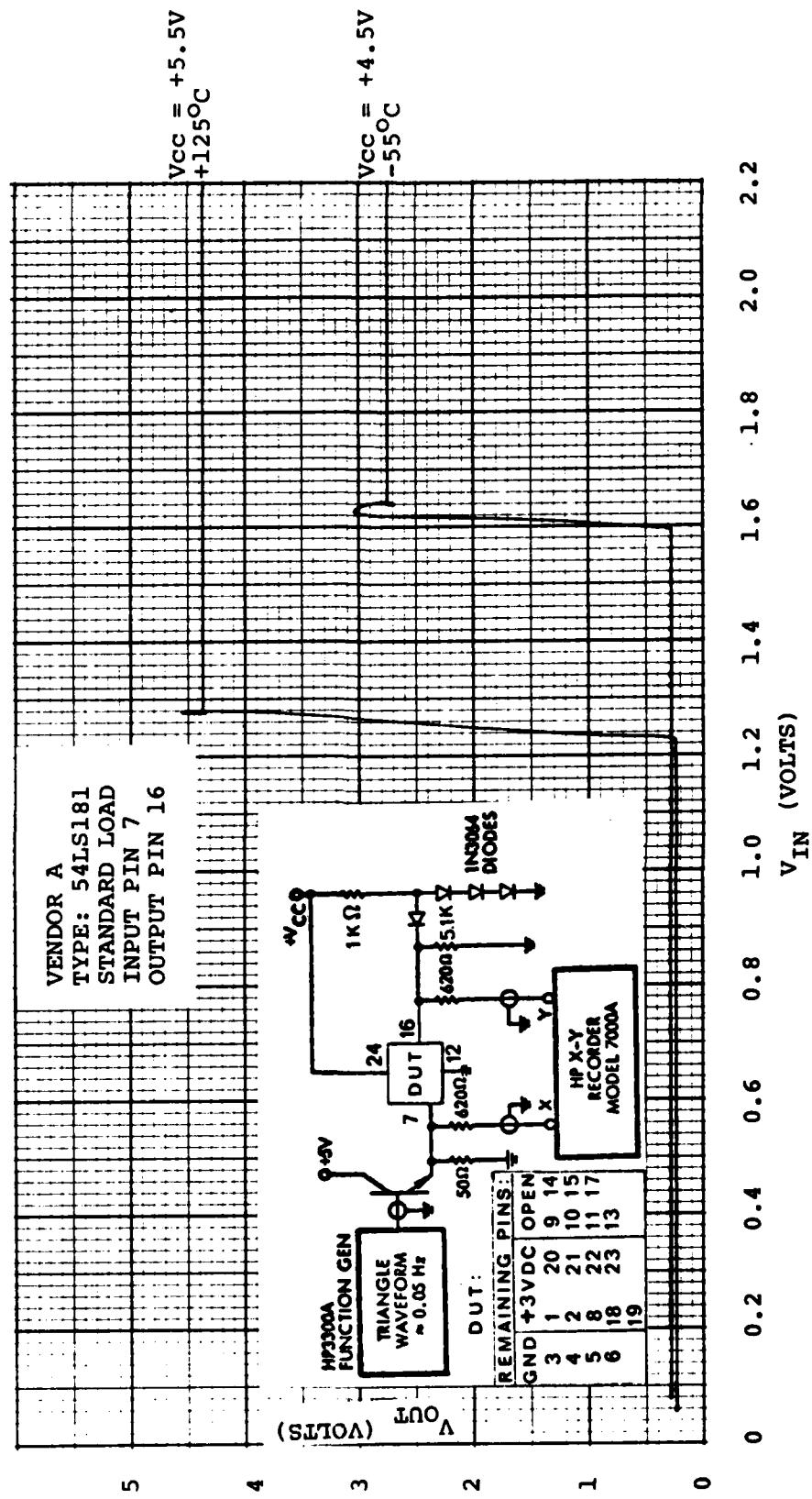
TRANSFER CHARACTERISTICS

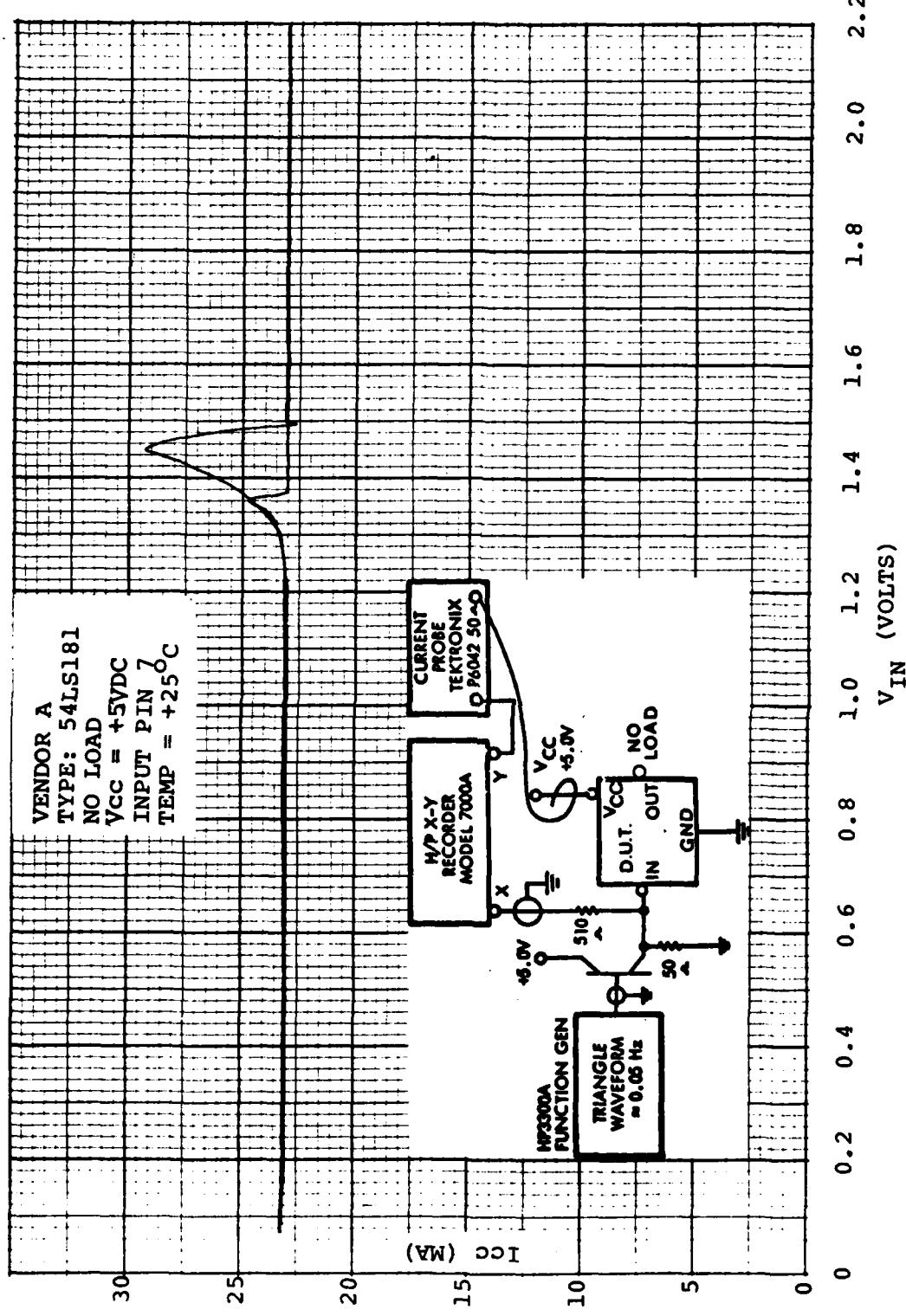


TRANSFER CHARACTERISTICS

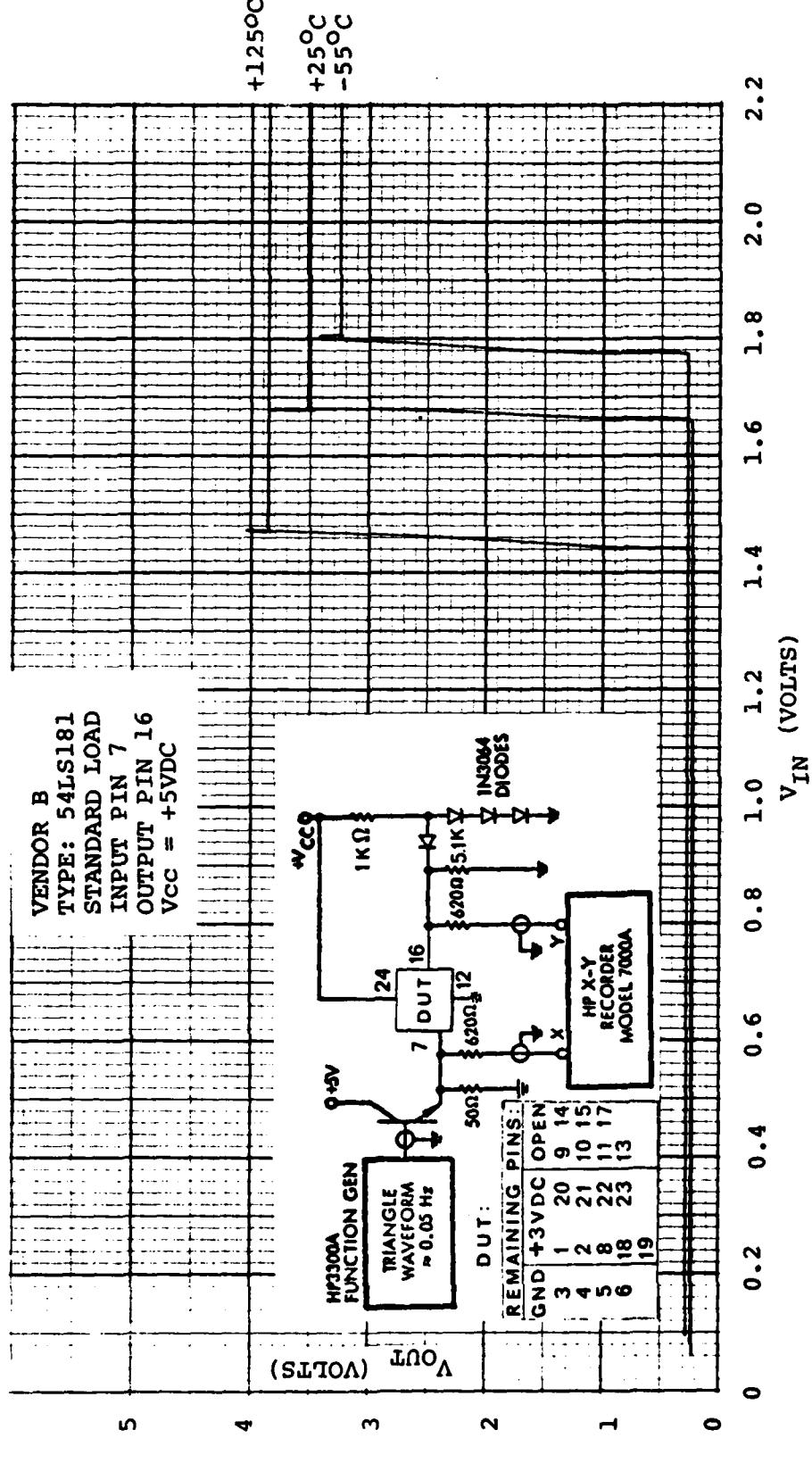


TRANSFER CHARACTERISTICS

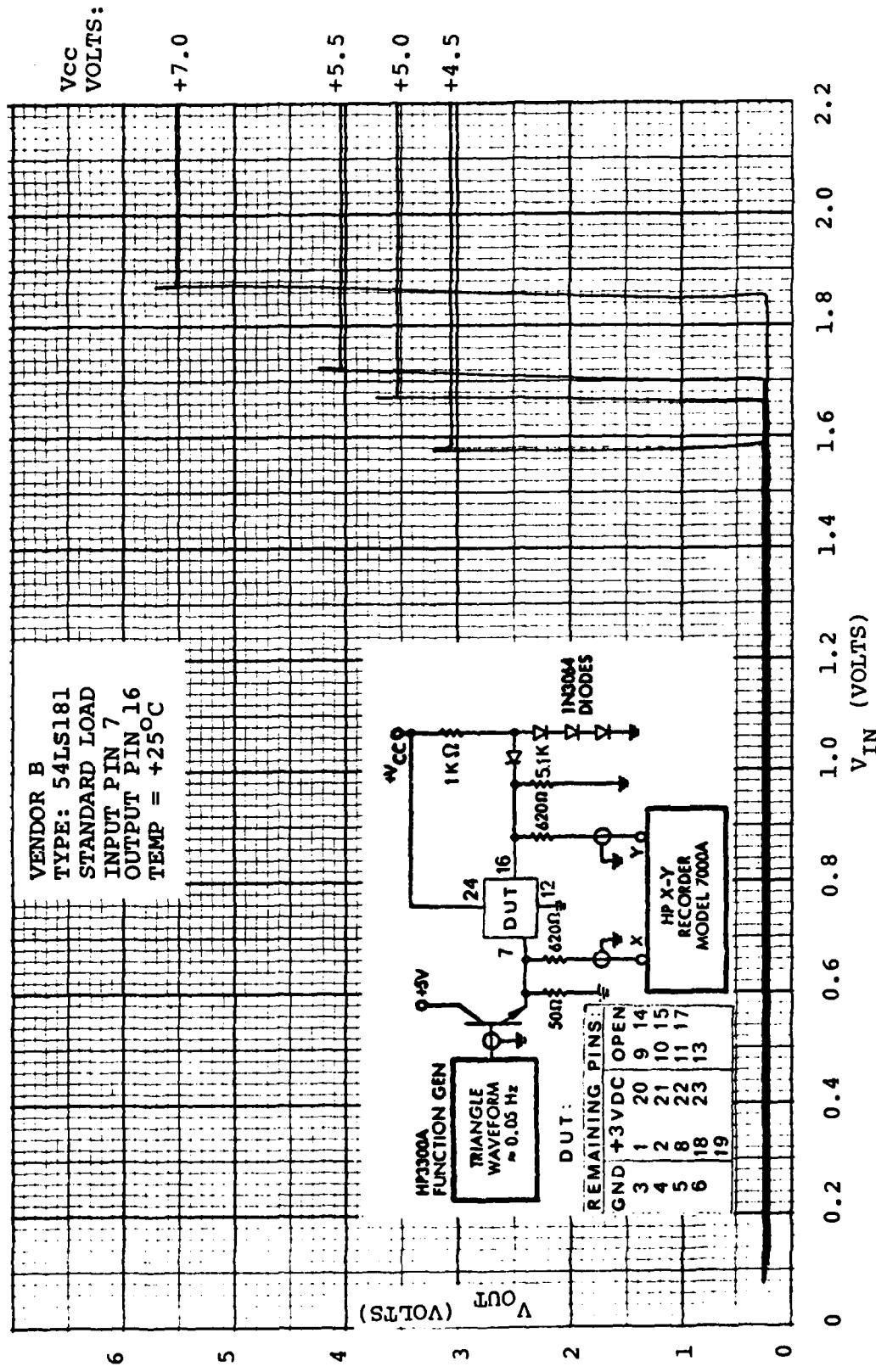




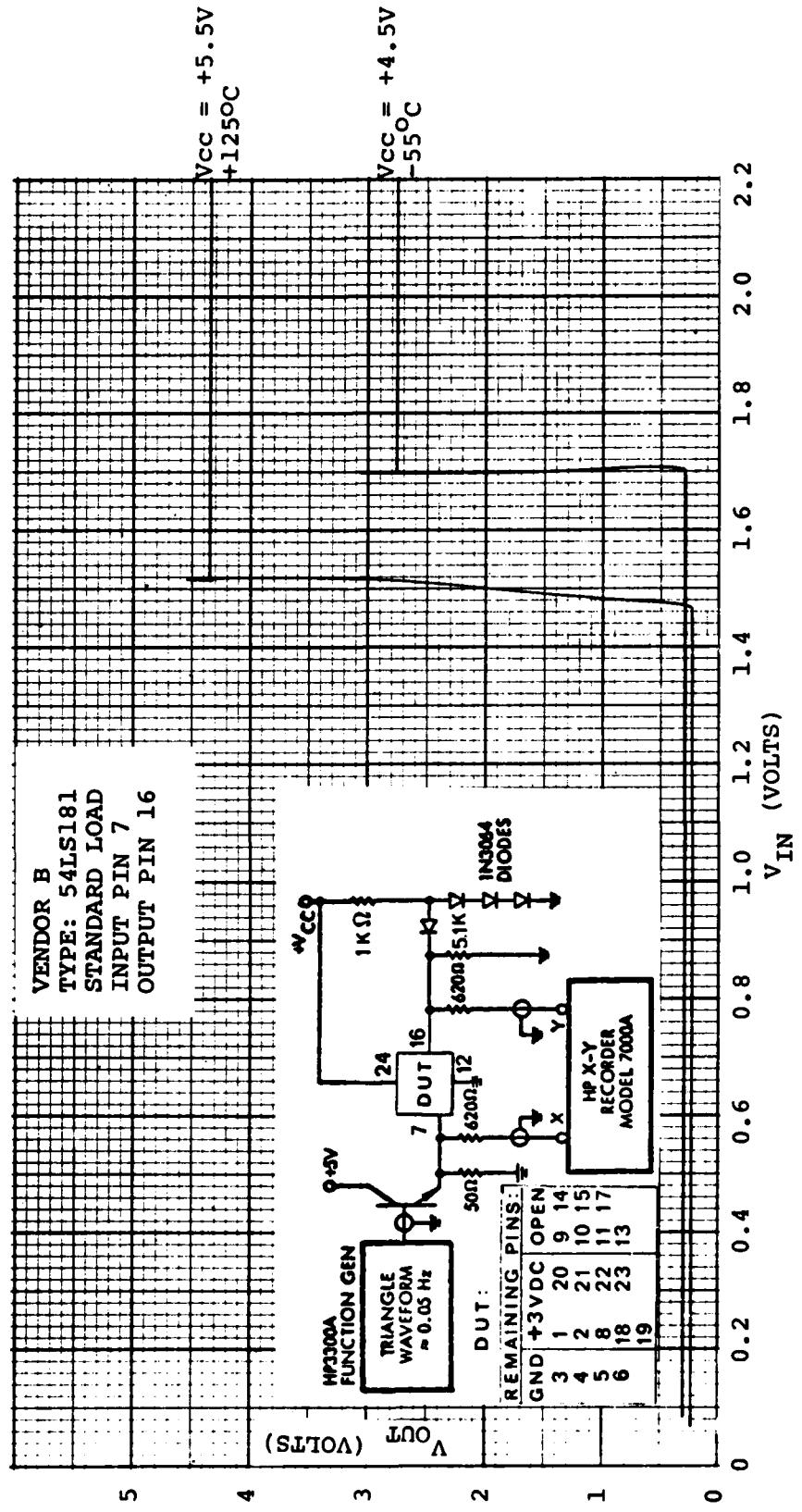
TRANSFER CHARACTERISTICS



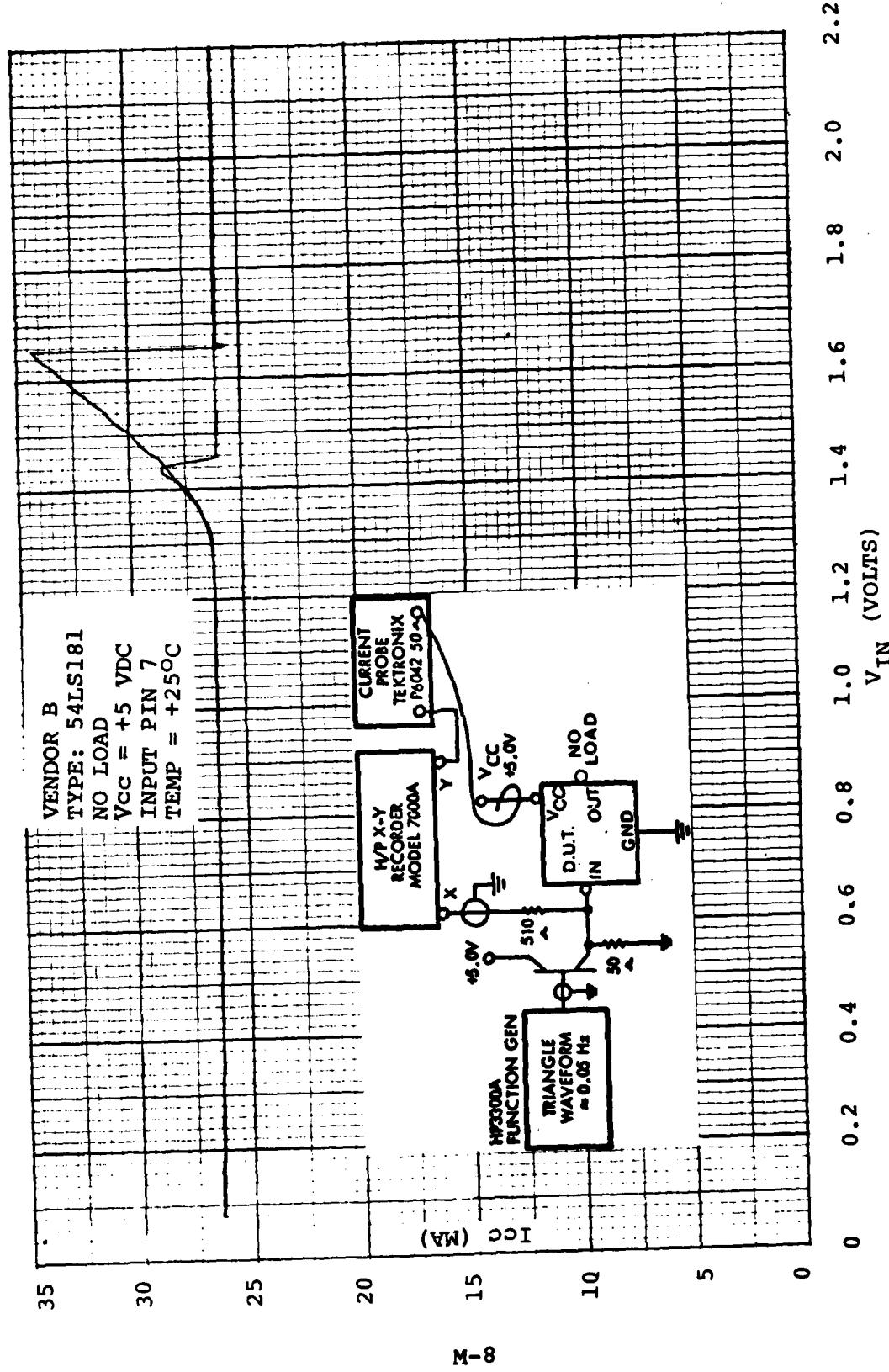
## TRANSFER CHARACTERISTICS



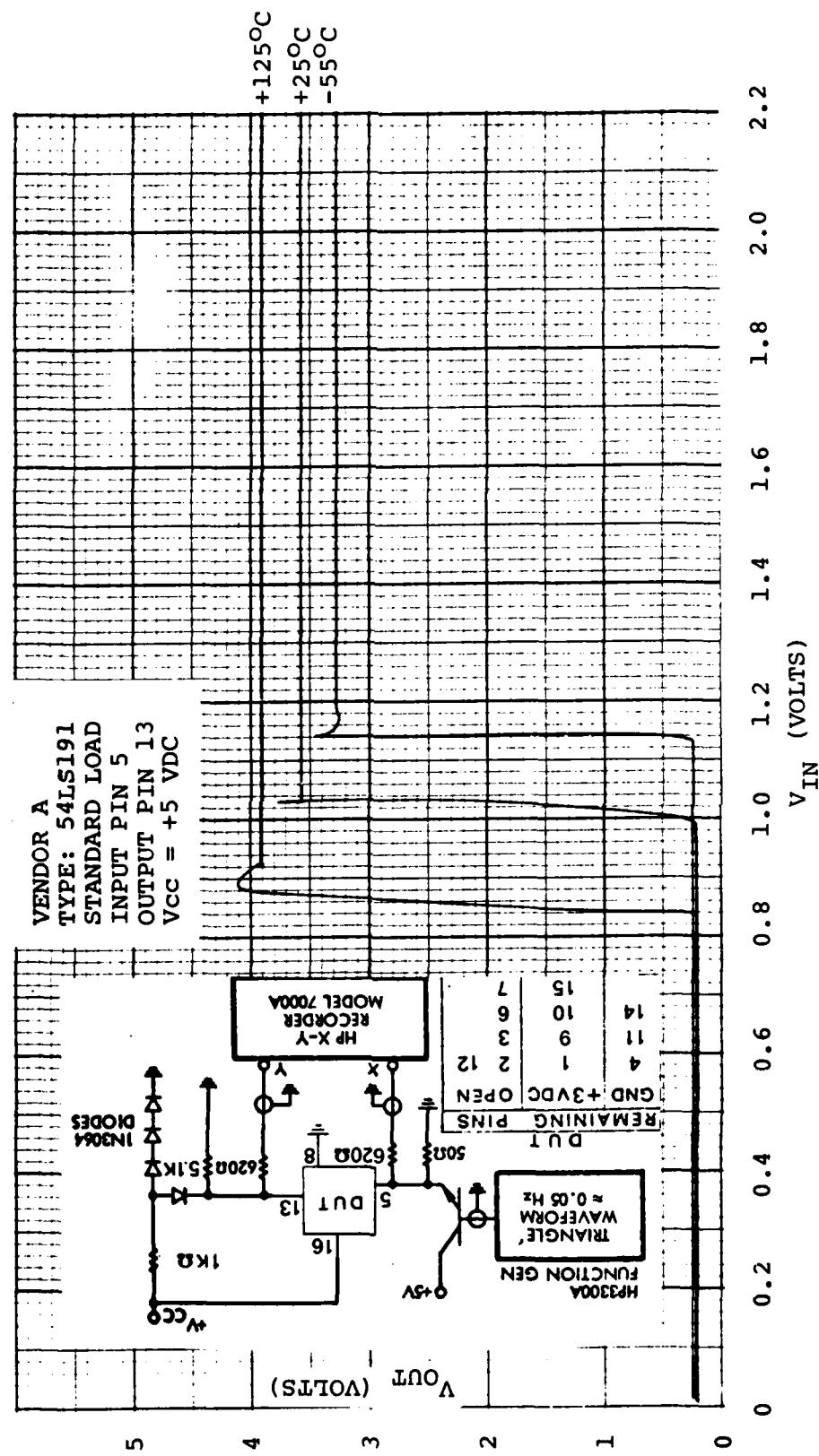
**TRANSFER CHARACTERISTICS**



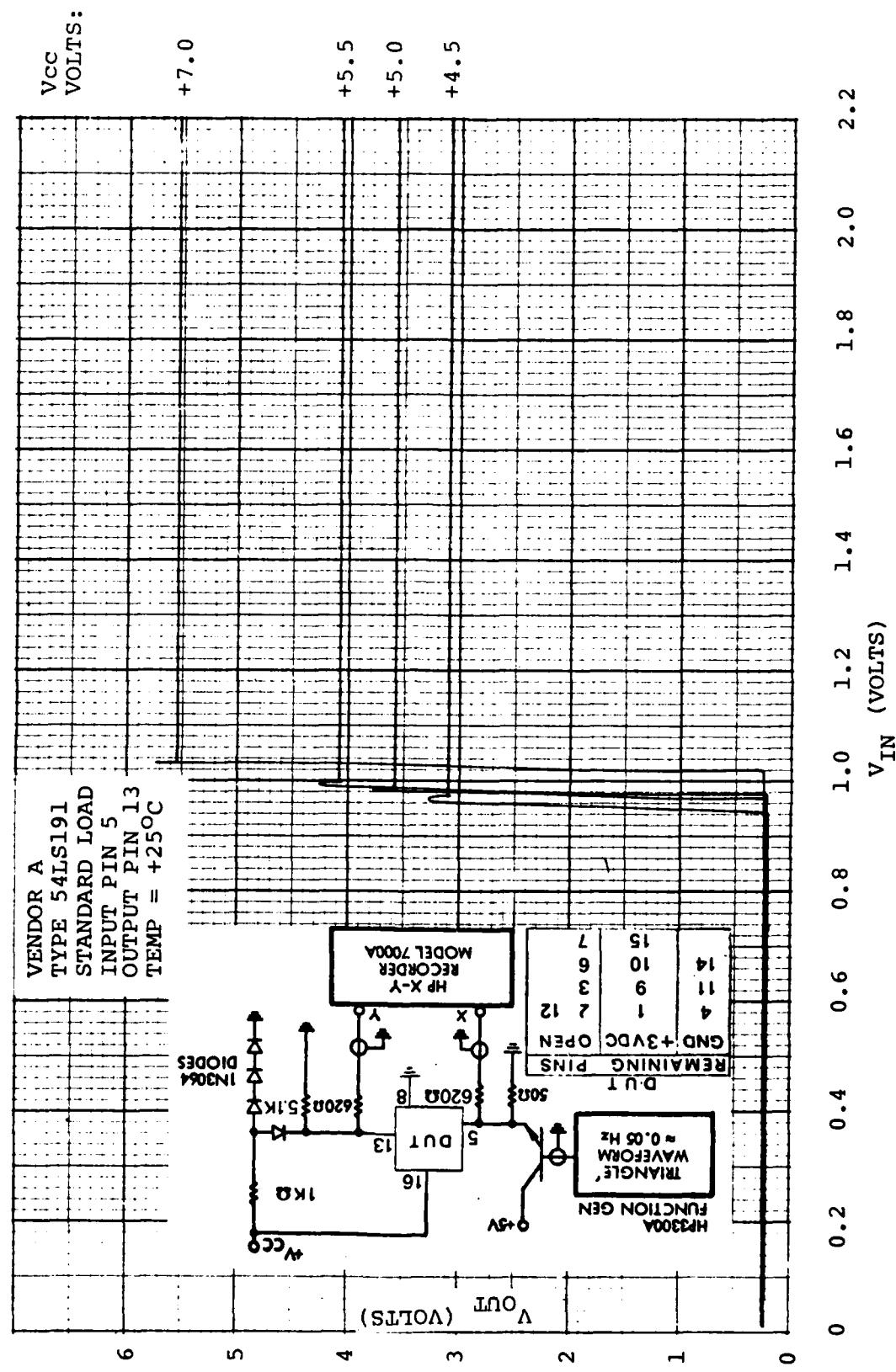
I<sub>CC</sub> VS INPUT VOLTAGE



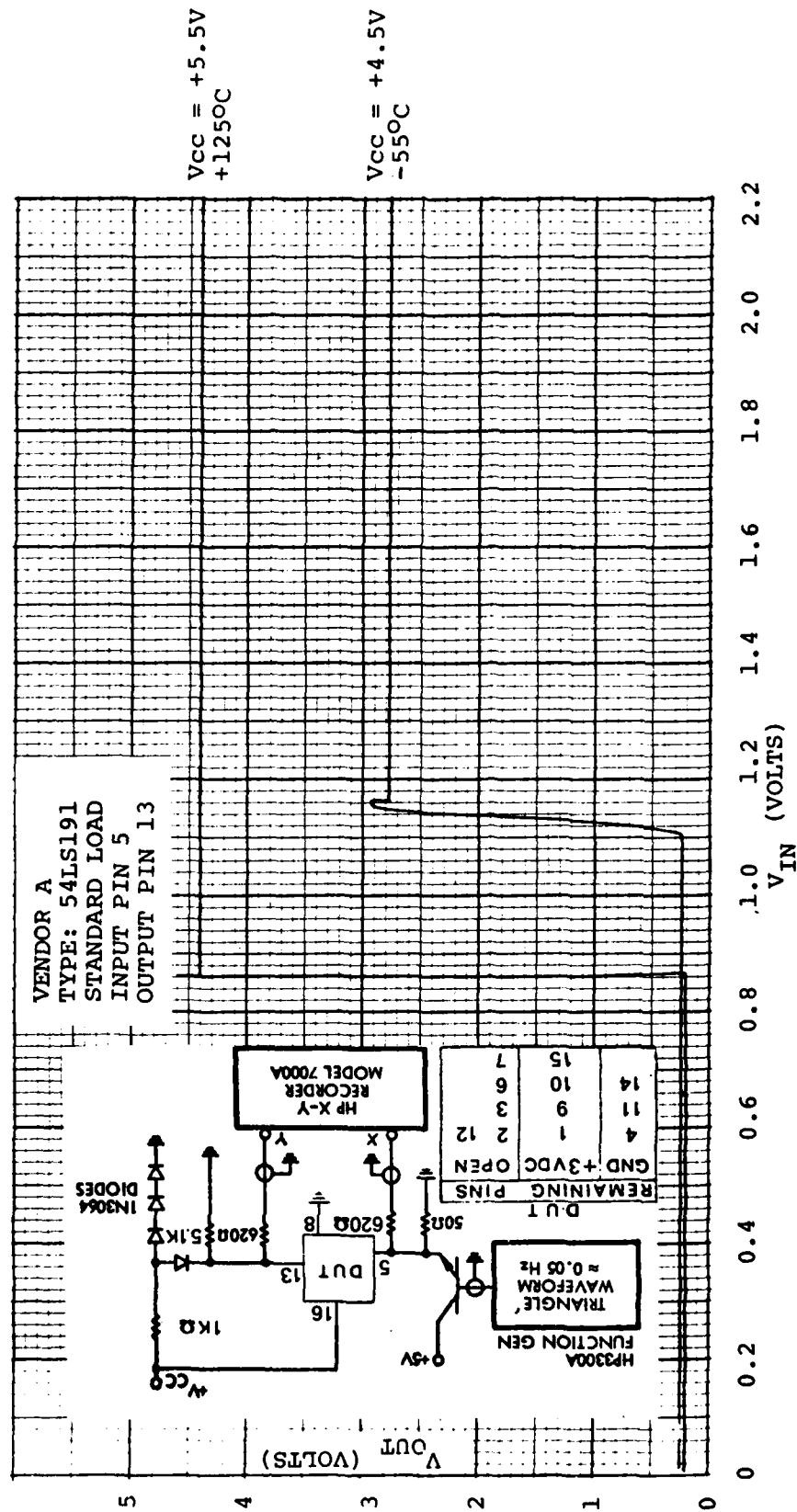
TRANSFER CHARACTERISTICS



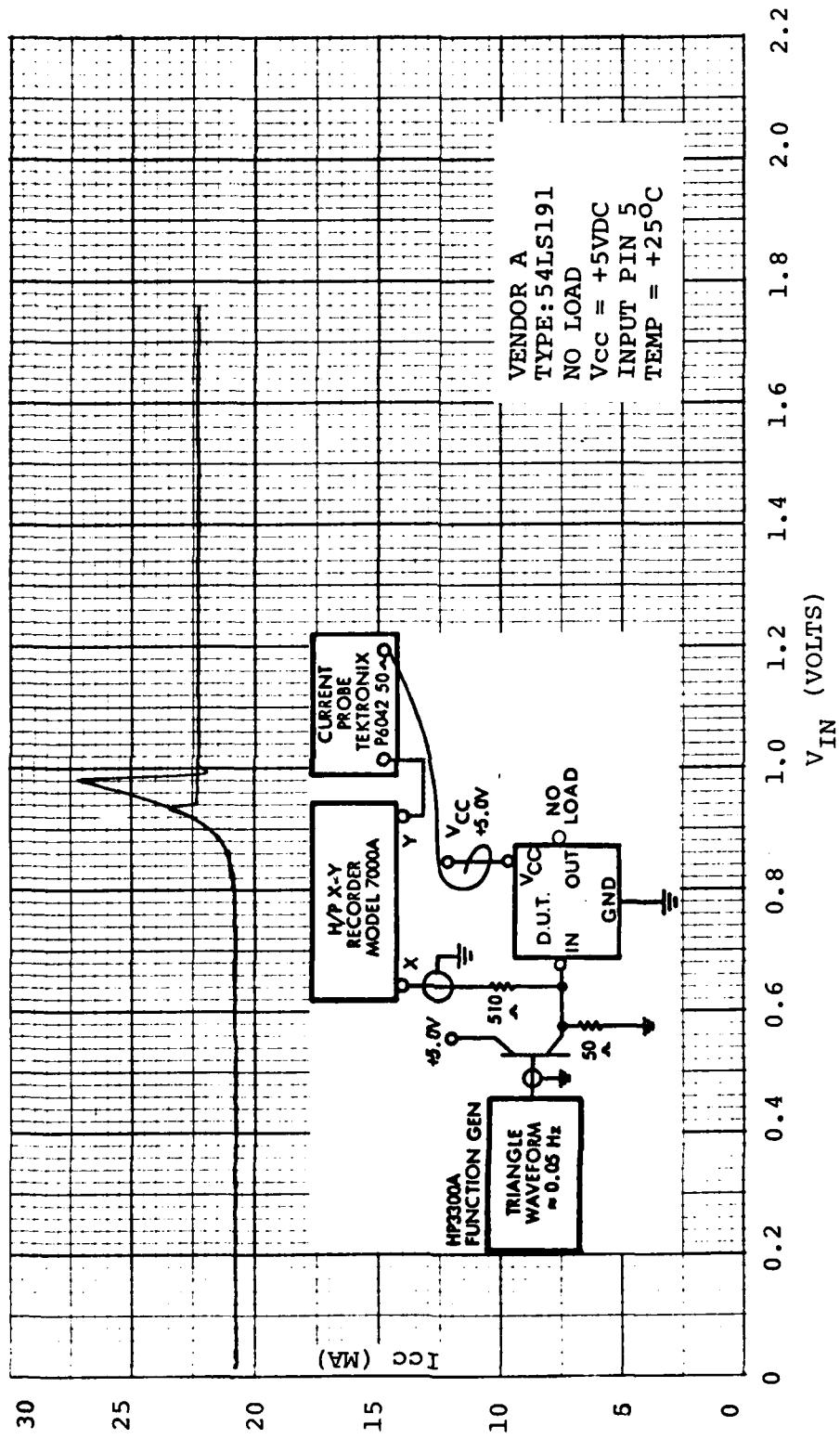
TRANSFER CHARACTERISTICS



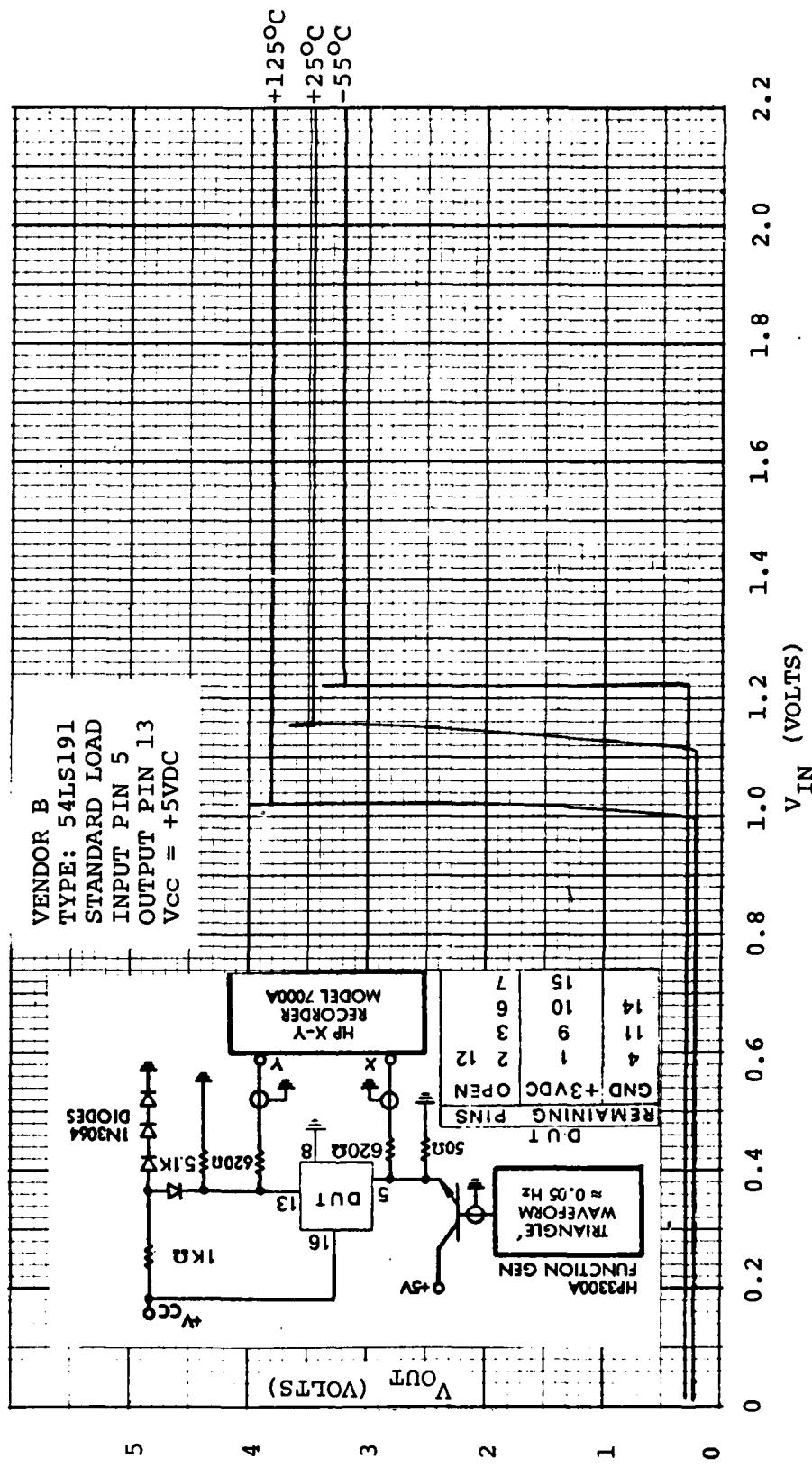
TRANSFER CHARACTERISTICS



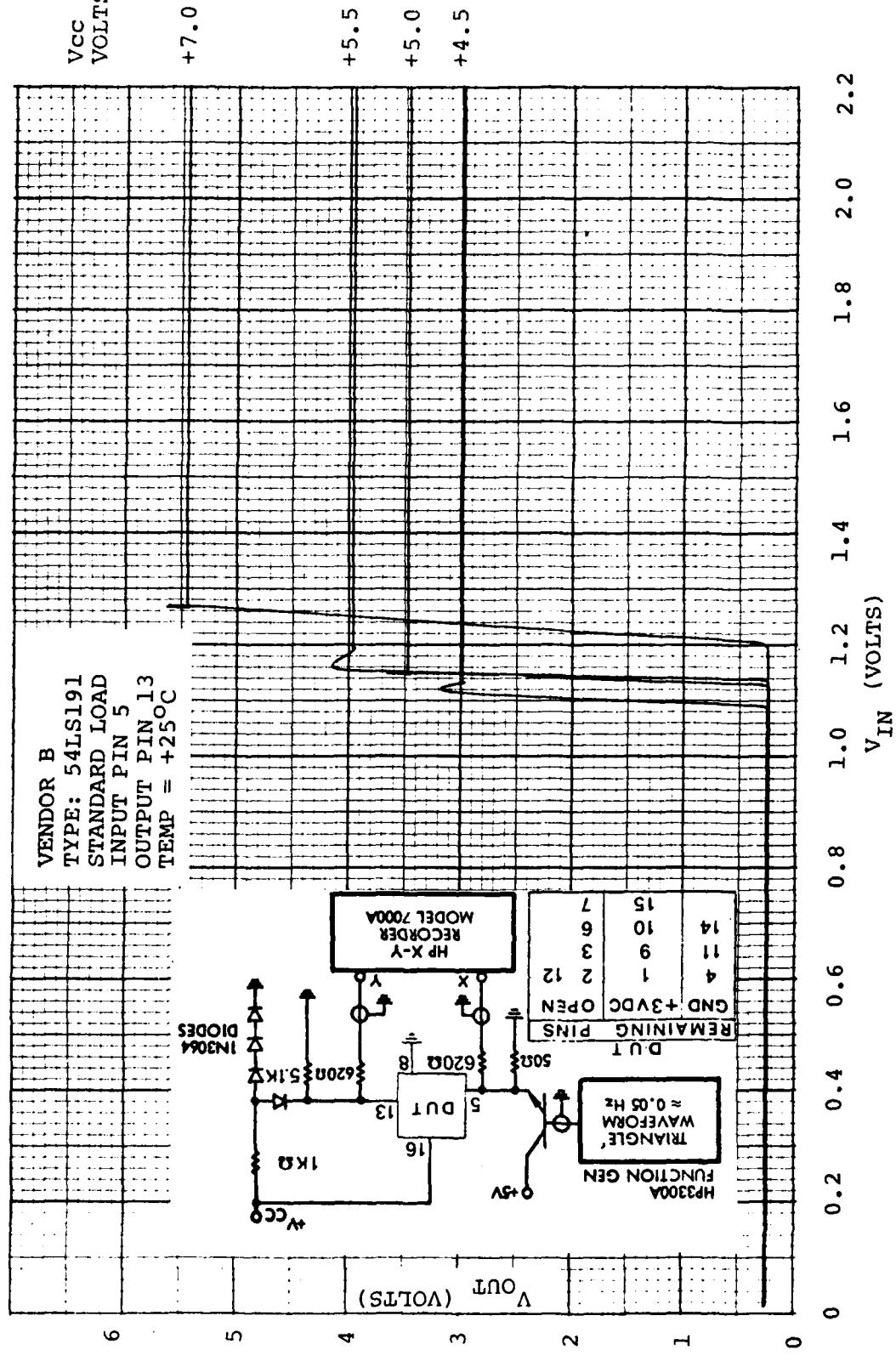
ICC VS INPUT VOLTAGE



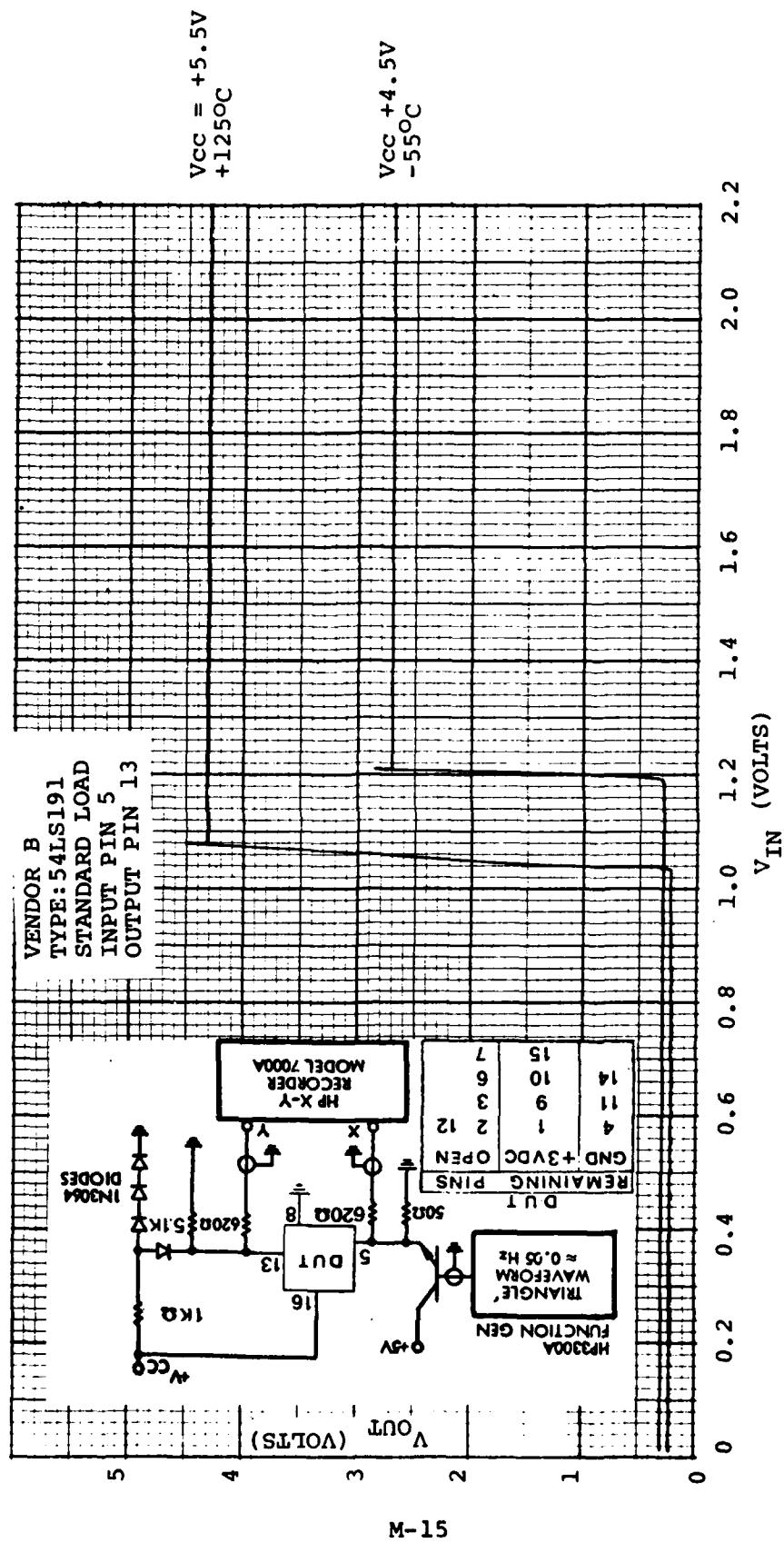
TRANSFER CHARACTERISTICS



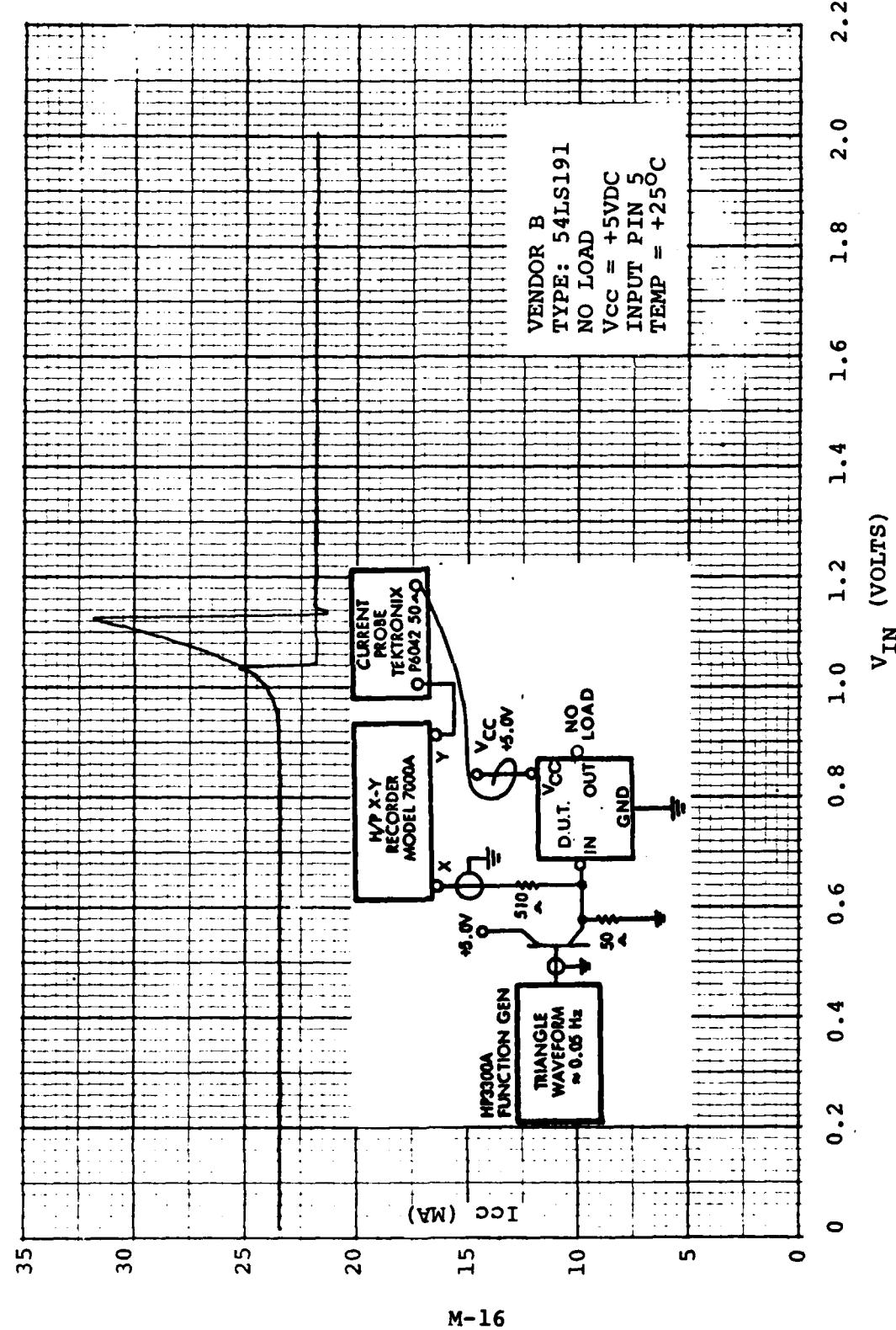
TRANSFER CHARACTERISTICS



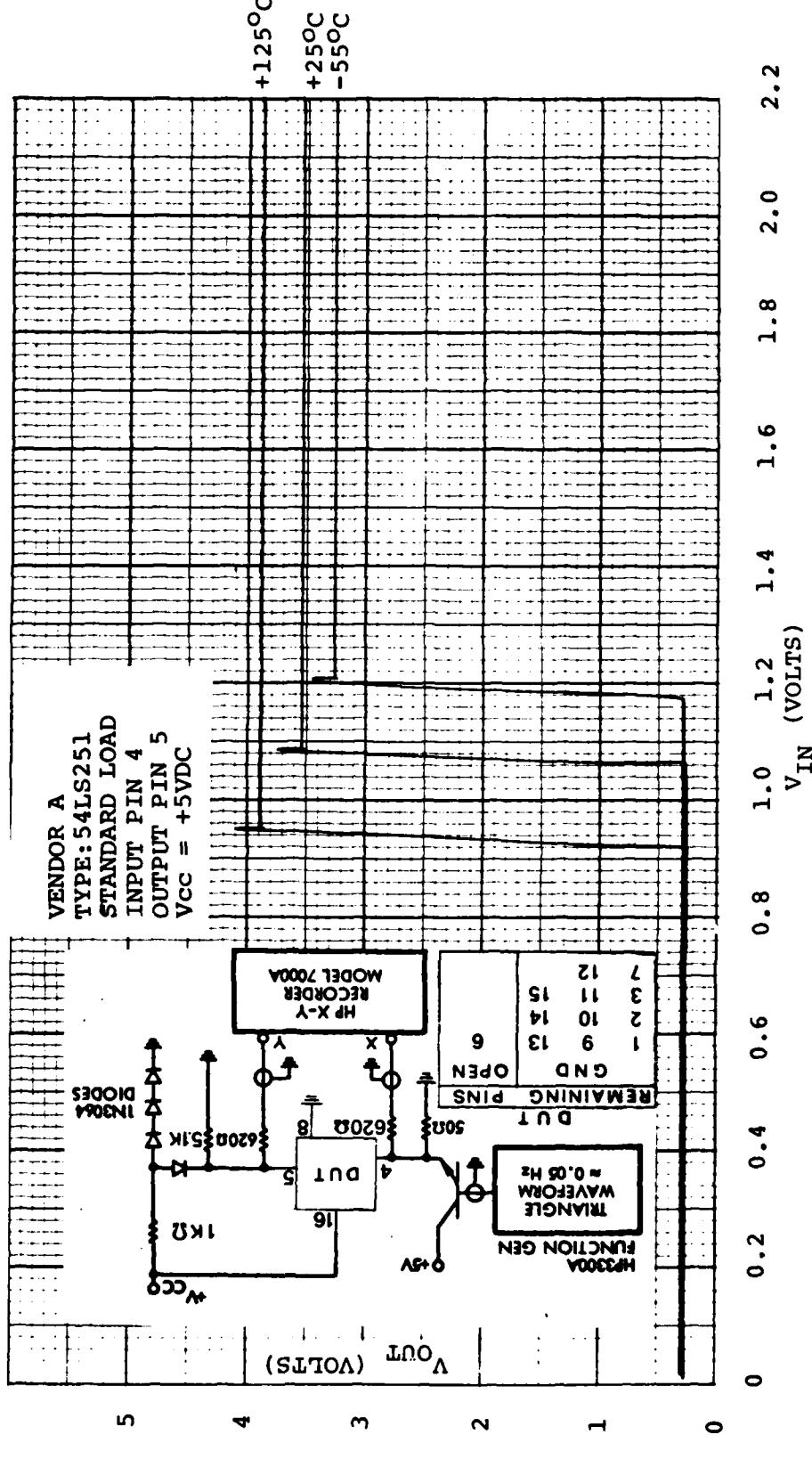
TRANSFER CHARACTERISTICS



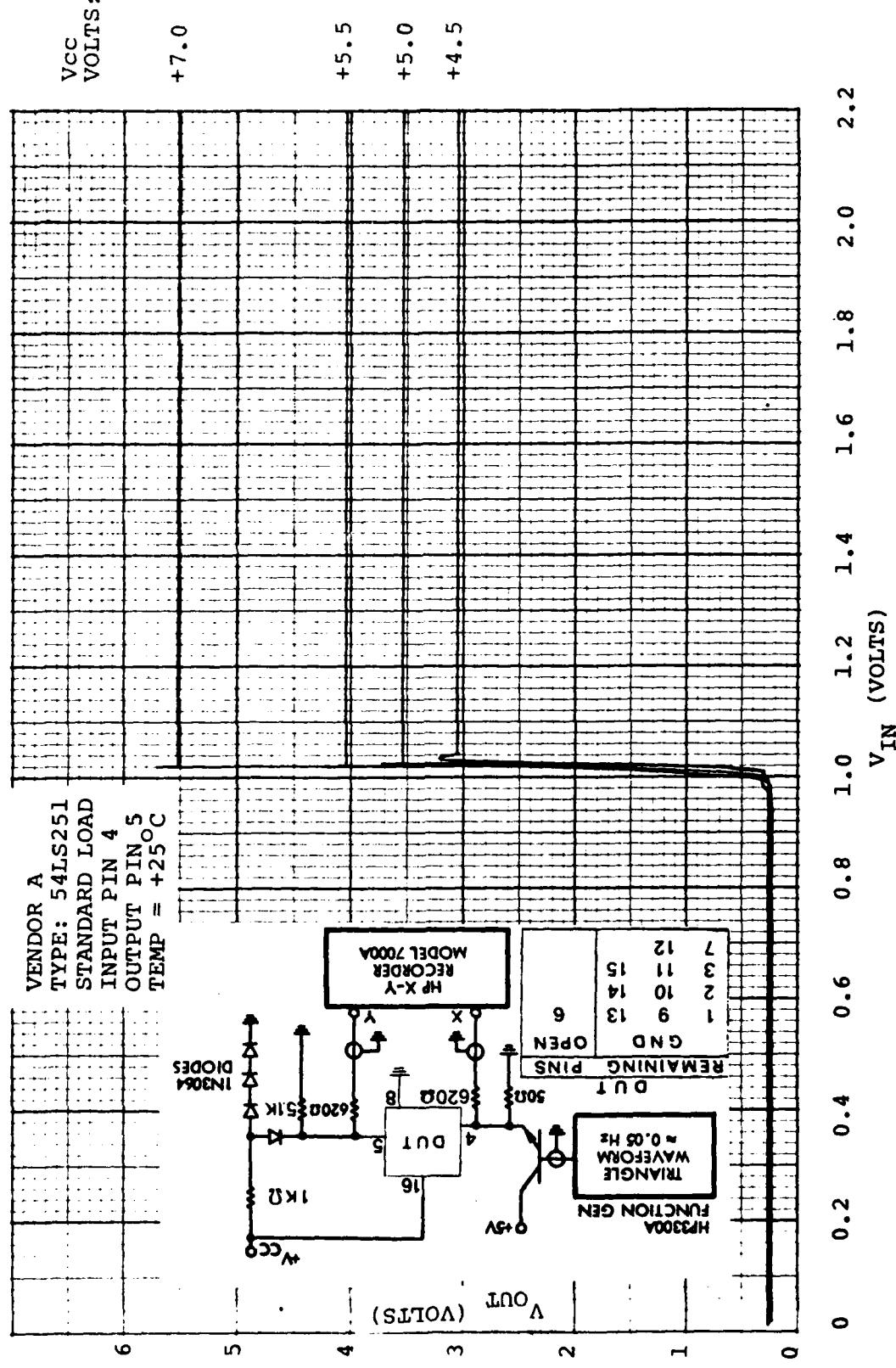
ICC VS INPUT VOLTAGE



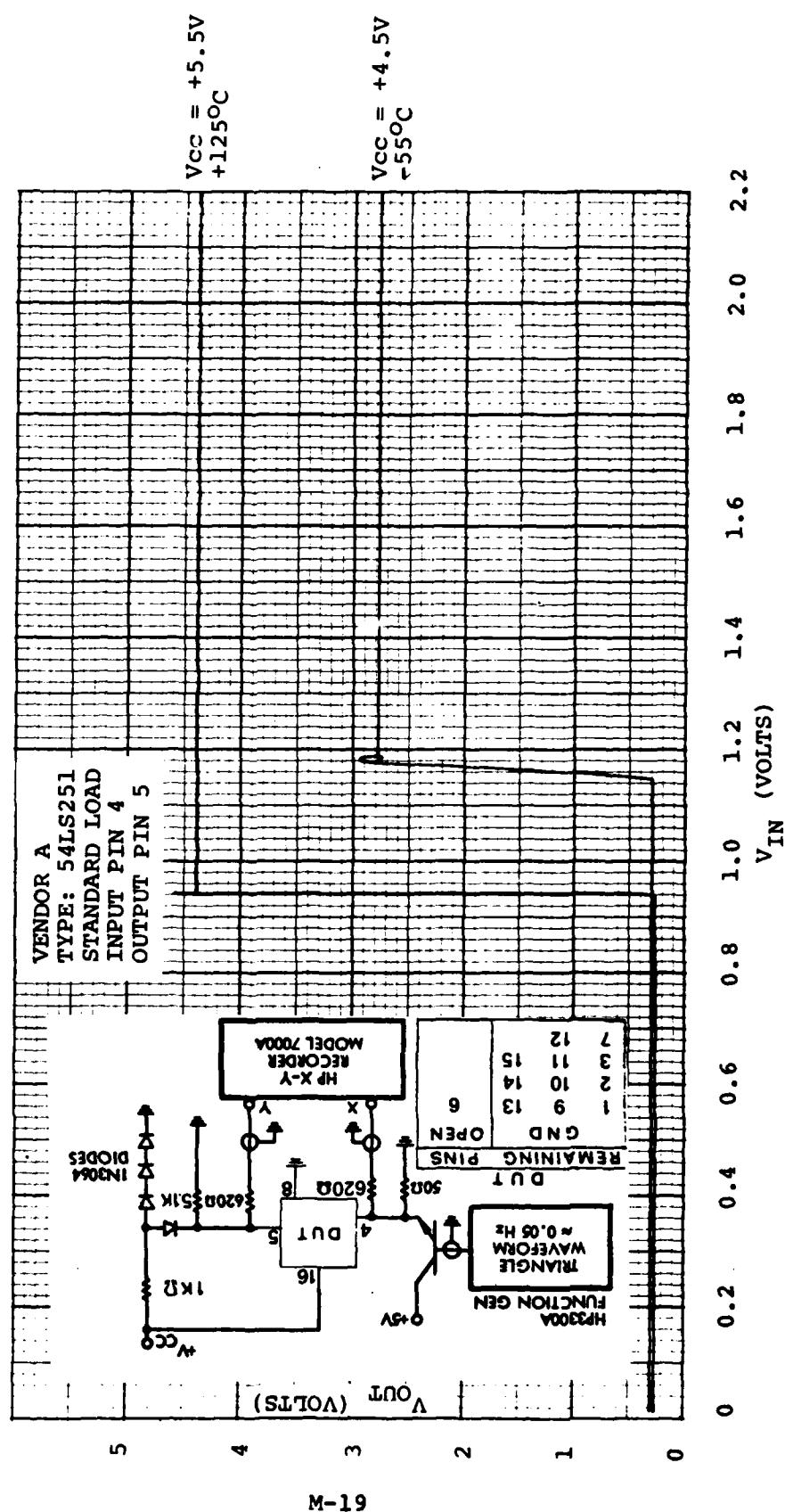
TRANSFER CHARACTERISTICS



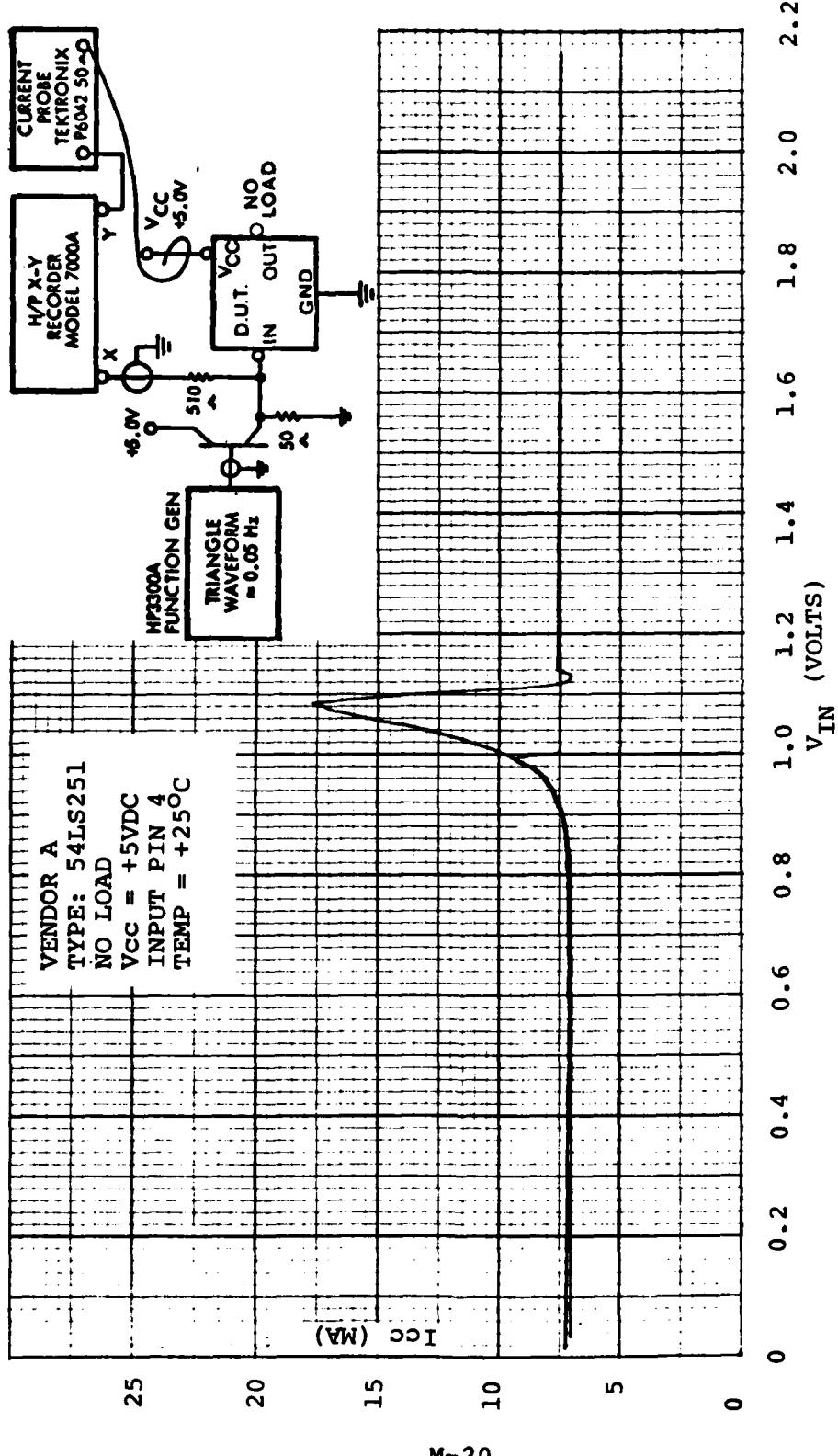
TRANSFER CHARACTERISTICS



TRANSFER CHARACTERISTICS

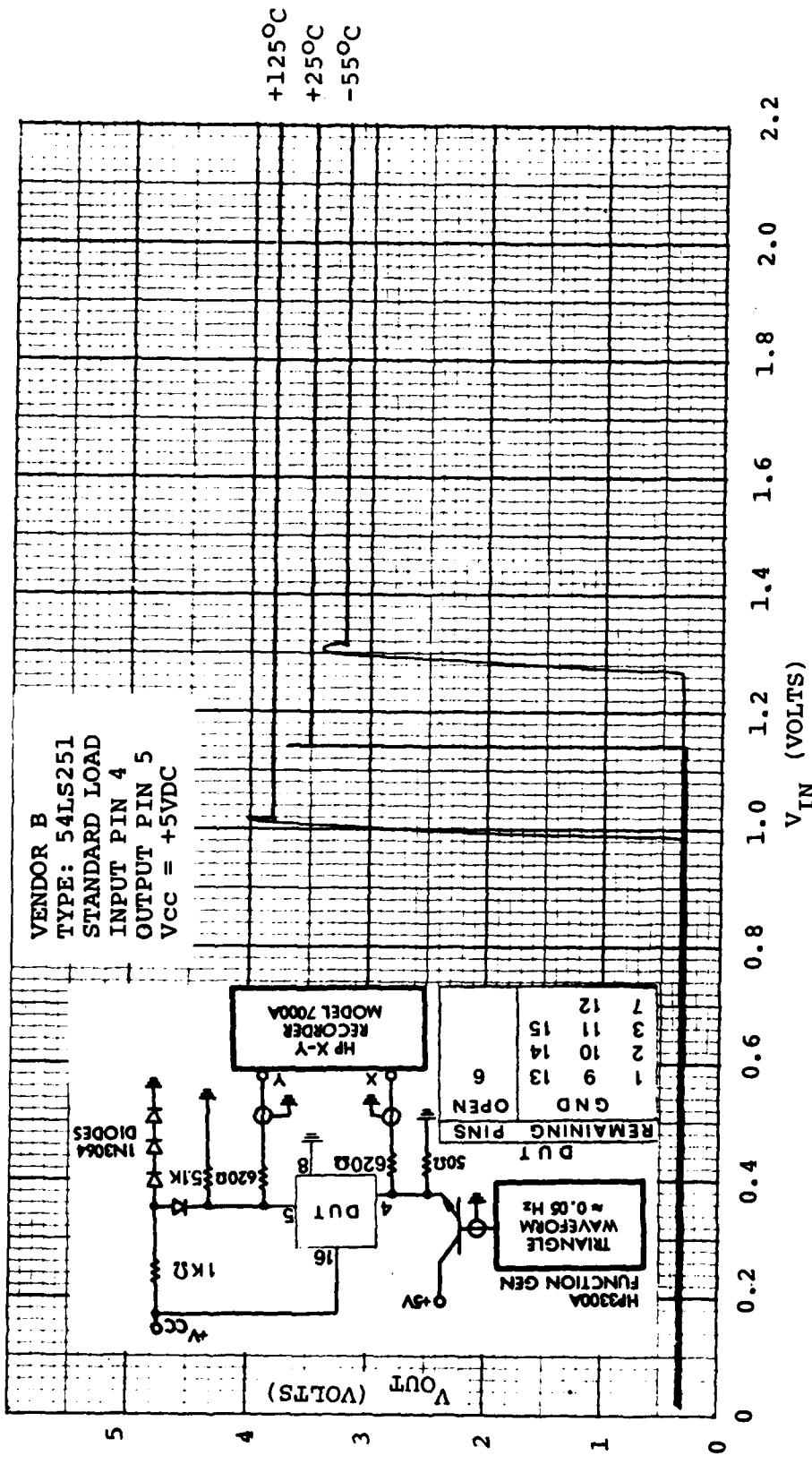


I<sub>CC</sub> VS INPUT VOLTAGE

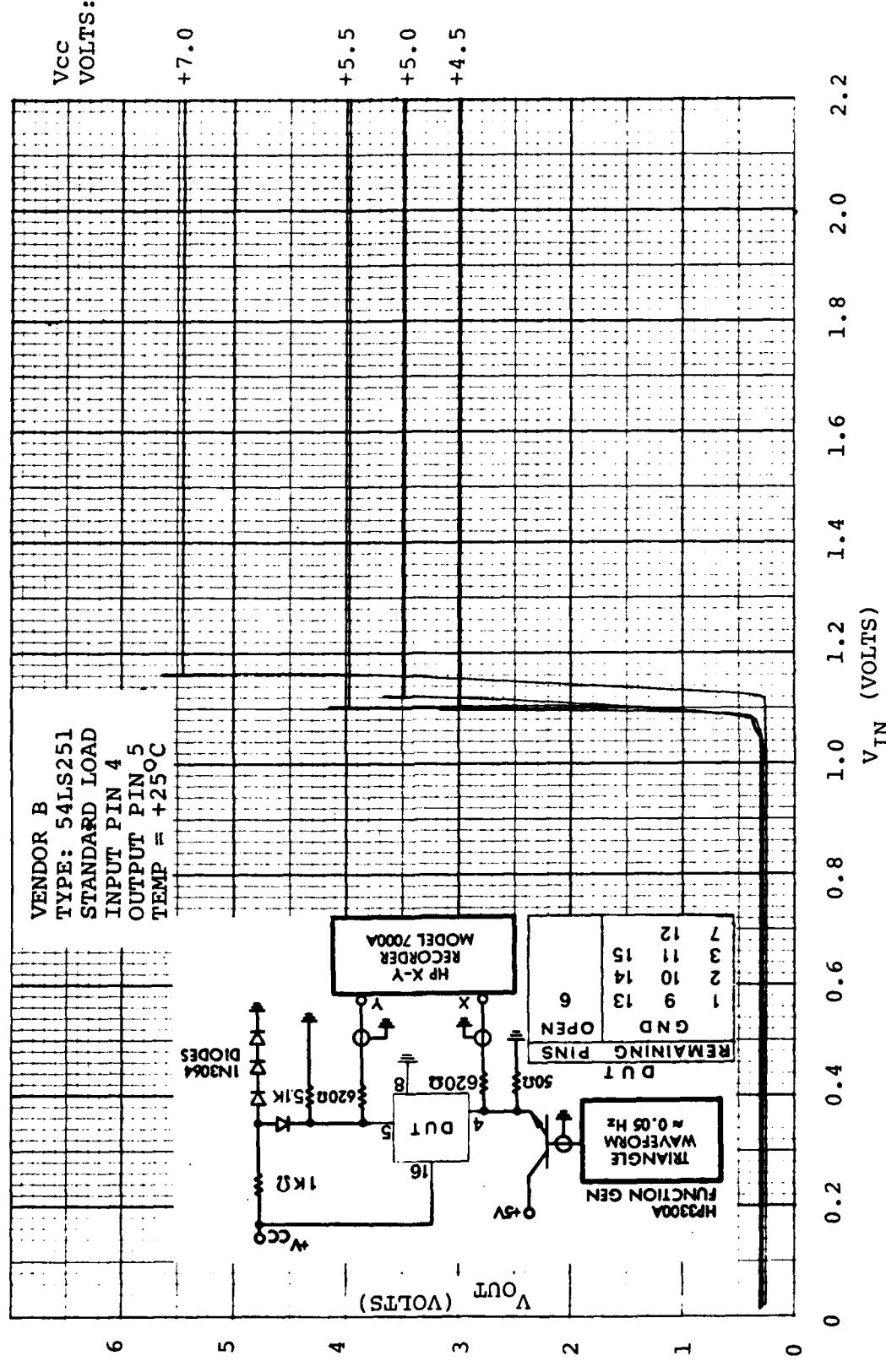


M-20

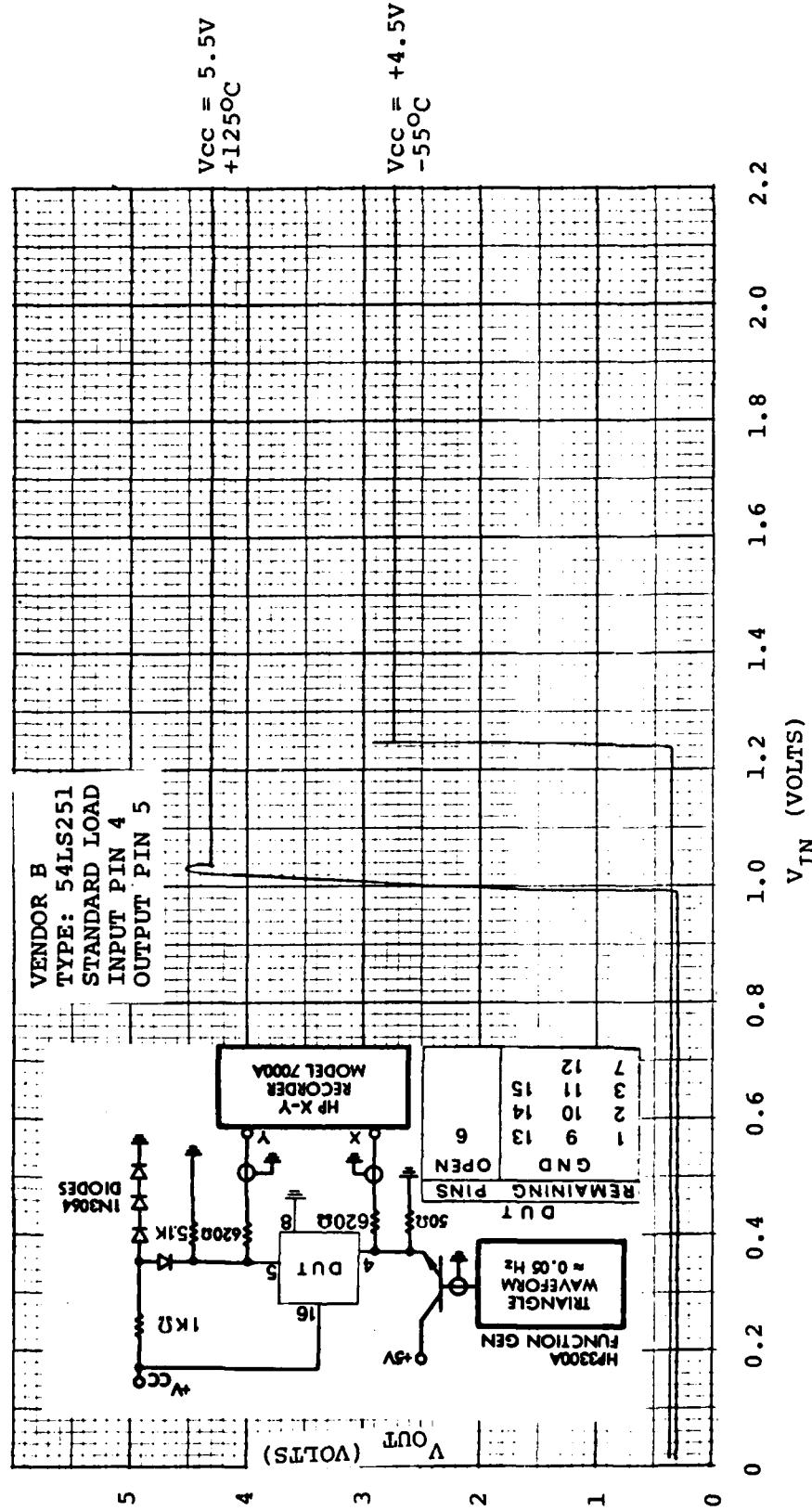
TRANSFER CHARACTERISTICS



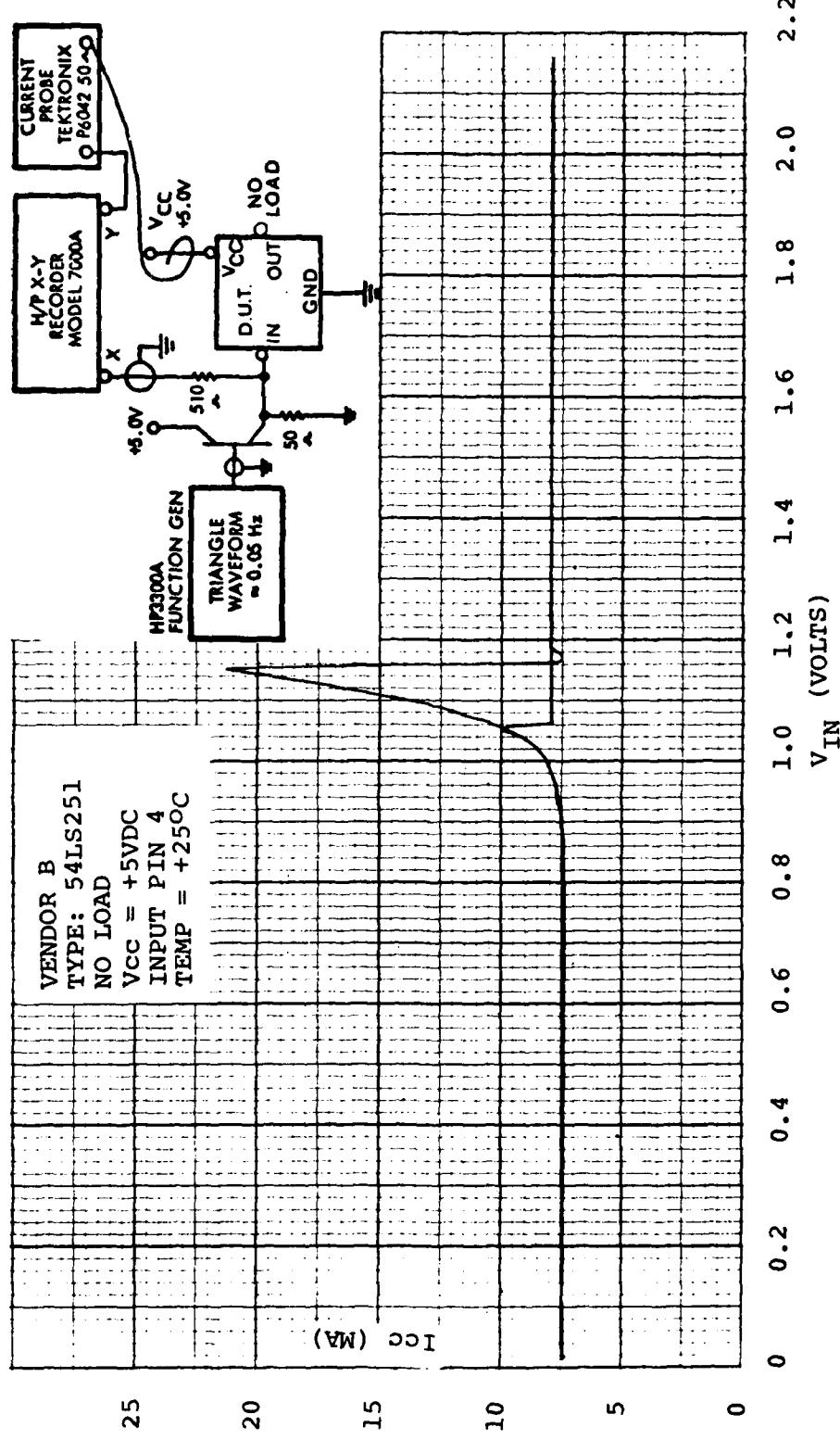
TRANSFER CHARACTERISTICS



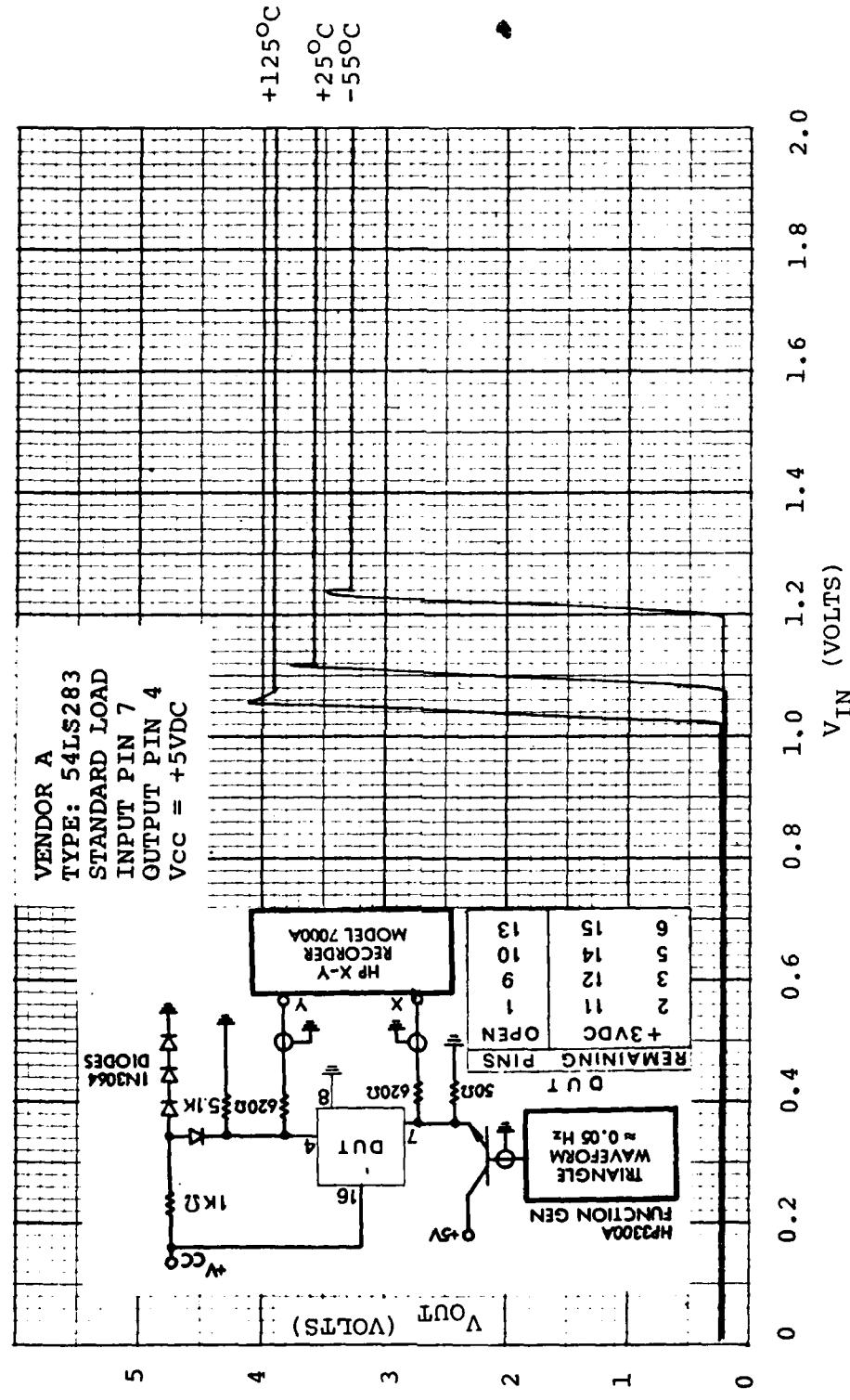
TRANSFER CHARACTERISTICS



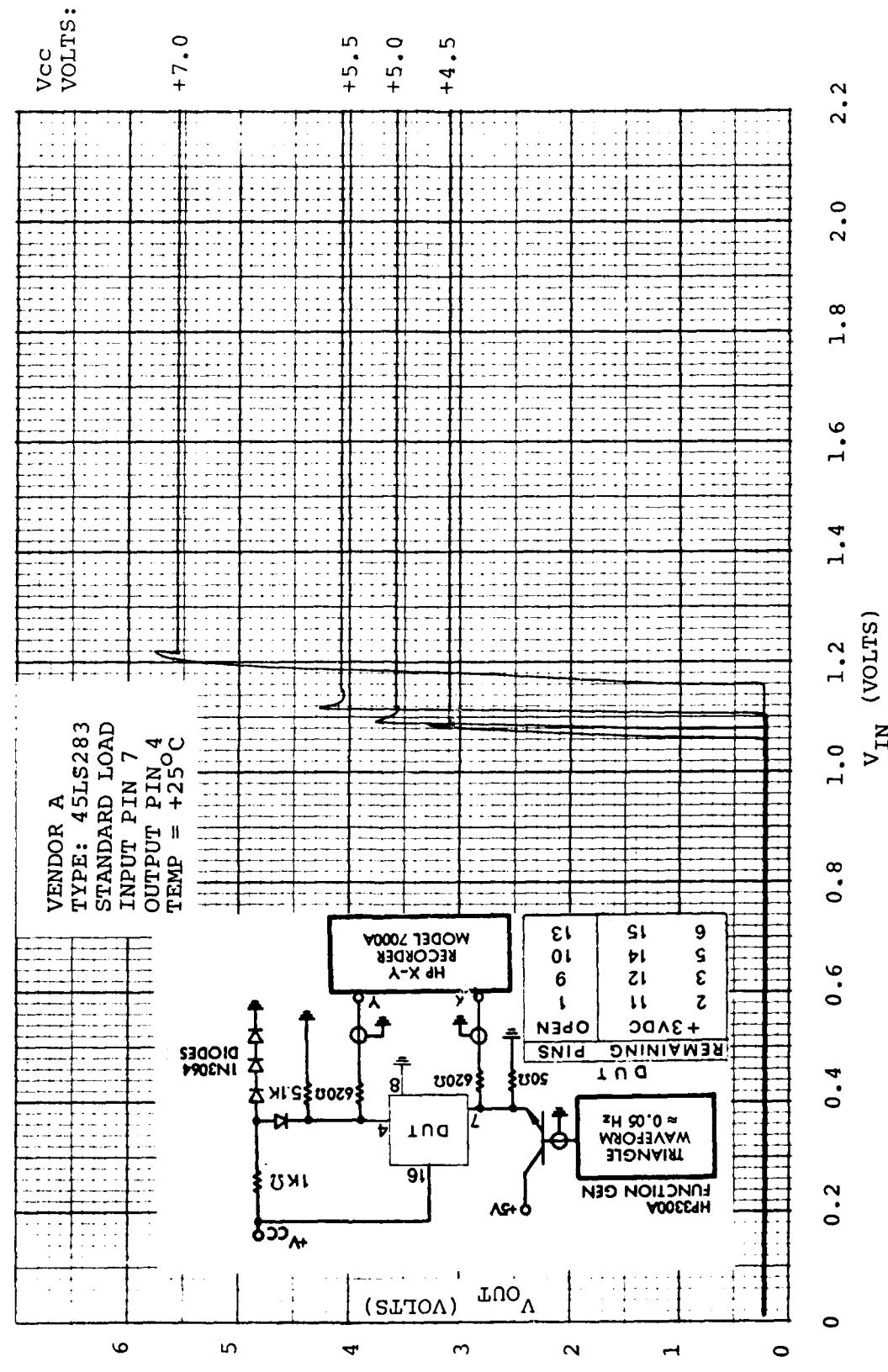
I<sub>CC</sub> VS INPUT VOLTAGE



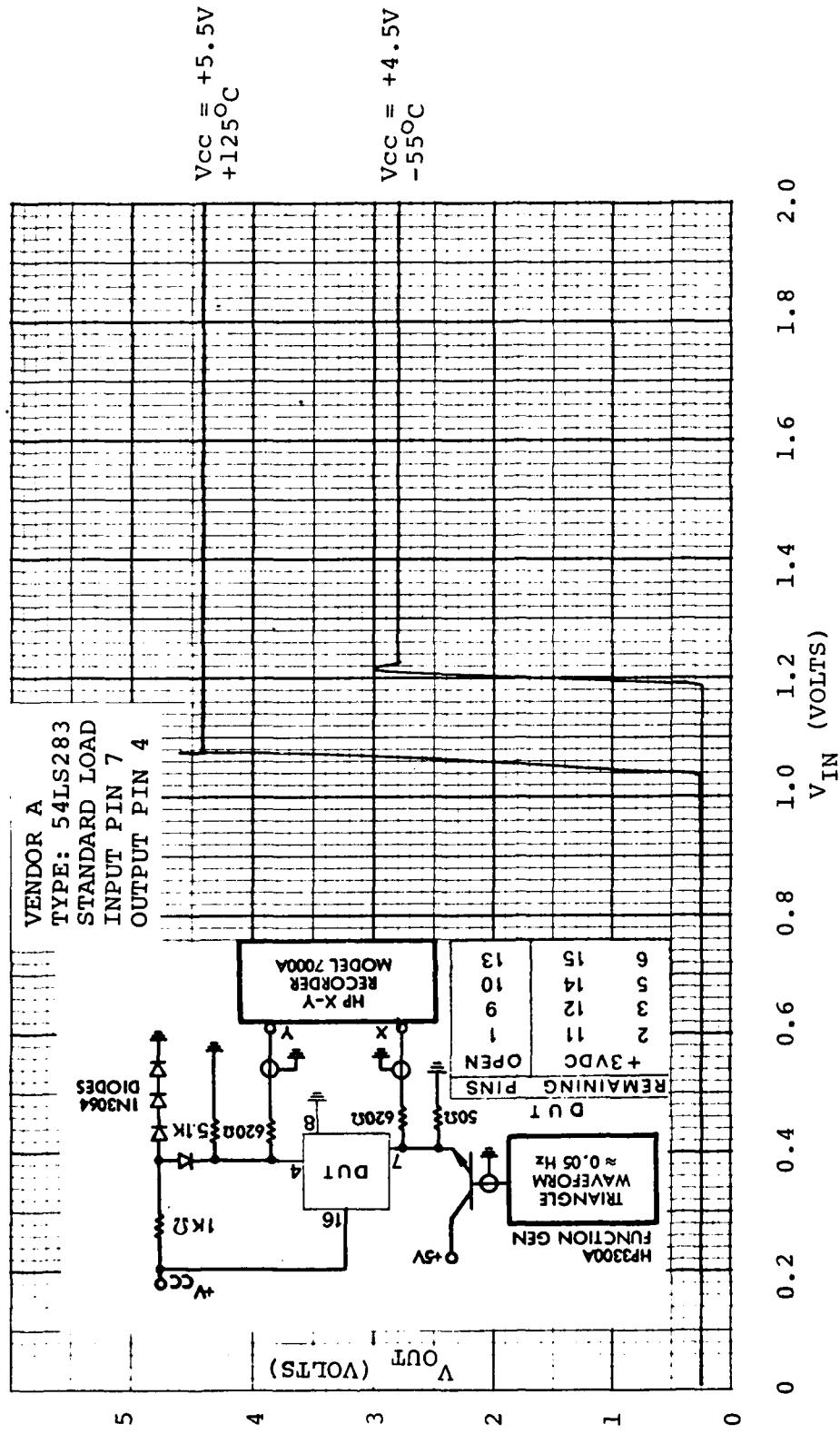
TRANSFER CHARACTERISTICS



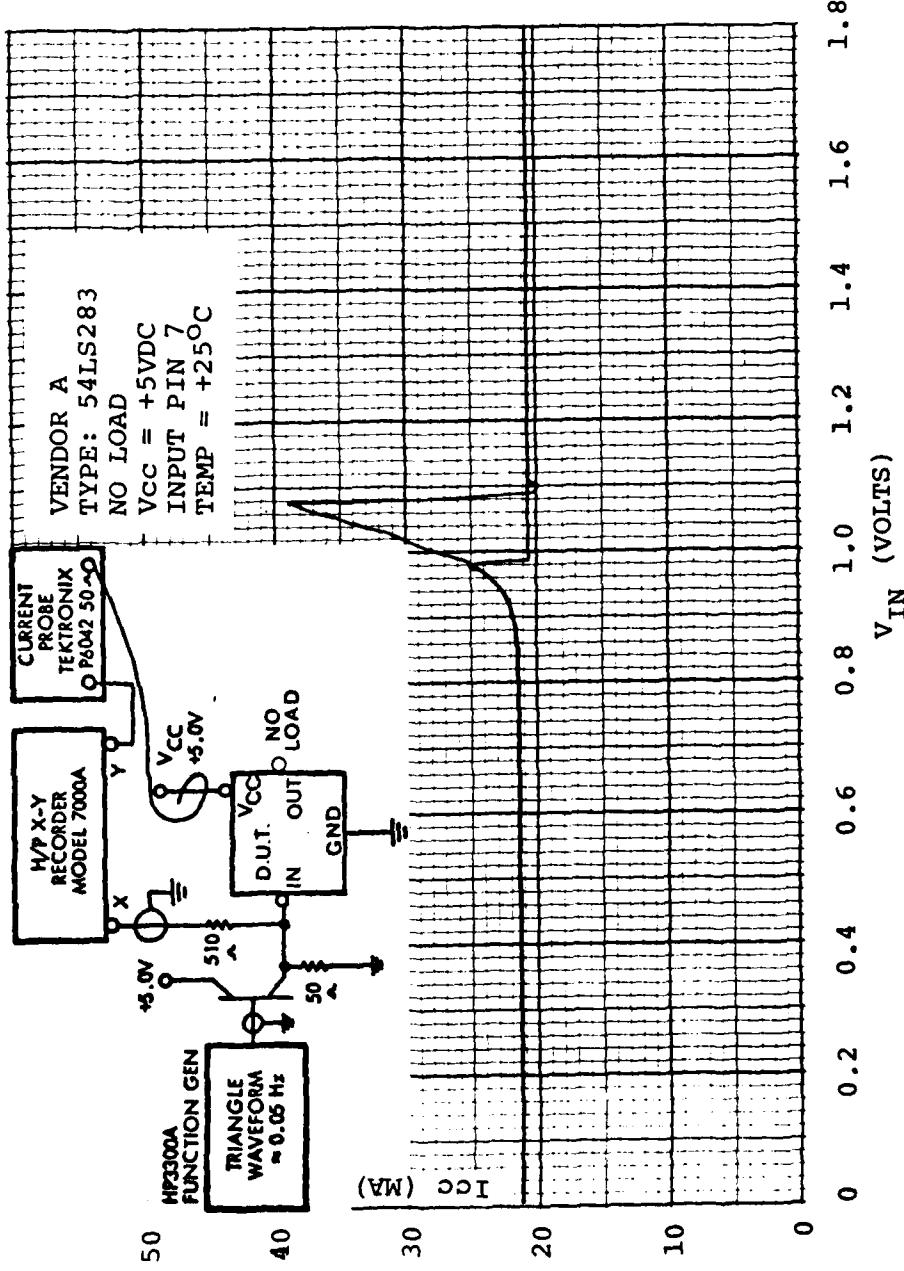
TRANSFER CHARACTERISTICS



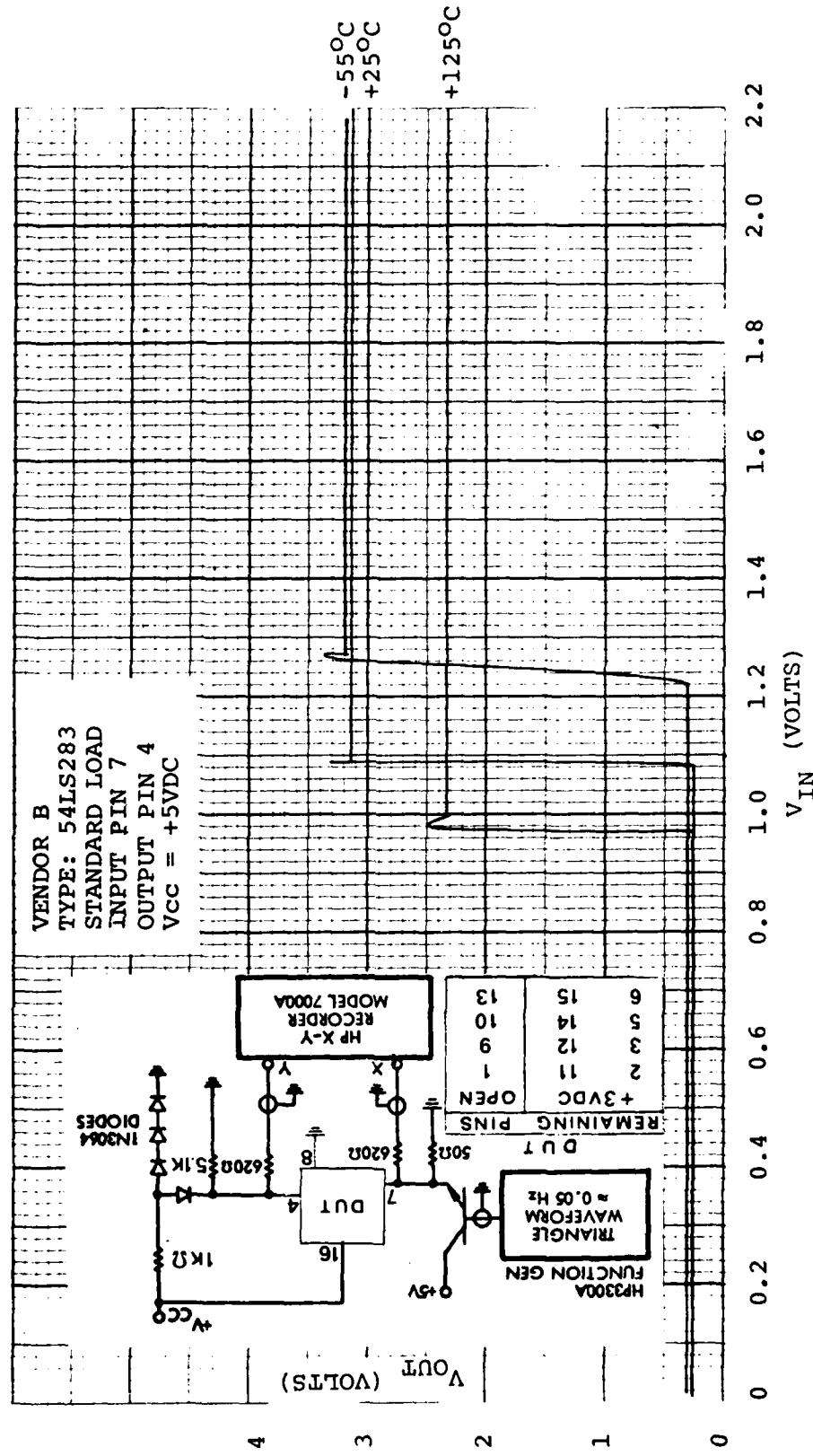
TRANSFER CHARACTERISTICS



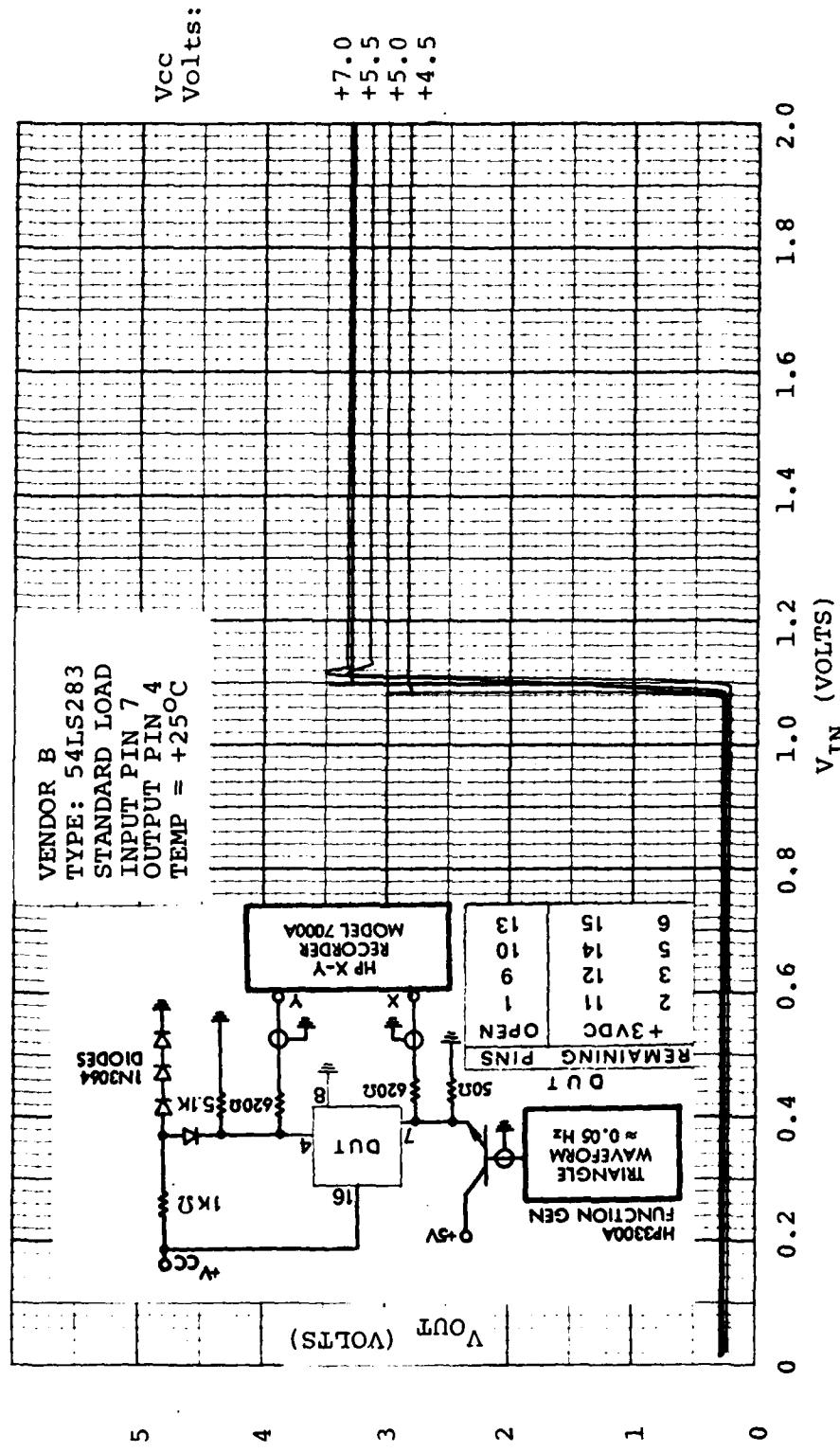
I<sub>CC</sub> VS INPUT VOLTAGE



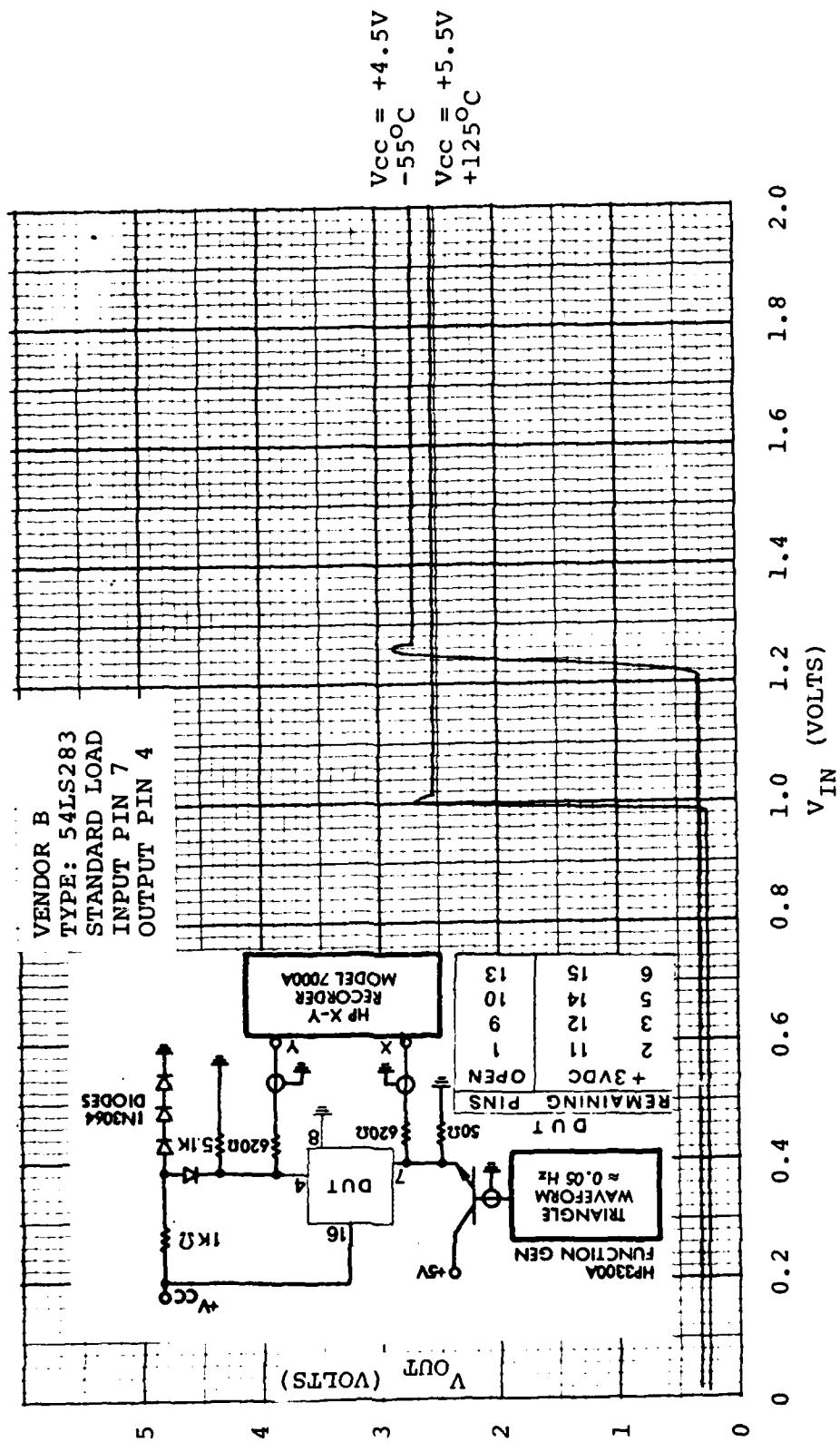
TRANSFER CHARACTERISTICS



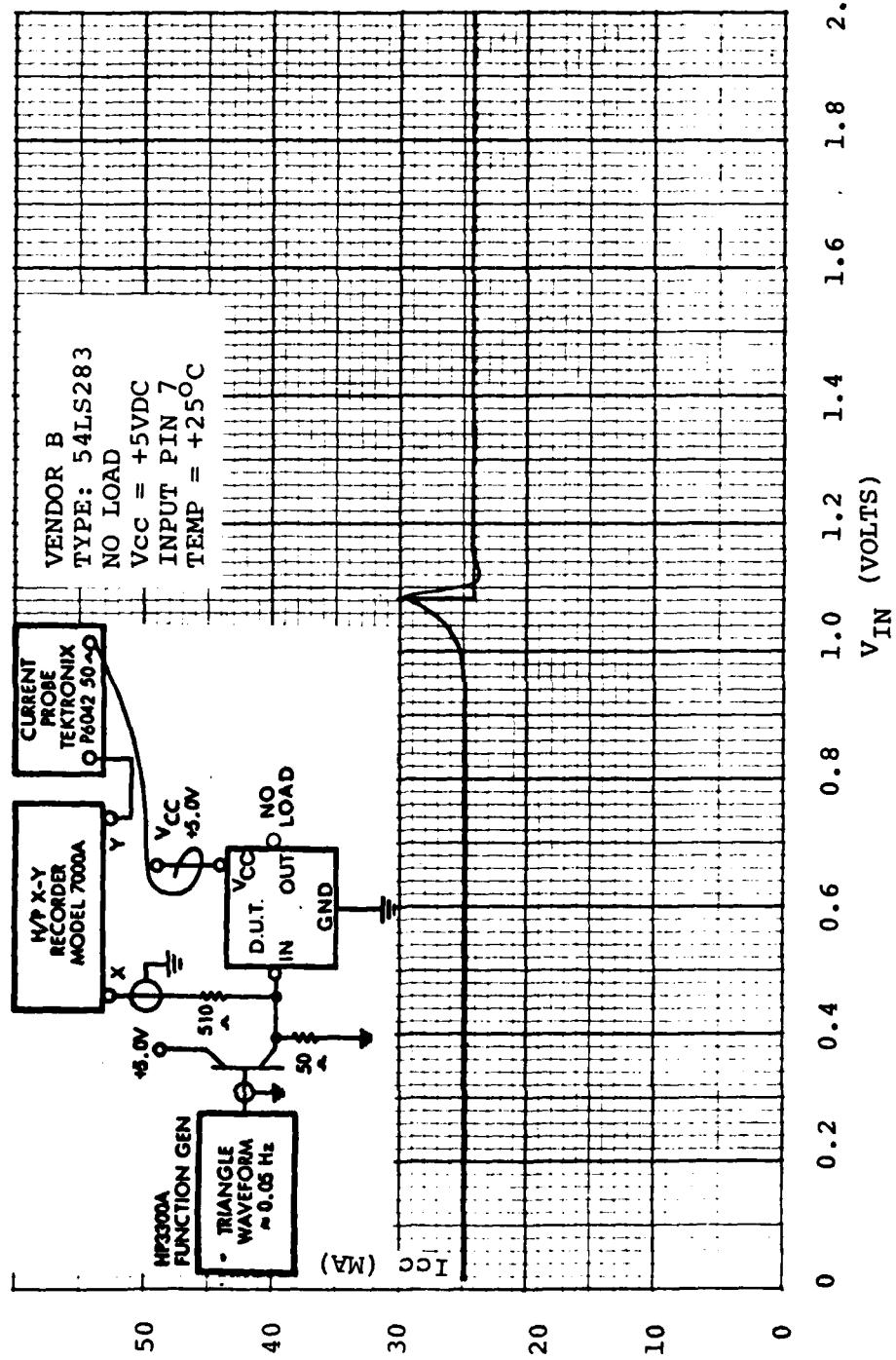
TRANSFER CHARACTERISTICS



TRANSFER CHARACTERISTICS

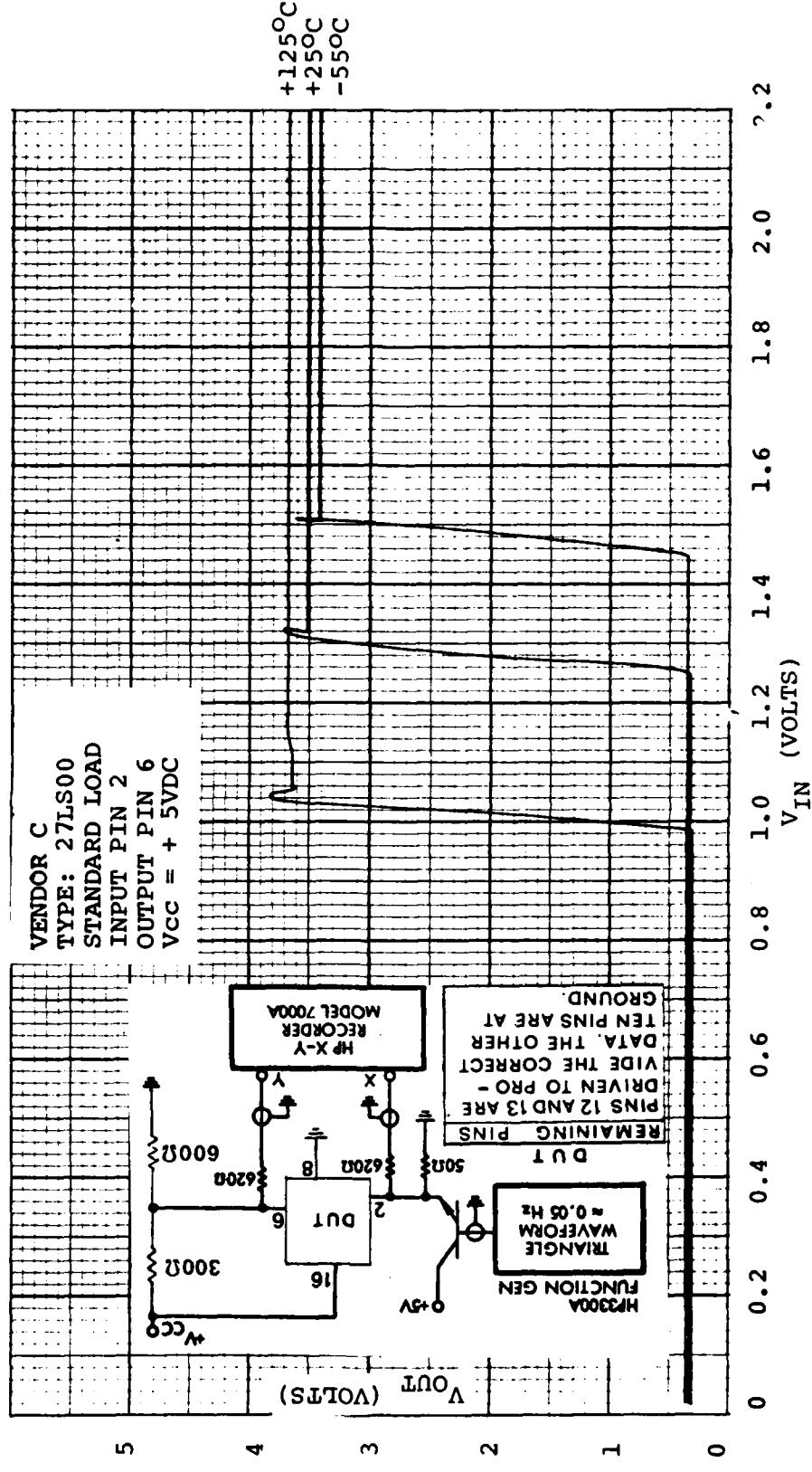


ICC VS INPUT VOLTAGE

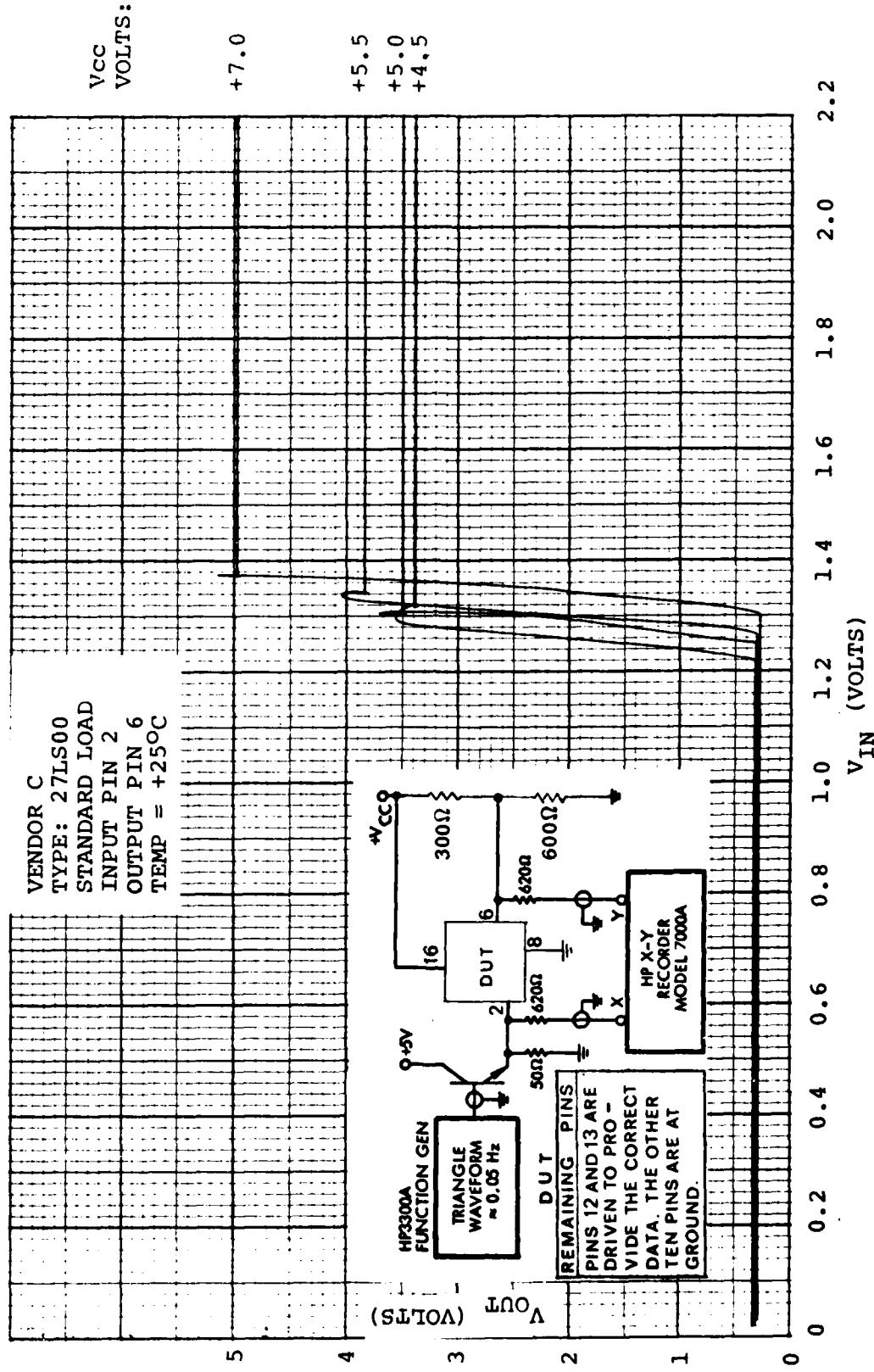


M-32

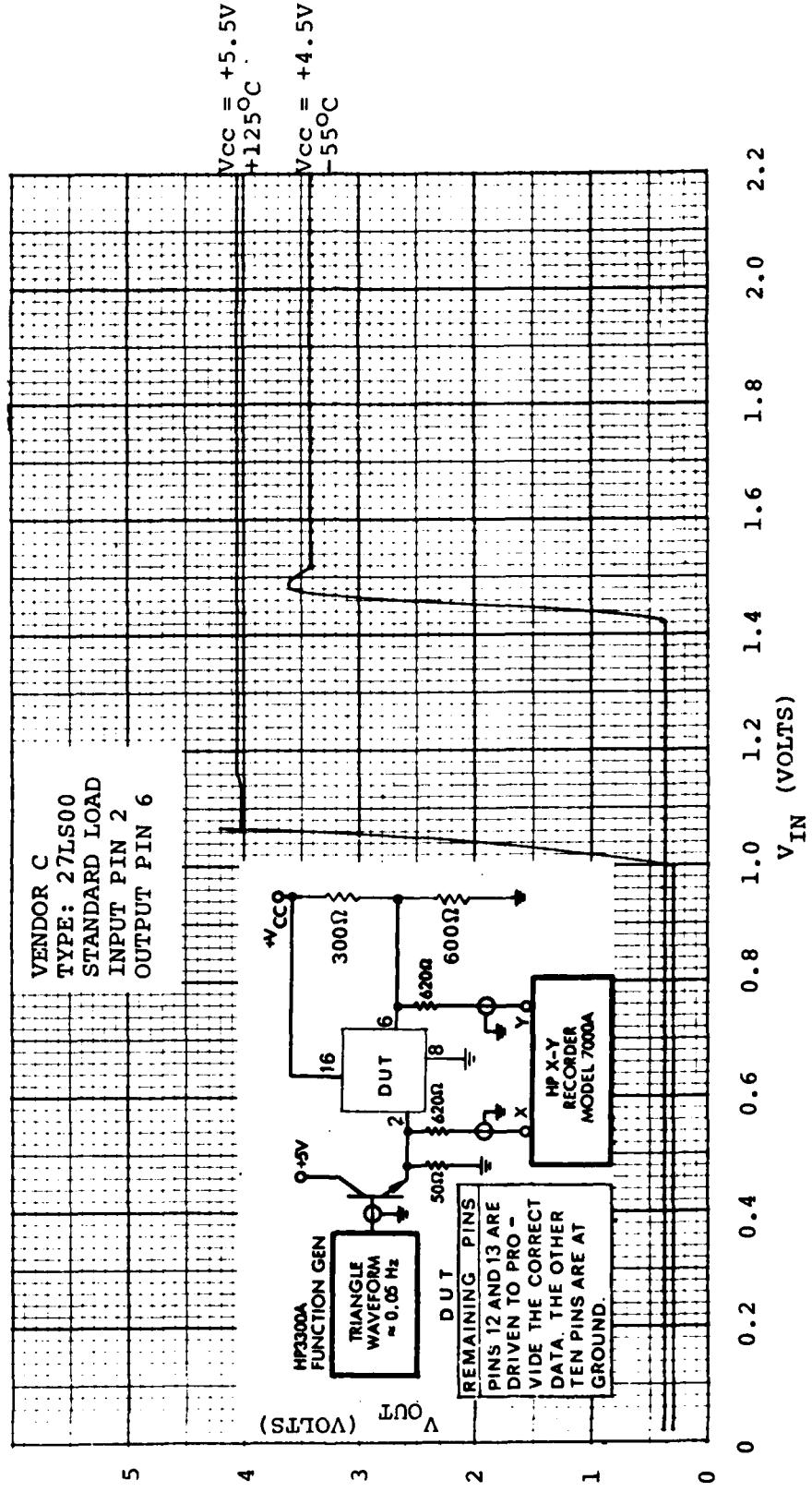
TRANSFER CHARACTERISTICS



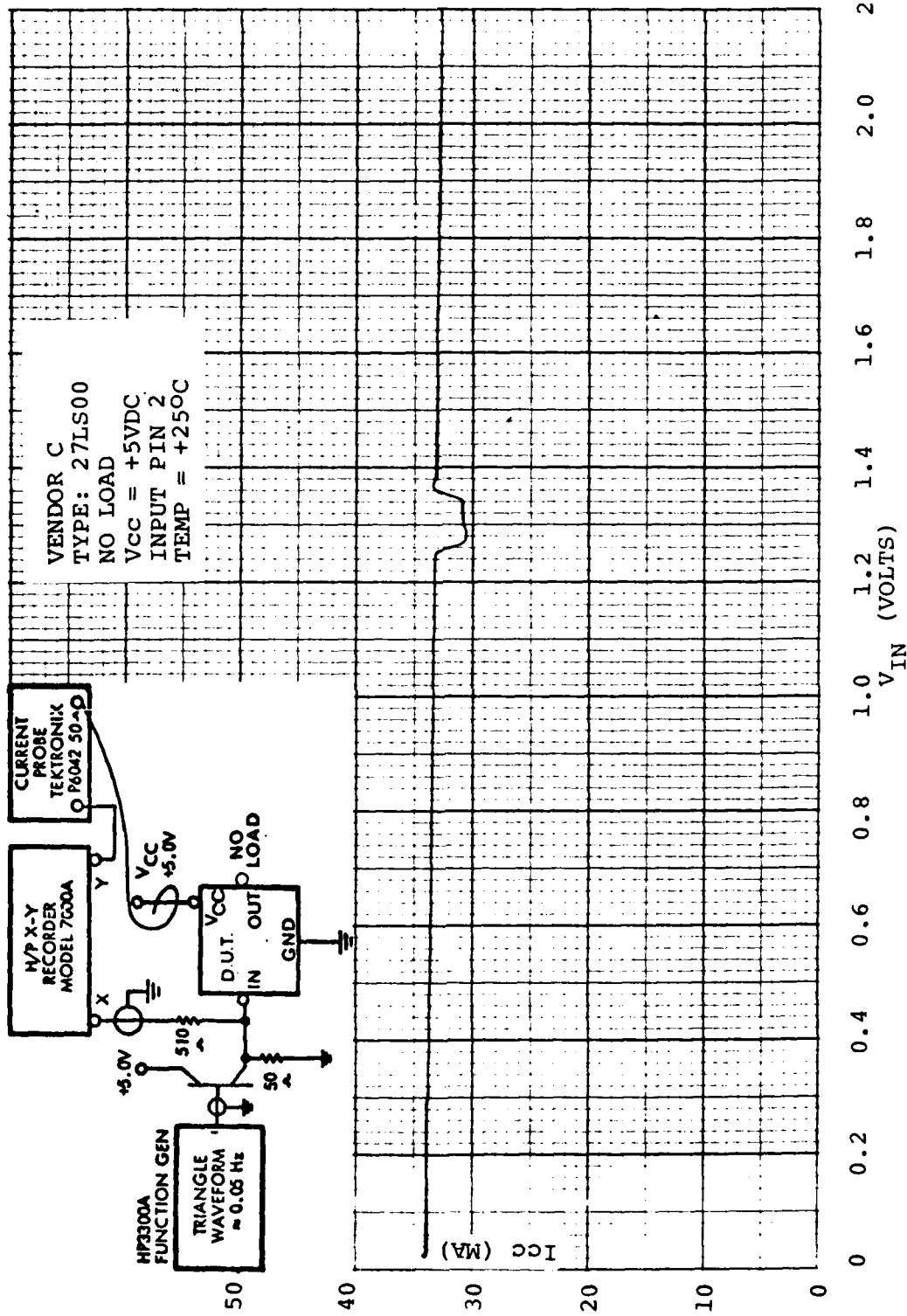
TRANSFER CHARACTERISTICS



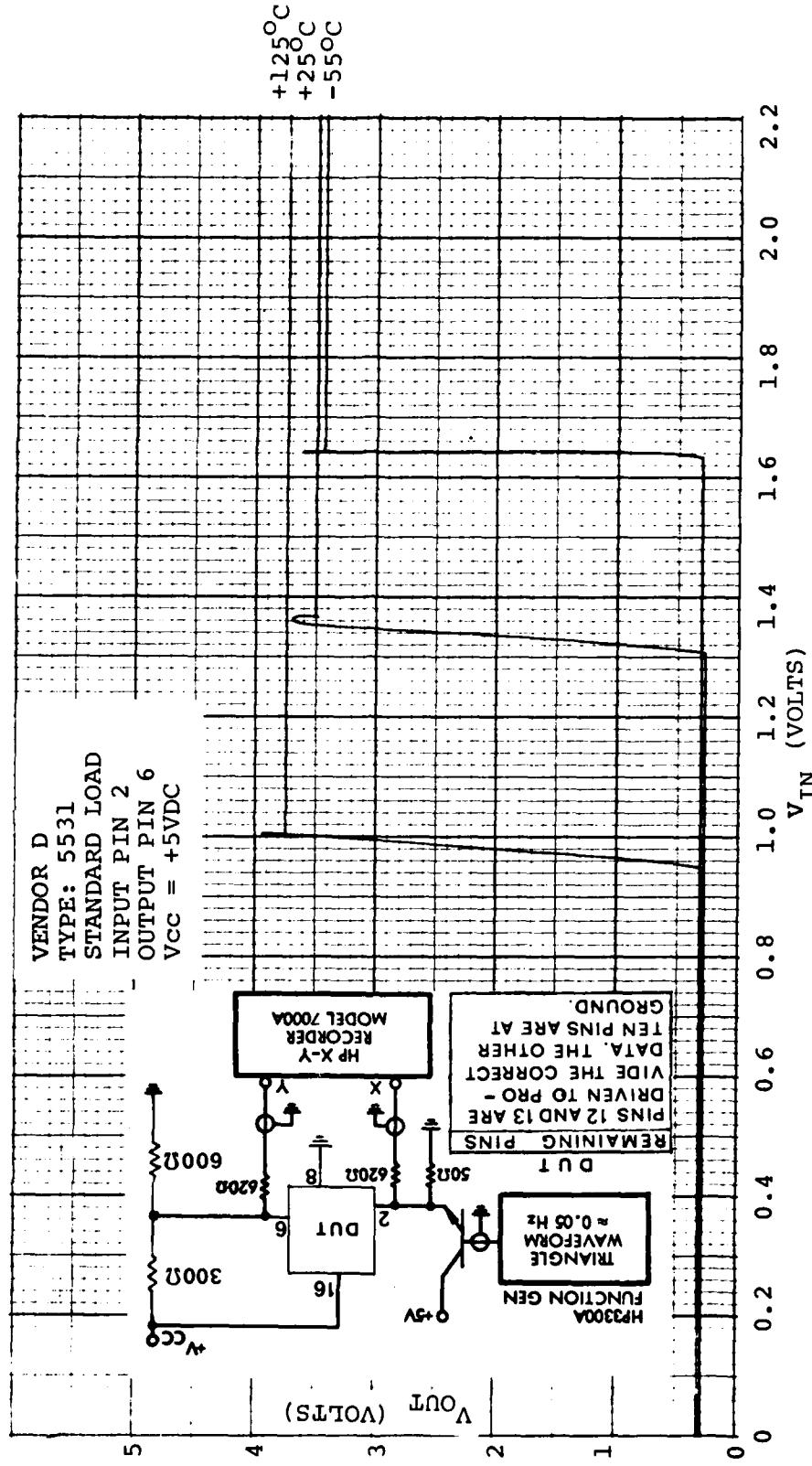
TRANSFER CHARACTERISTICS



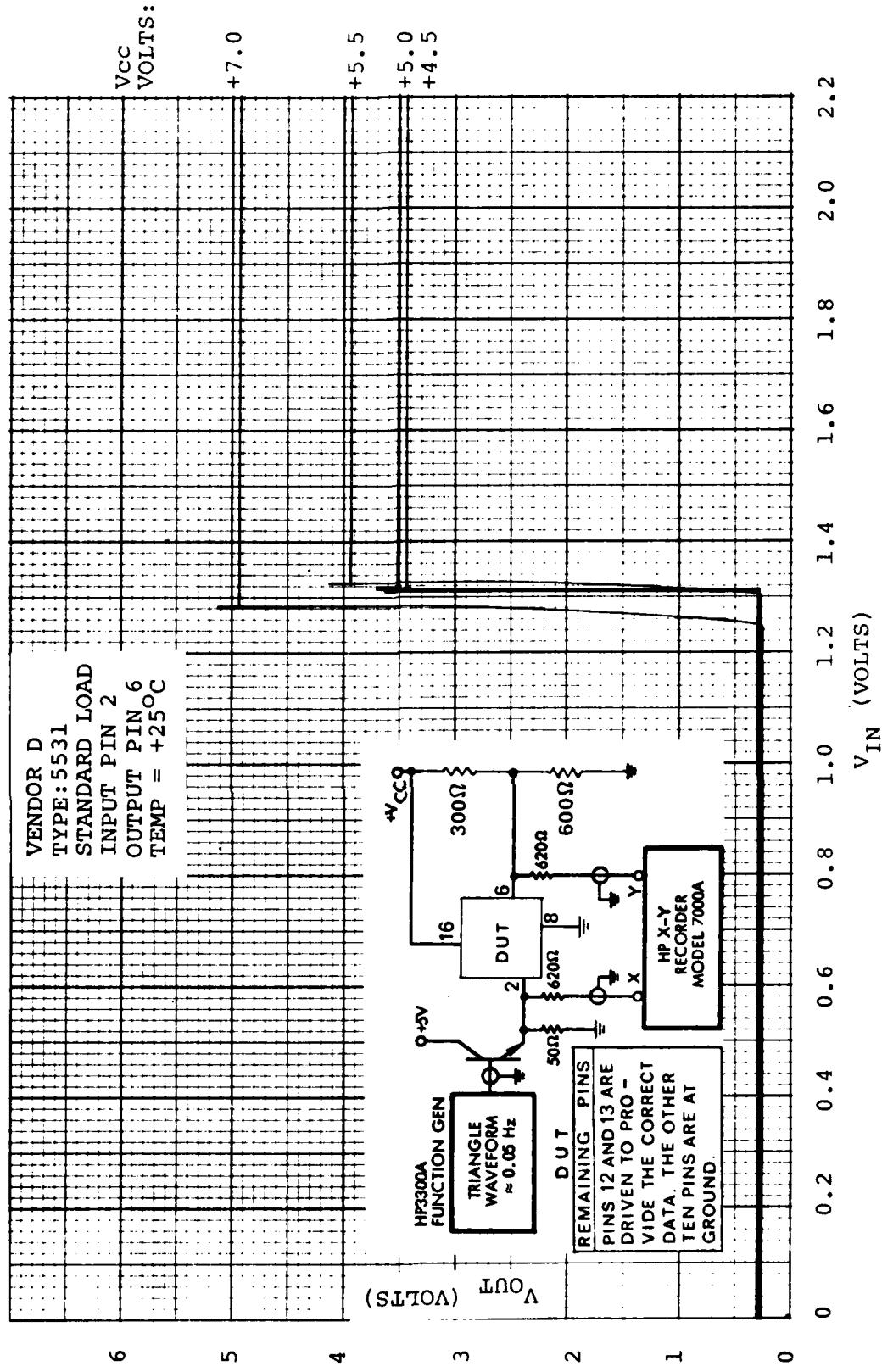
I<sub>CC</sub> VS INPUT VOLTAGE



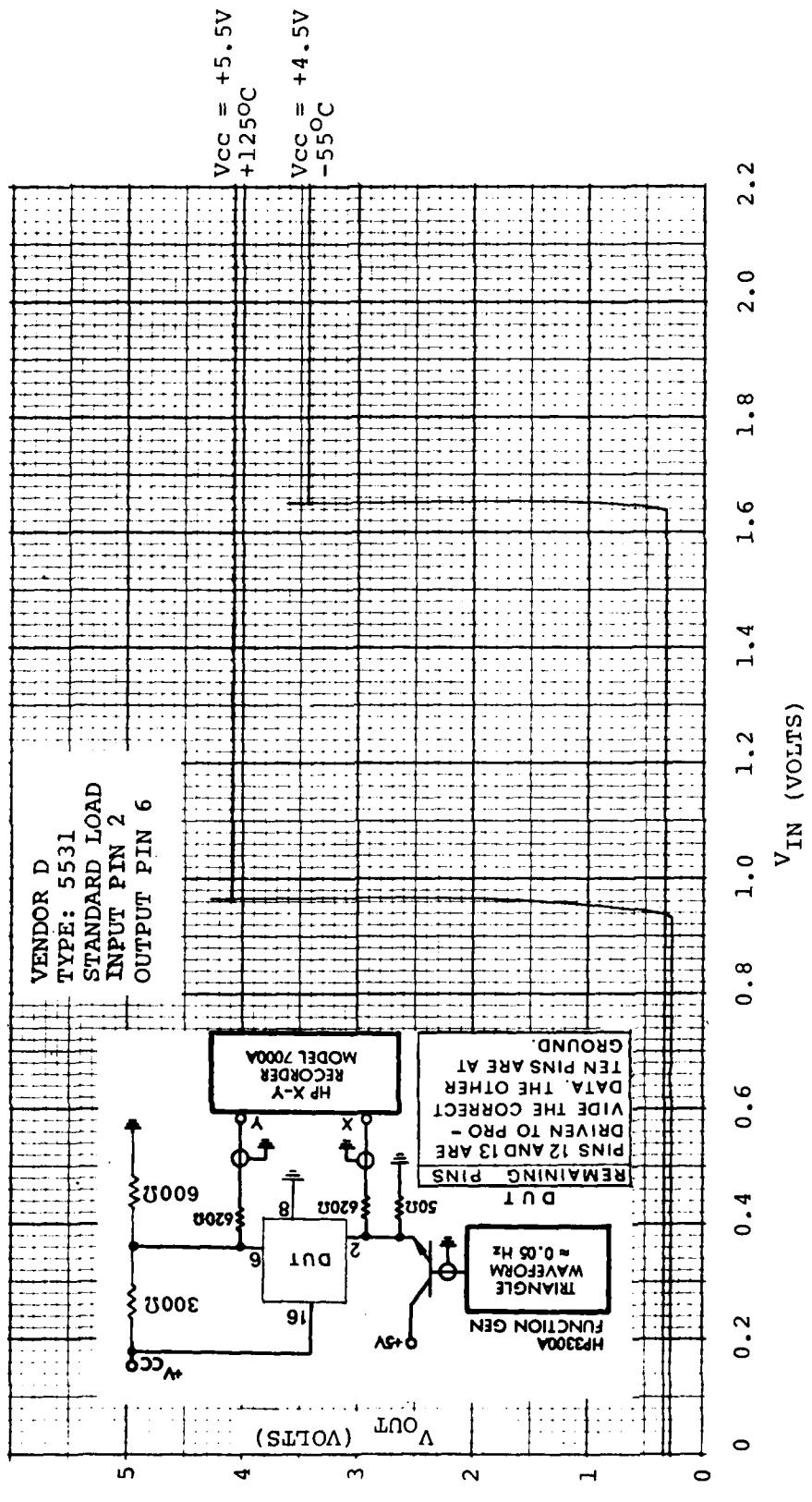
TRANSFER CHARACTERISTICS



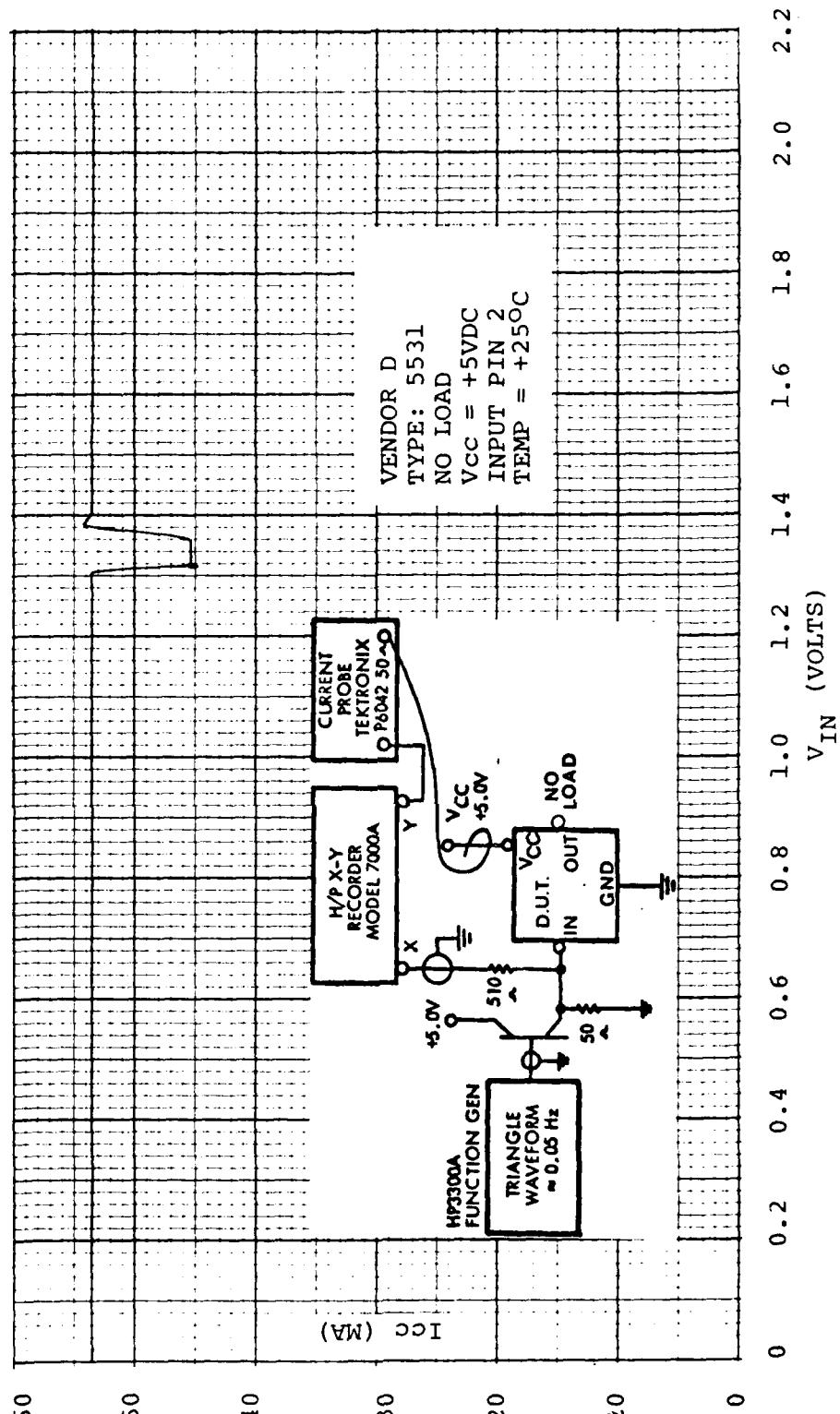
TRANSFER CHARACTERISTICS



TRANSFER CHARACTERISTICS



I<sub>CC</sub> VS INPUT VOLTAGE

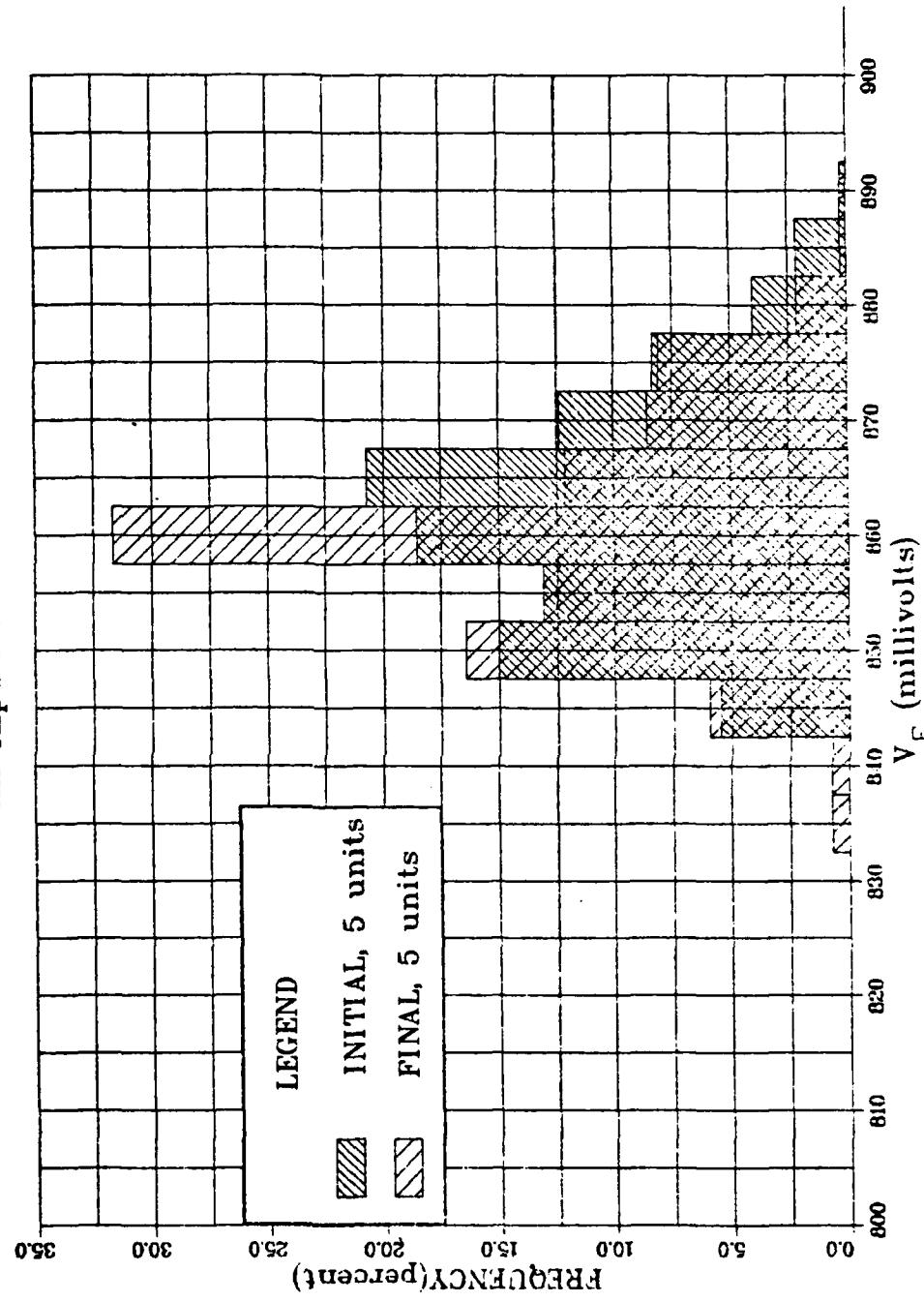


## Input Clamp Voltage Distribution

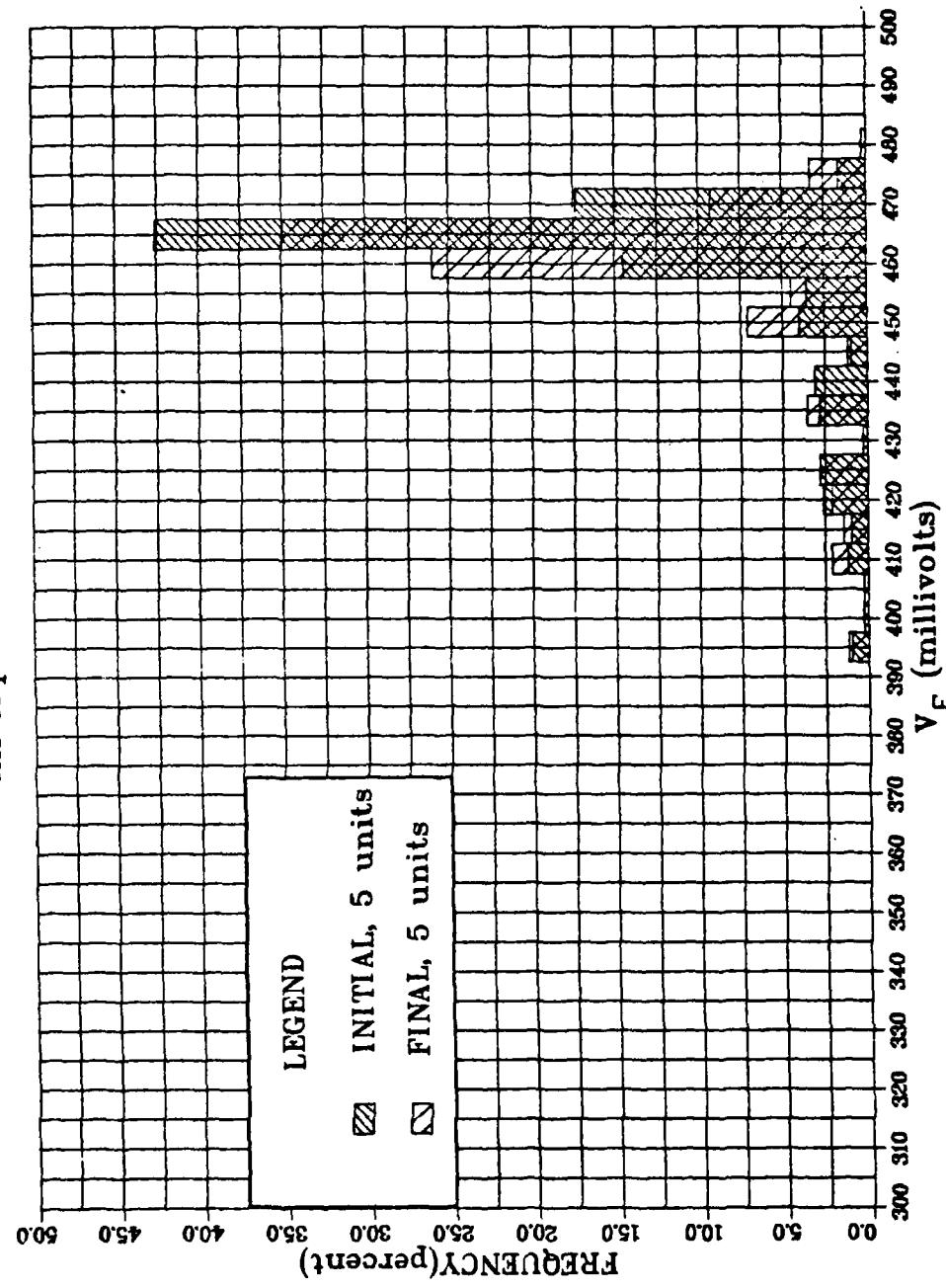
(18 millamps)

Vendor A 54LS181

All Inputs at +25°C

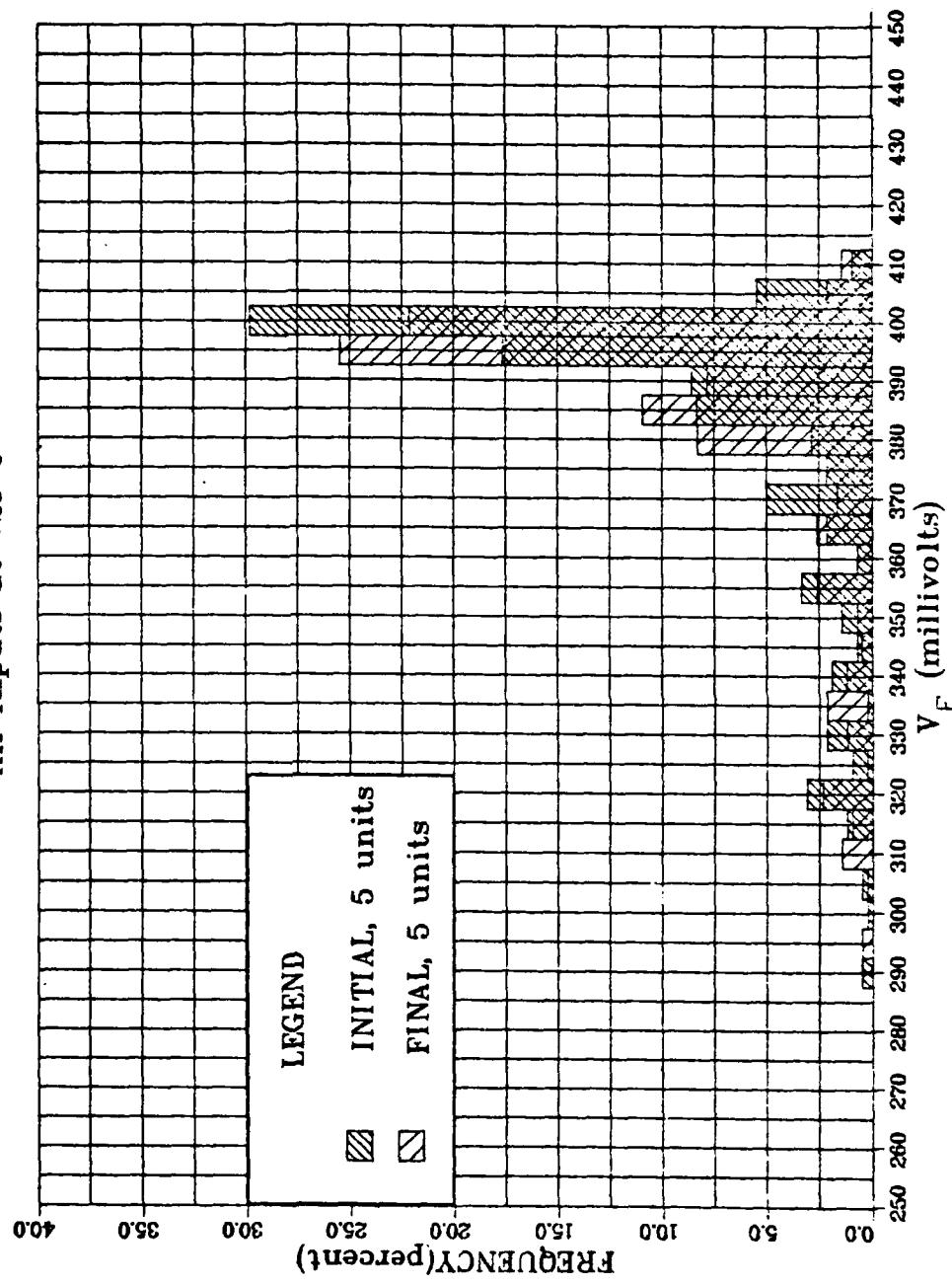


Input Clamp Voltage Distribution  
(10 microamps)  
Vendor A 54LS181  
All Inputs at +25°C



## Input Clamp Voltage Distribution

( $\mu$  microamp)  
Vendor A 54LS181  
All Inputs at +25°C

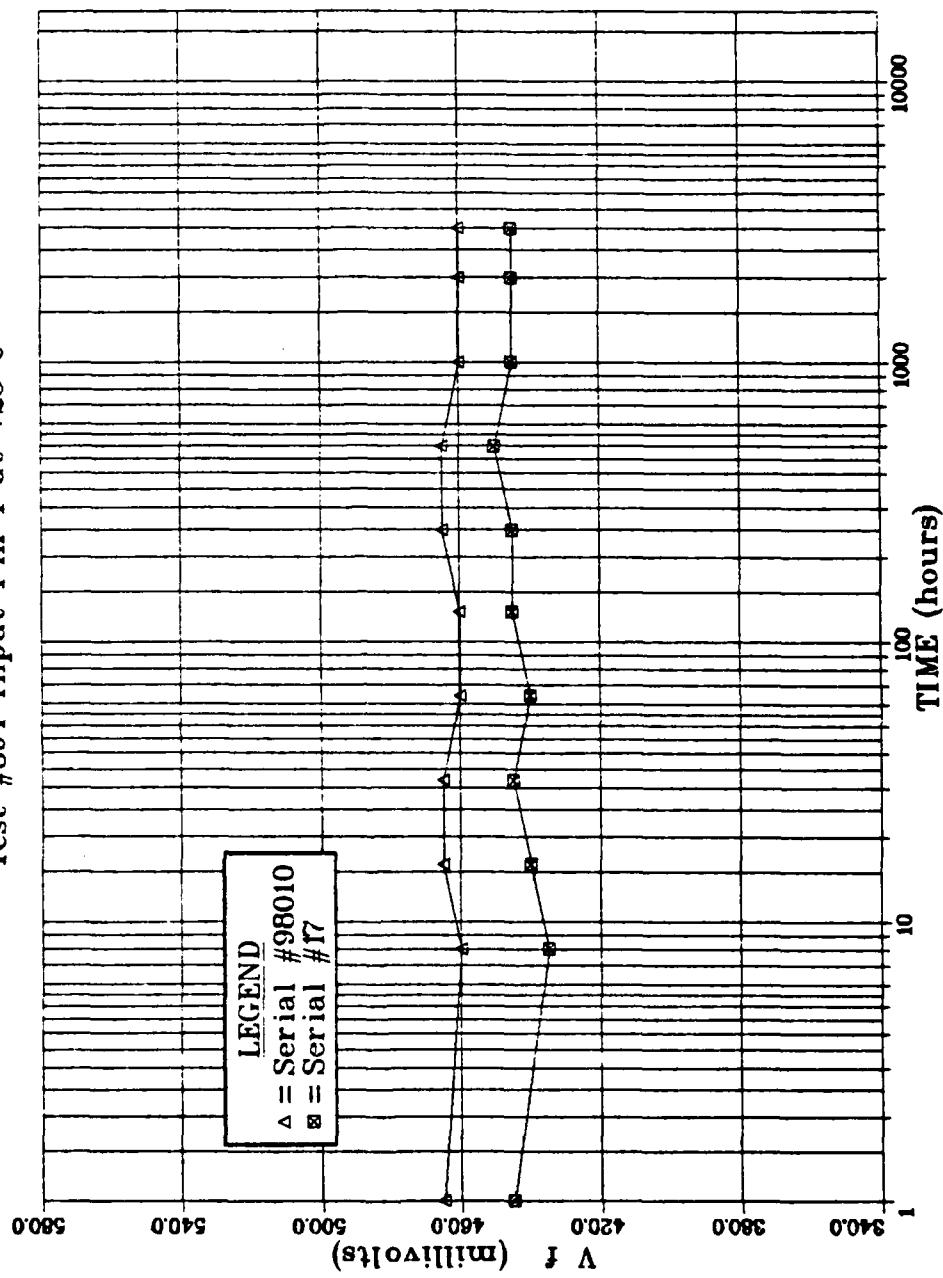


## Input Clamp Voltage Stability

Vendor A 54LS181 (10 microamps)

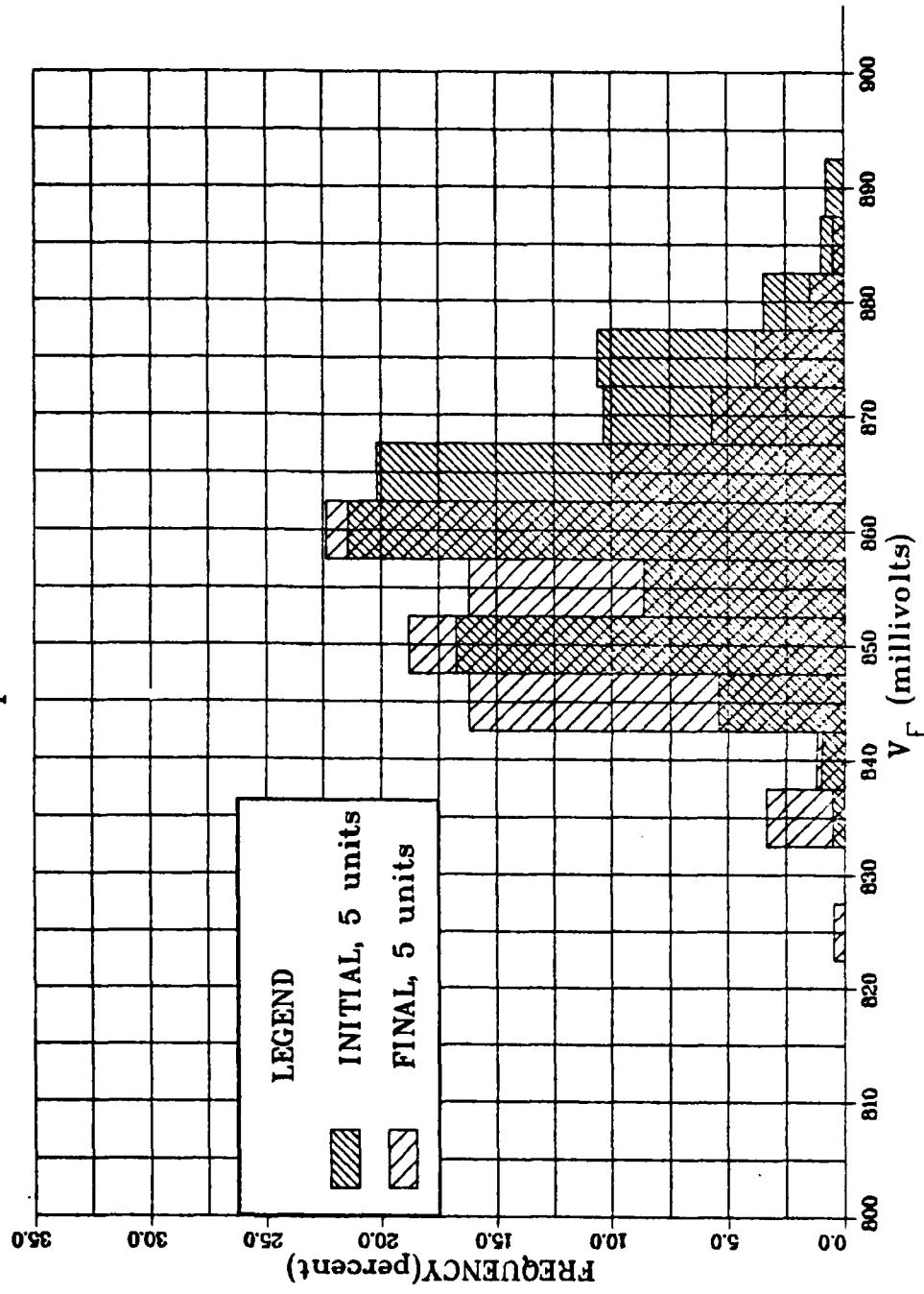
Stress Temperature +250°C

Test #304 Input Pin 1 at +25°C



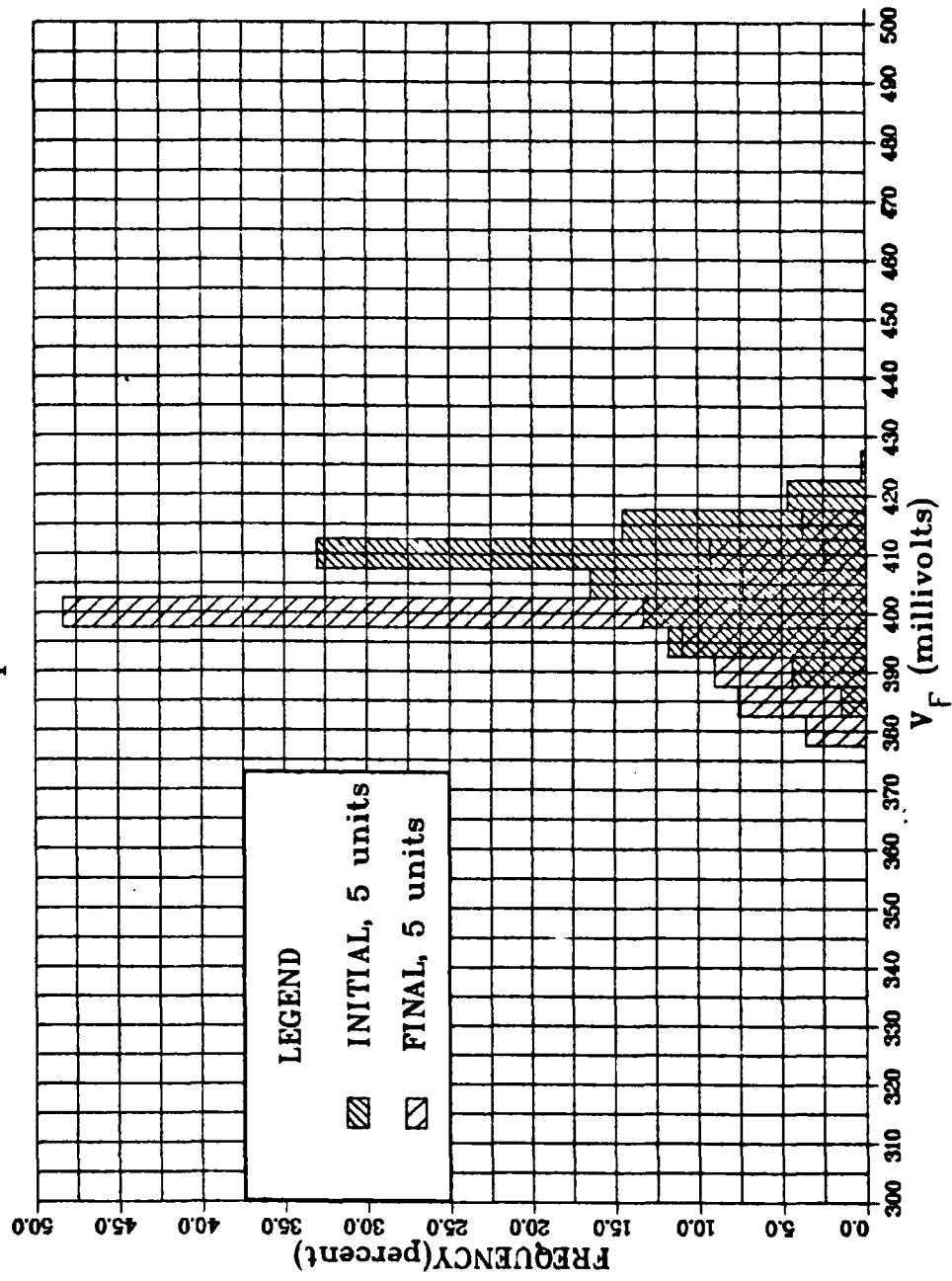
## Input Clamp Voltage Distribution

(18 milliamps)  
Vendor B 54LS181  
All Inputs at +25°C



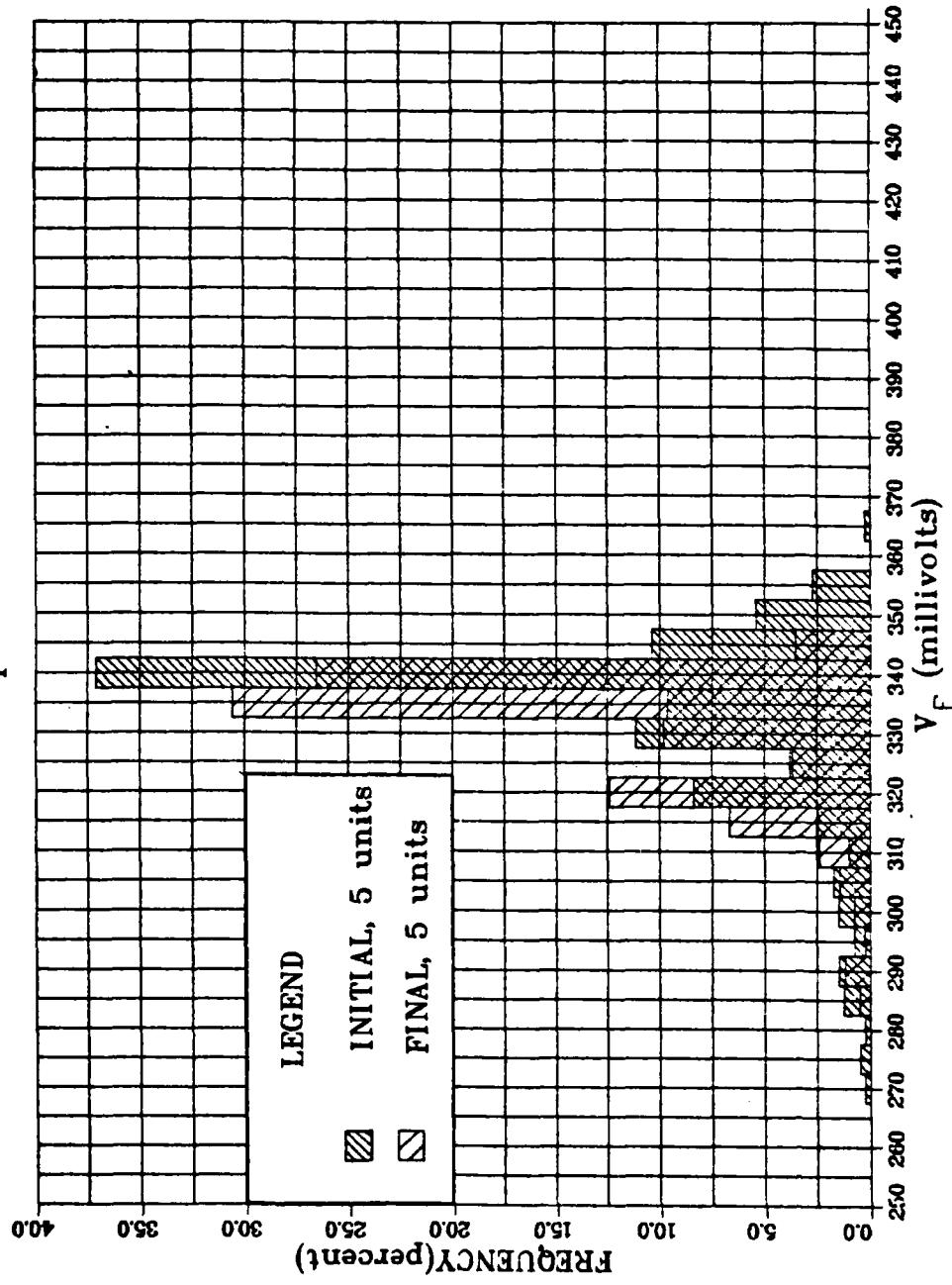
## Input Clamp Voltage Distribution

(10 microamps)  
Vendor B 541S181  
All Inputs at +25°C



## Input Clamp Voltage Distribution

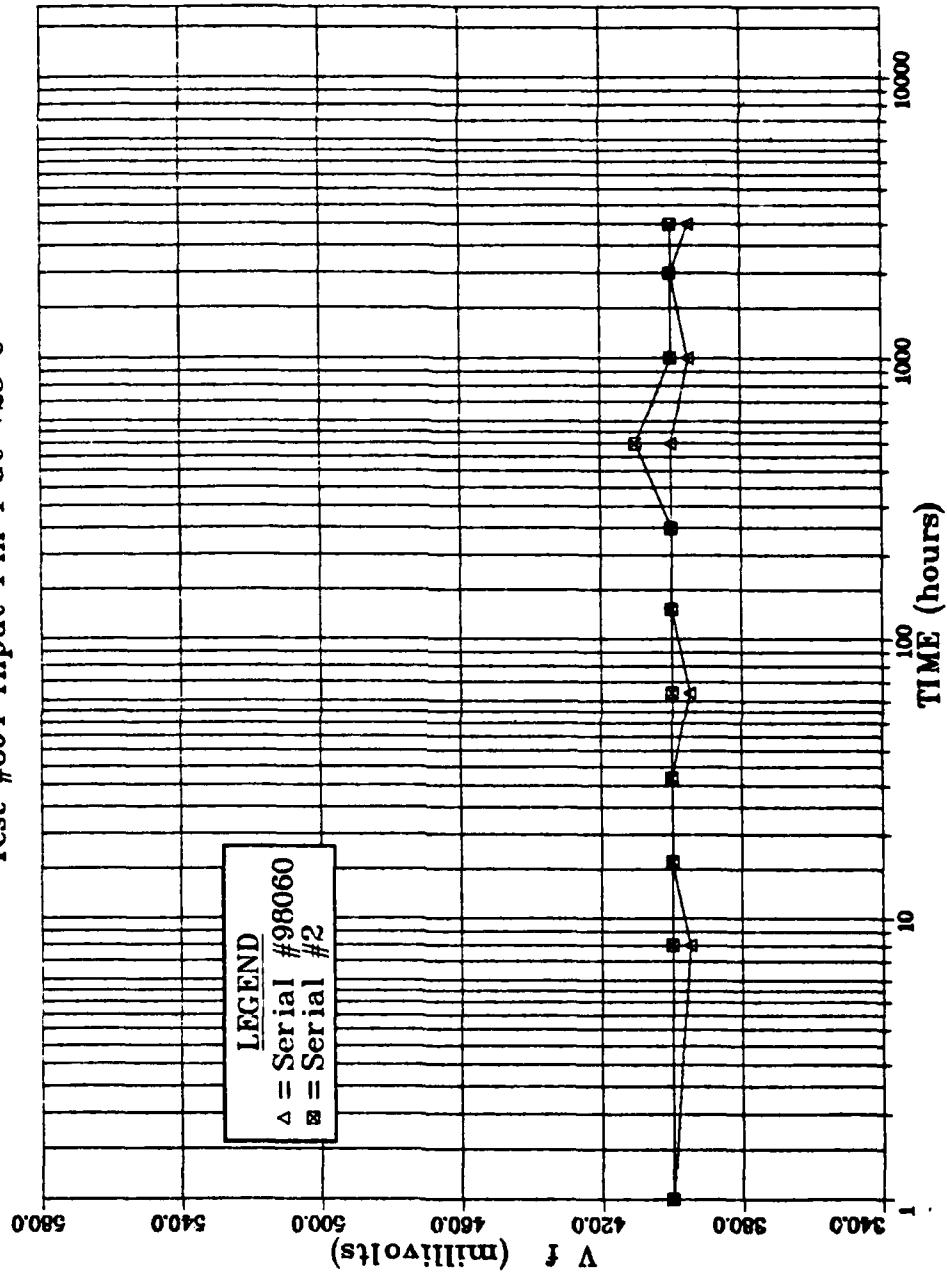
(1 microamp)  
Vendor B 54LS181  
All Inputs at +25°C



PLOT 1 07-59.15 MON 8 OCT. 1979 JOB-BR00145 : RAYTHEON DISSECTOR 7.5

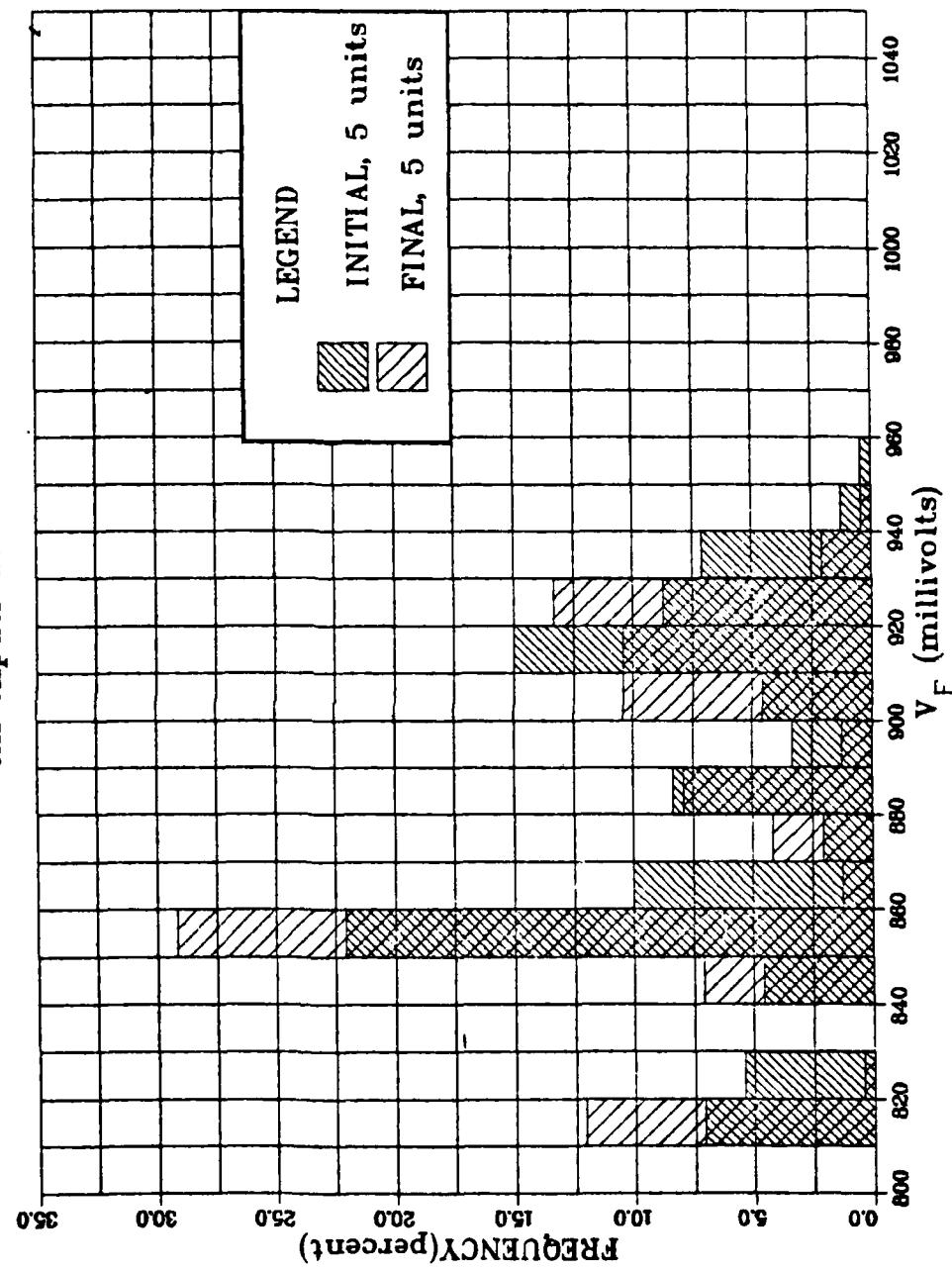
## Input Clamp Voltage Stability

Vendor B 54LS181 (10 microamps)  
Stress Temperature +250°C  
Test #304 Input Pin 1 at +25°C



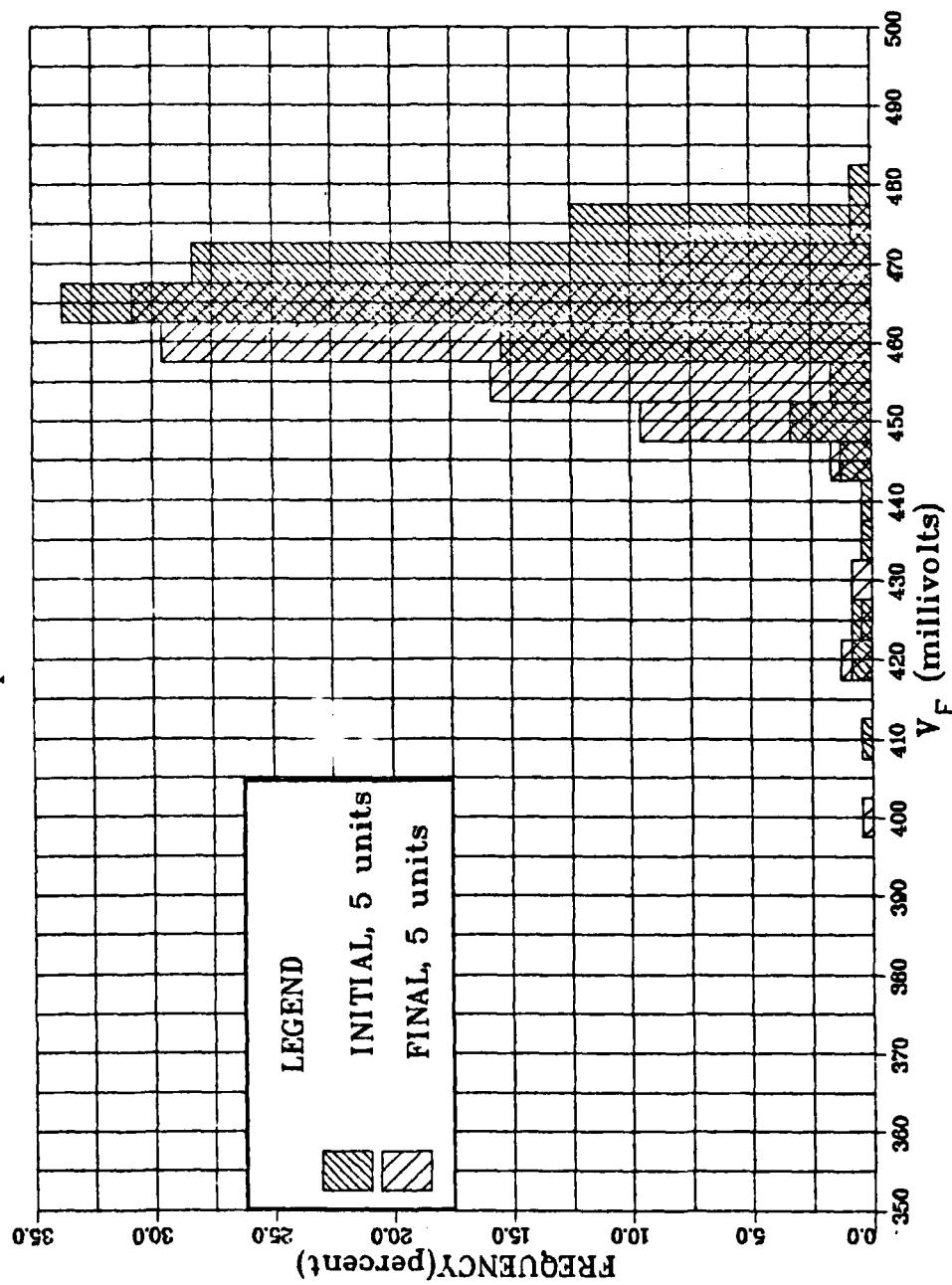
## Input Clamp Voltage Distribution

(18 millamps)  
Vendor A 54LS191  
All Inputs at +25°C



## Input Clamp Voltage Distribution

(10 microamps)  
Vendor A 54LS191  
All Inputs at +25°C

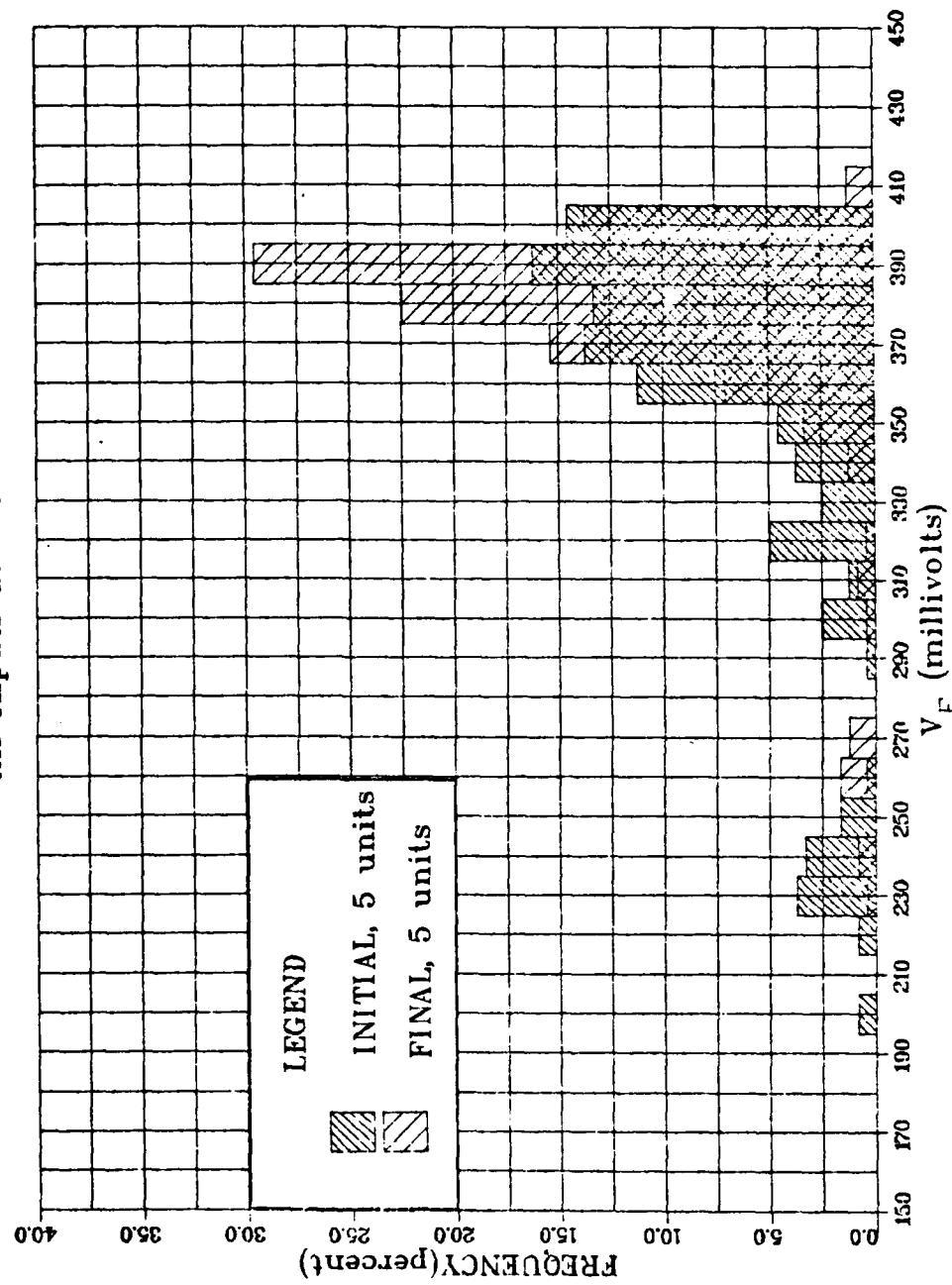


N=10

## Input Clamp Voltage Distribution

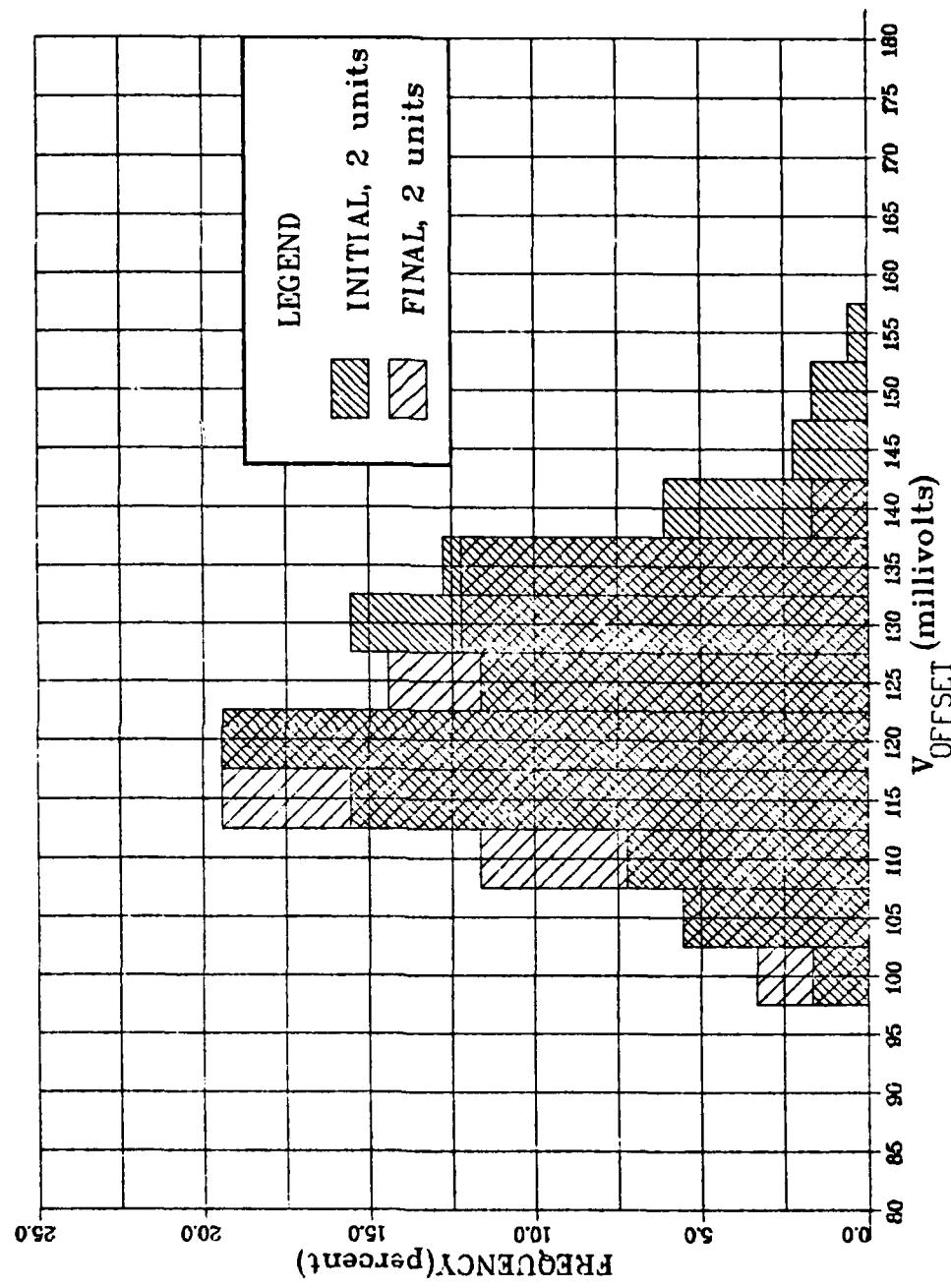
(1 microamp)

Vendor A 541S191  
All Inputs at +25°C



## Offset Voltage Distribution

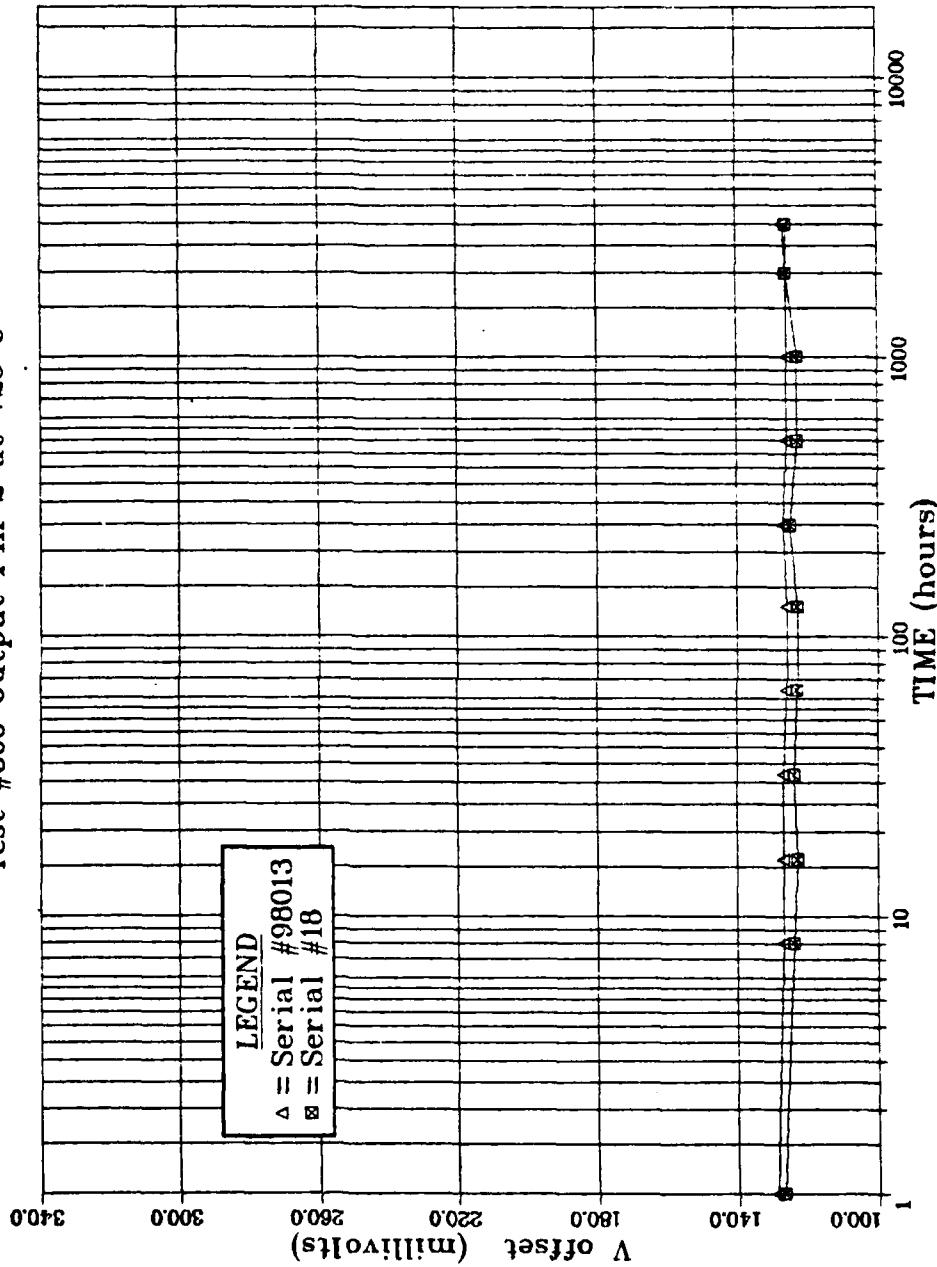
Vendor A 54LS191  
All Outputs at +25°C



## Offset Voltage Stability

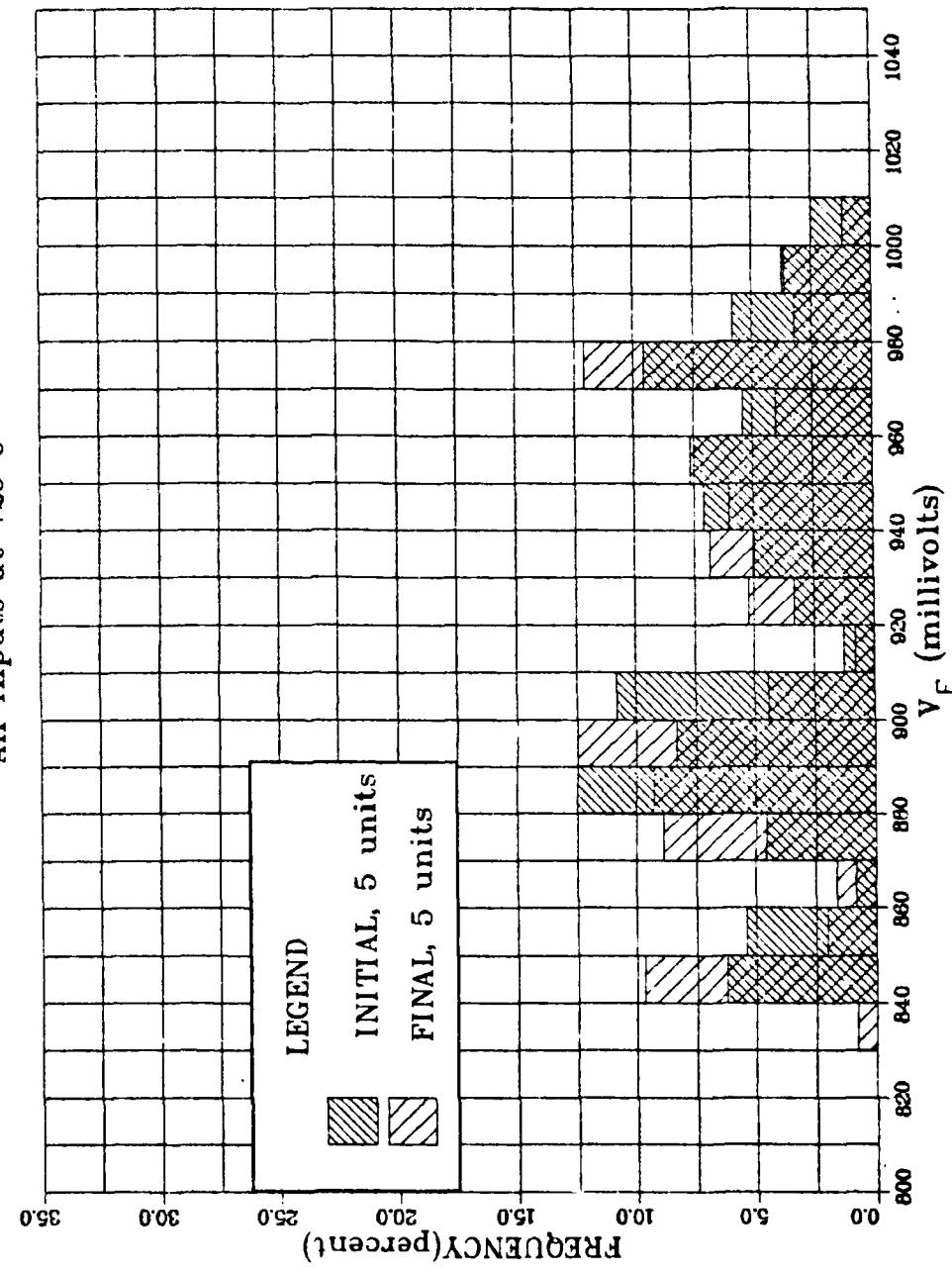
Vendor A 54LS191

Stress Temperature +250°C  
Test #500 Output Pin 2 at +25°C



## Input Clamp Voltage Distribution

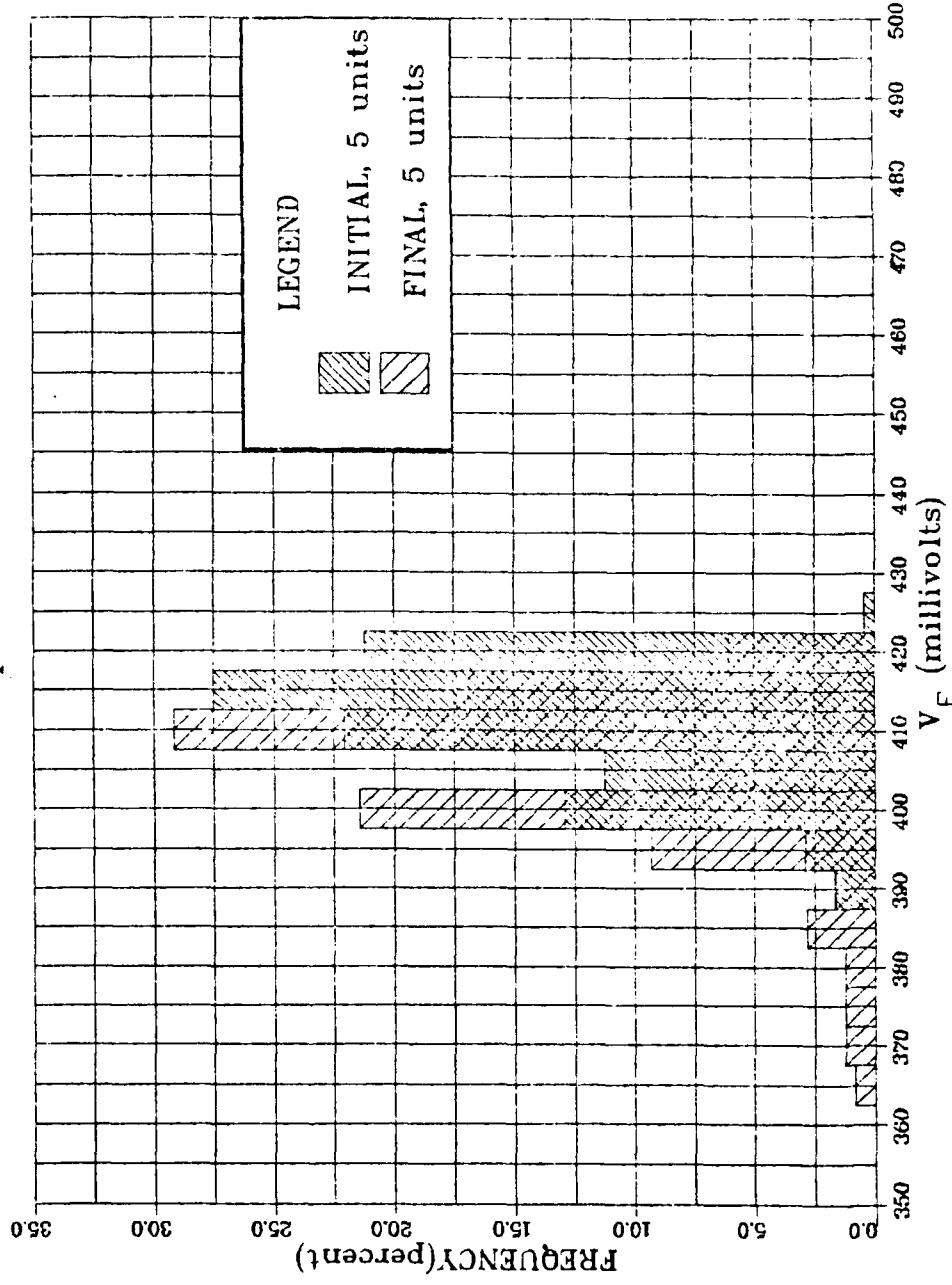
(18 millamps)  
Vendor B 54LS191  
All Inputs at +25°C



## Input Clamp Voltage Distribution

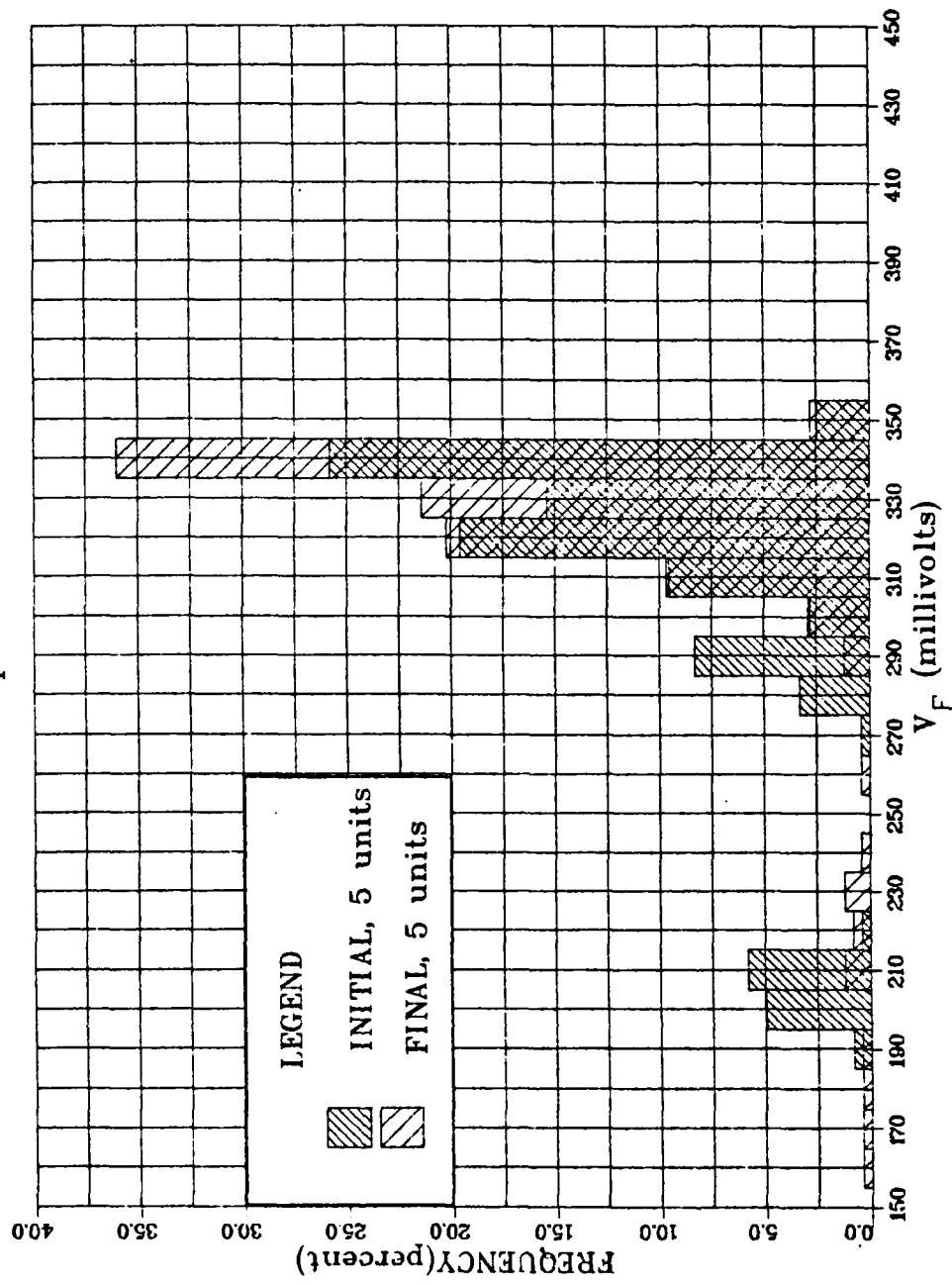
(10 microamps)

Vendor B 54LS191  
All Inputs at +25°C



## Input Clamp Voltage Distribution

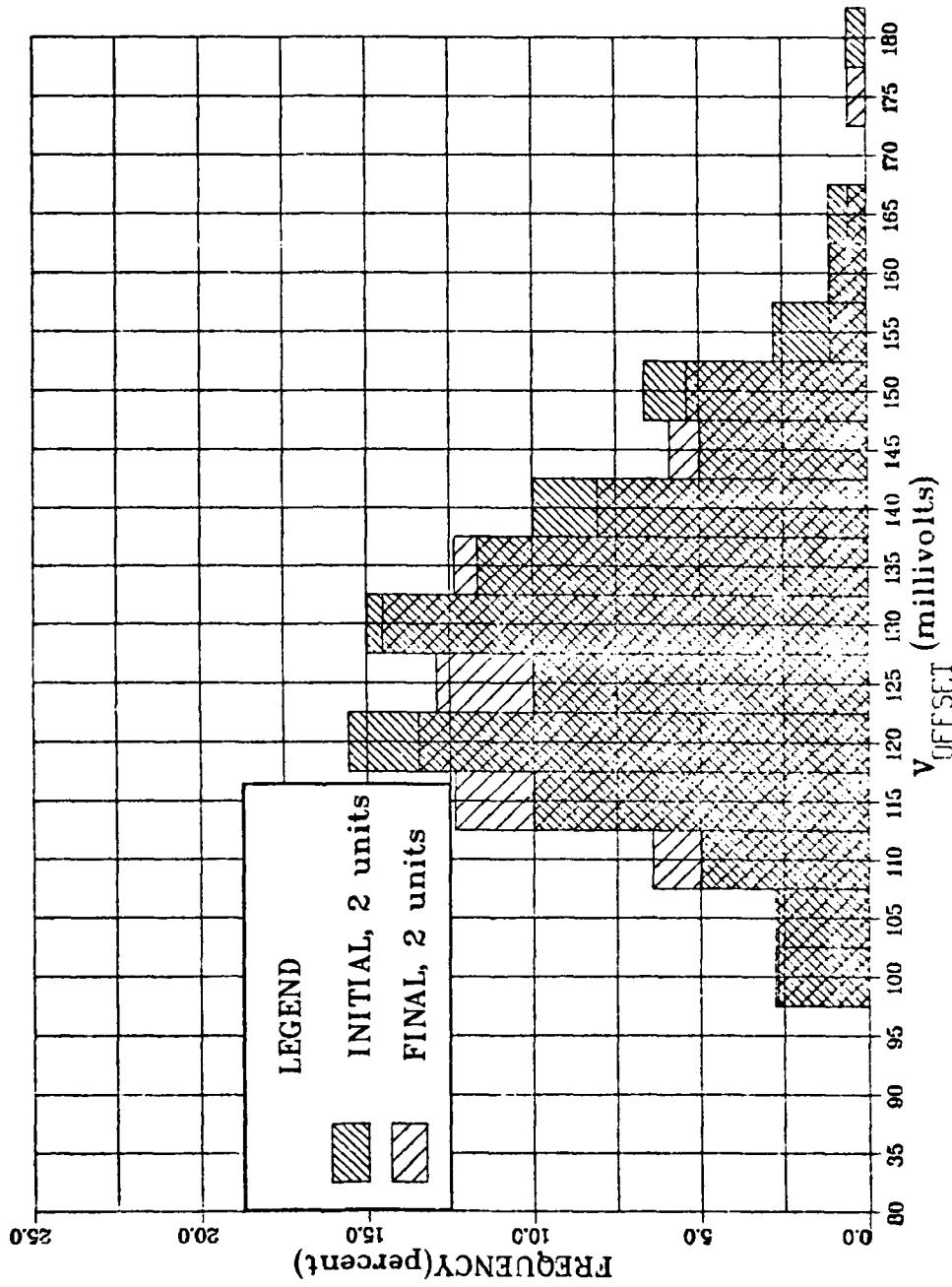
(1 microamp)  
Vendor B 54LS191  
All Inputs at +25°C



## Offset Voltage Distribution

Vendor B 54LS191

All Outputs at +25°C

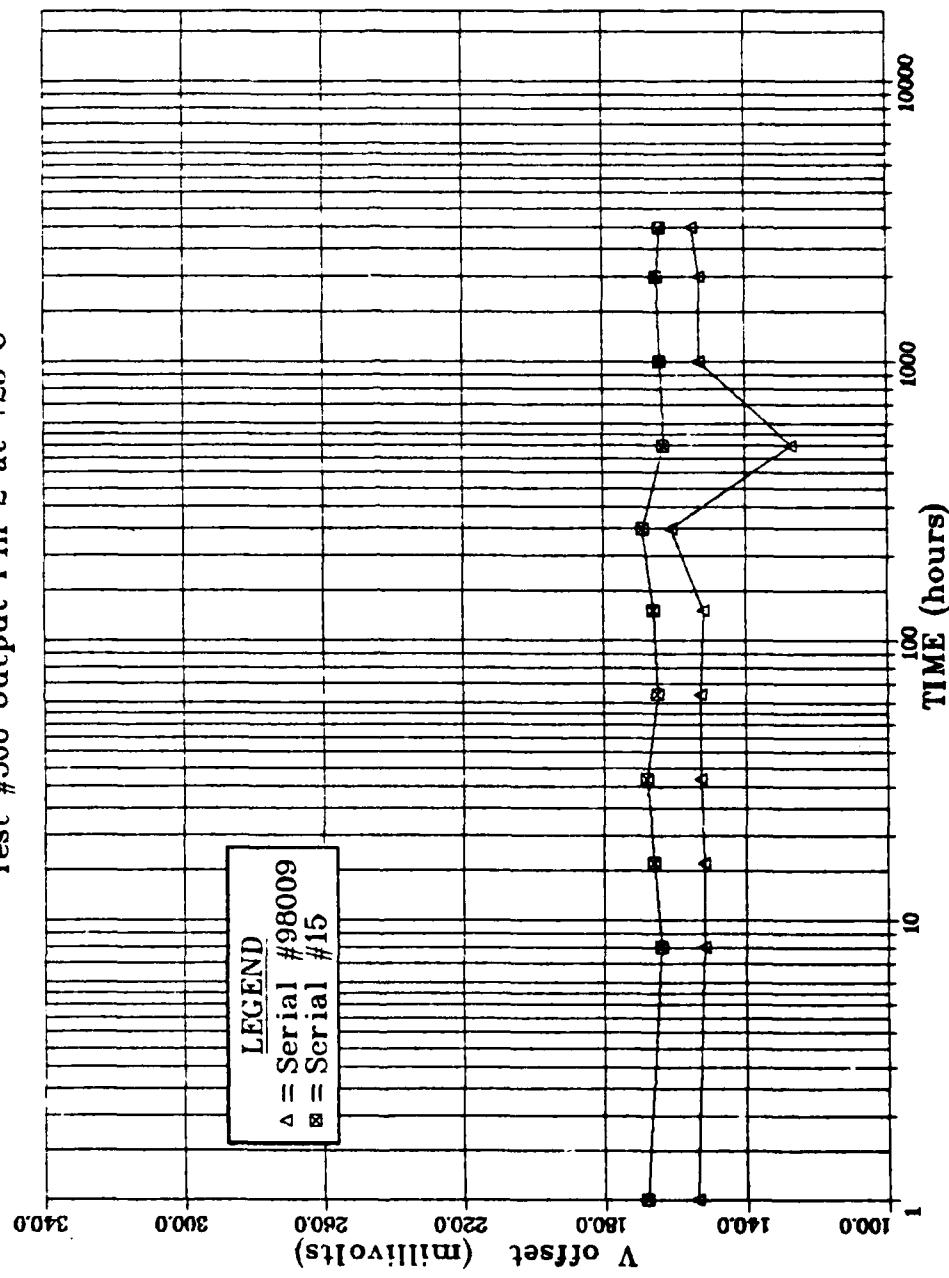


PLOT 1 10.27.76 MON 8 OCT. 1979 J08-B40015 RAYTHEON 0155PCL VEP 7.5

## Offset Voltage Stability

Vendor B 54LS191

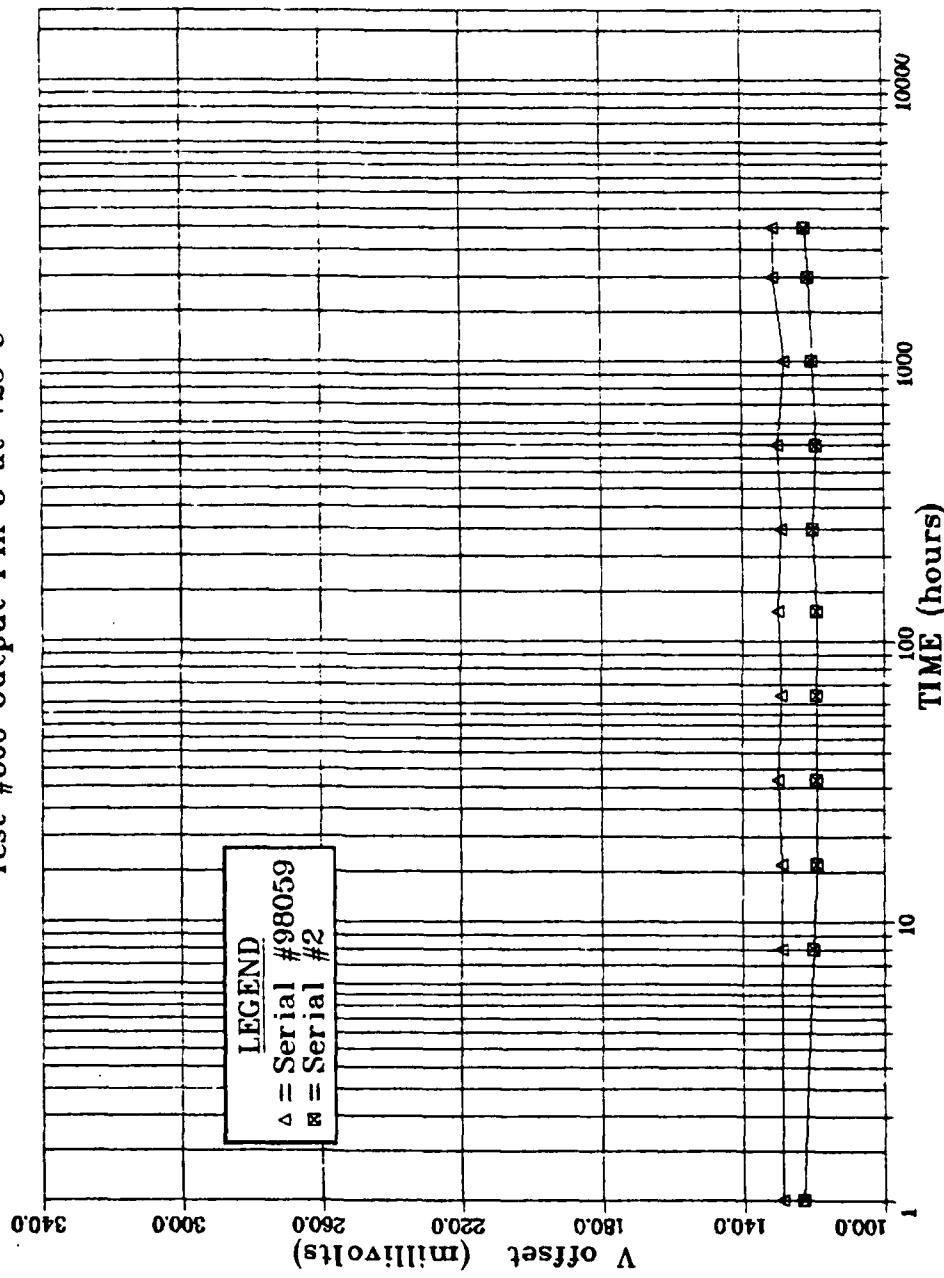
Stress Temperature +250°C  
Test #500 Output Pin 2 at +25°C



## Offset Voltage Stability

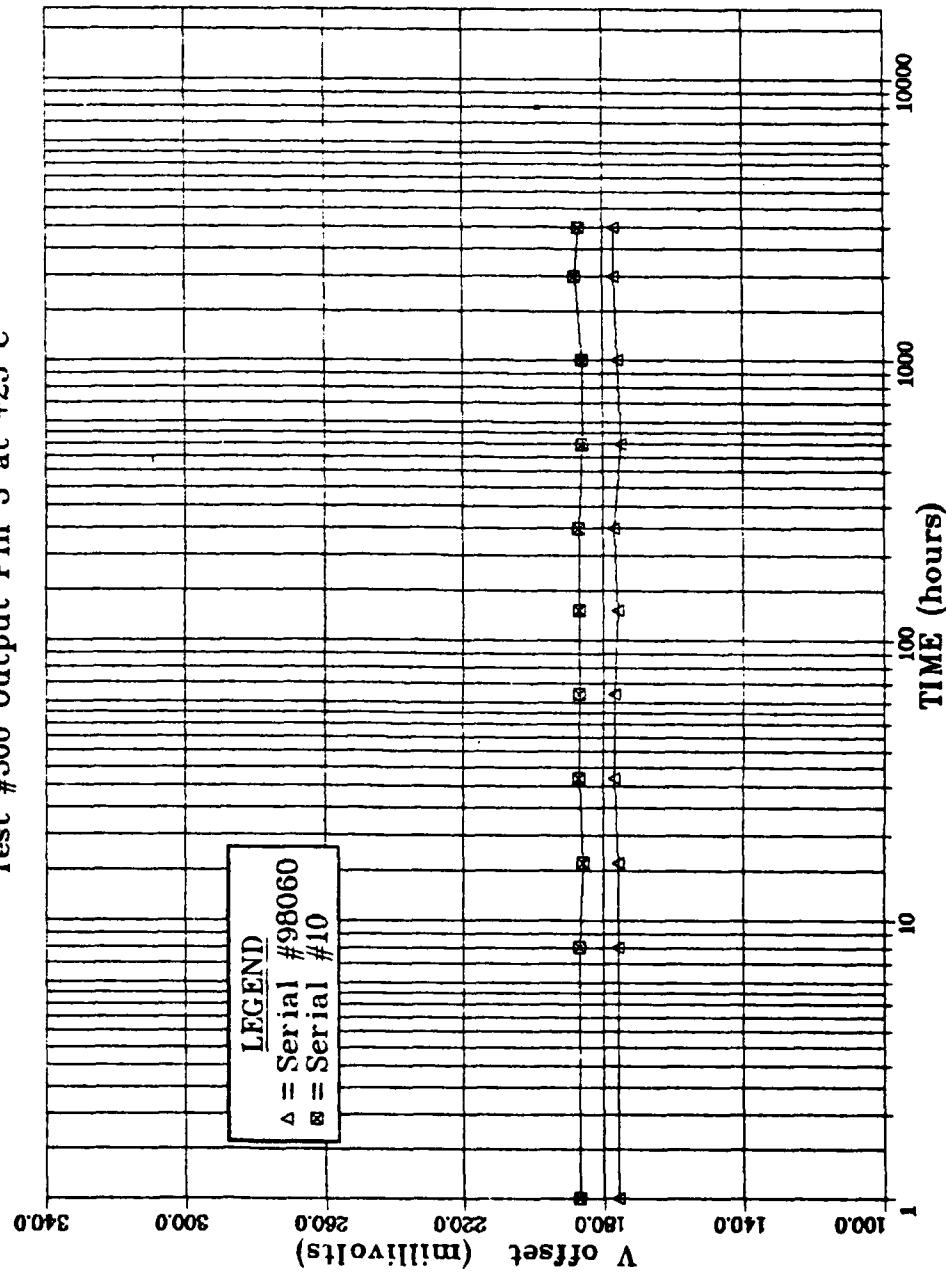
Vendor A 54LS251

Stress Temperature +250°C  
Test #500 Output Pin 5 at +25°C



## Offset Voltage Stability

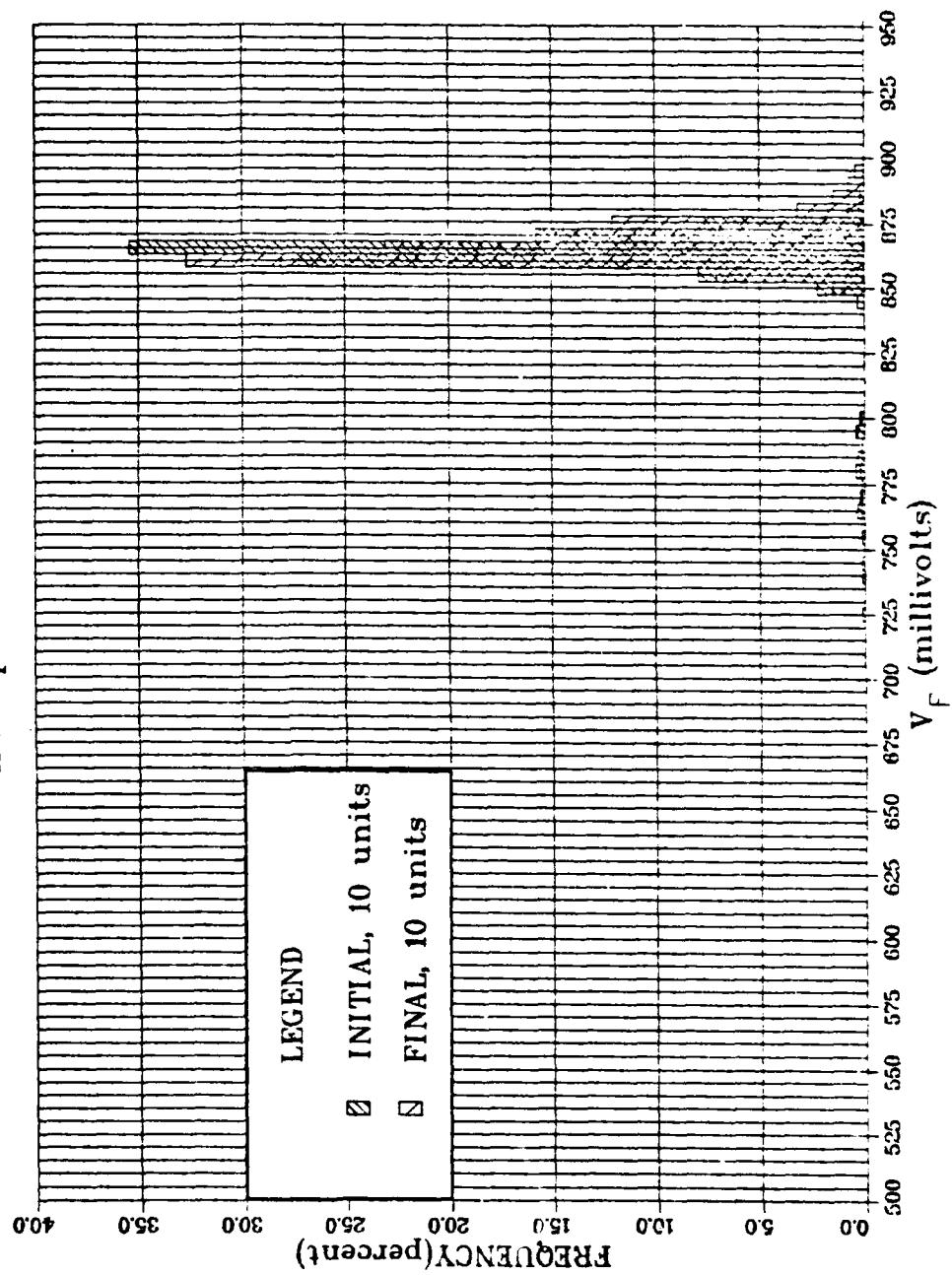
Vendor B 54LS251  
Stress Temperature +250°C  
Test #500 Output Pin 5 at +25°C



## Input Clamp Voltage Distribution

(18 millamps)

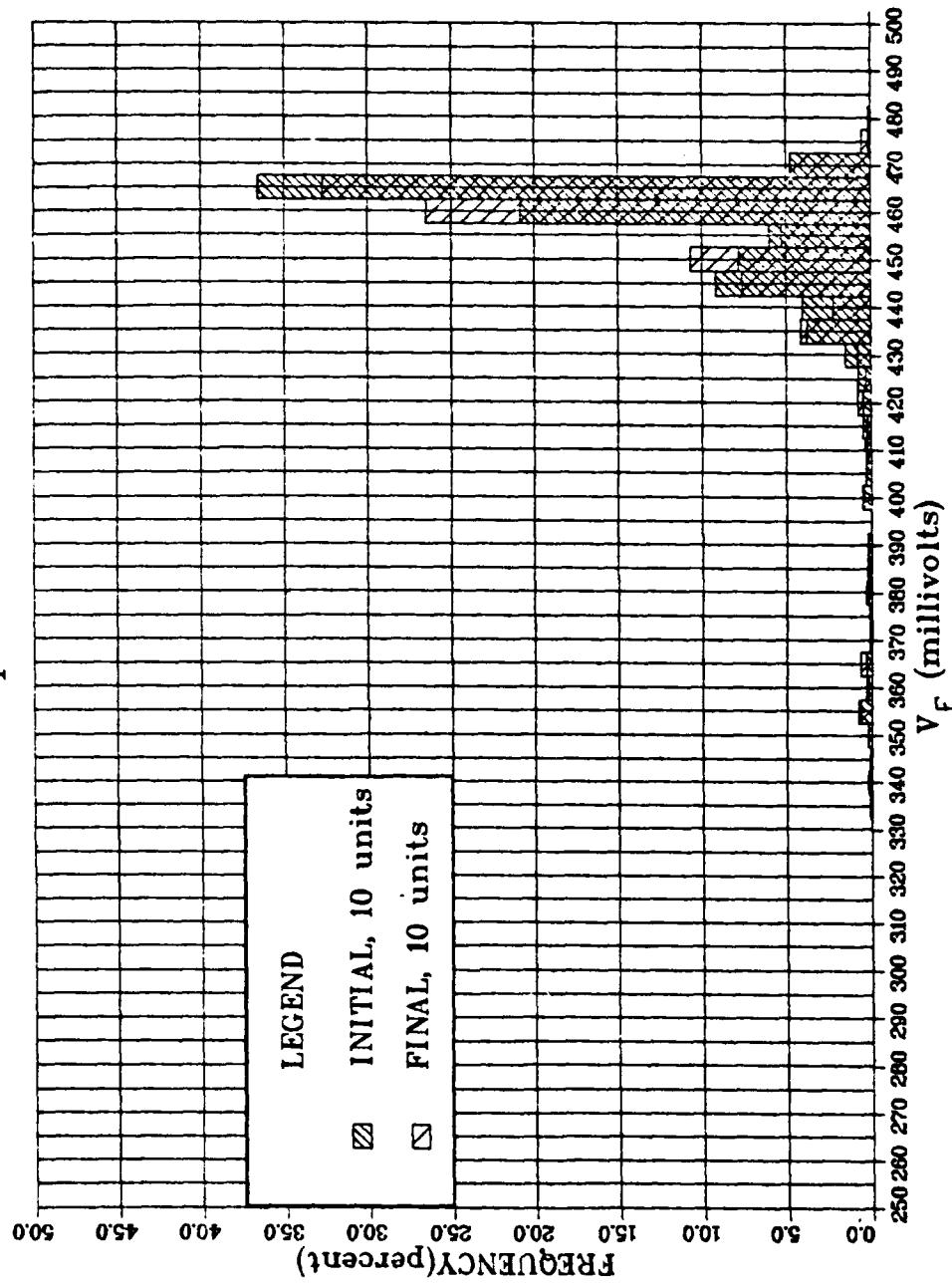
Vendor A 54LS283  
All Inputs at +25°C



## Input Clamp Voltage Distribution

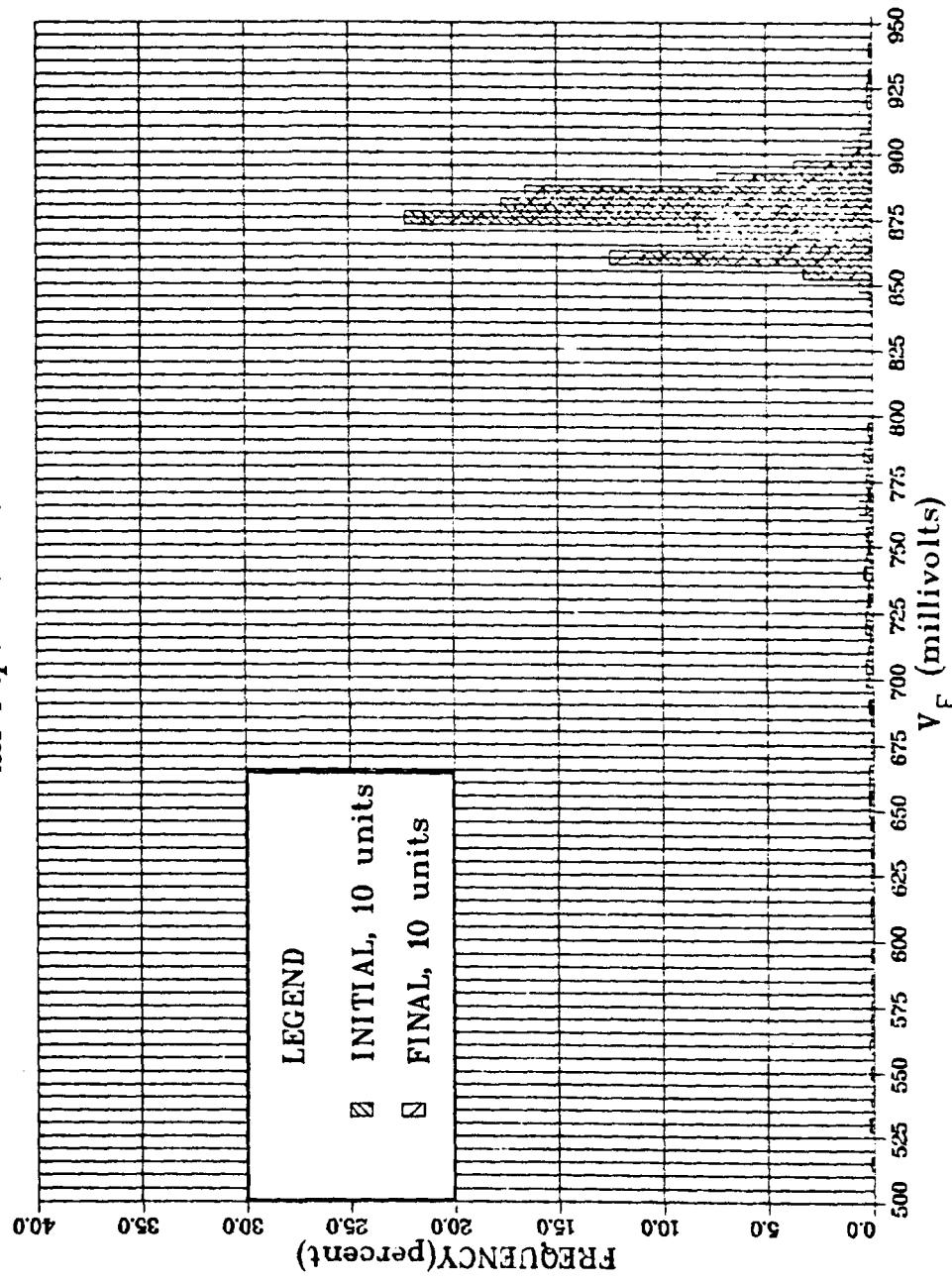
(10 microamps)

Vendor A 54LS283  
All Inputs at +25°C



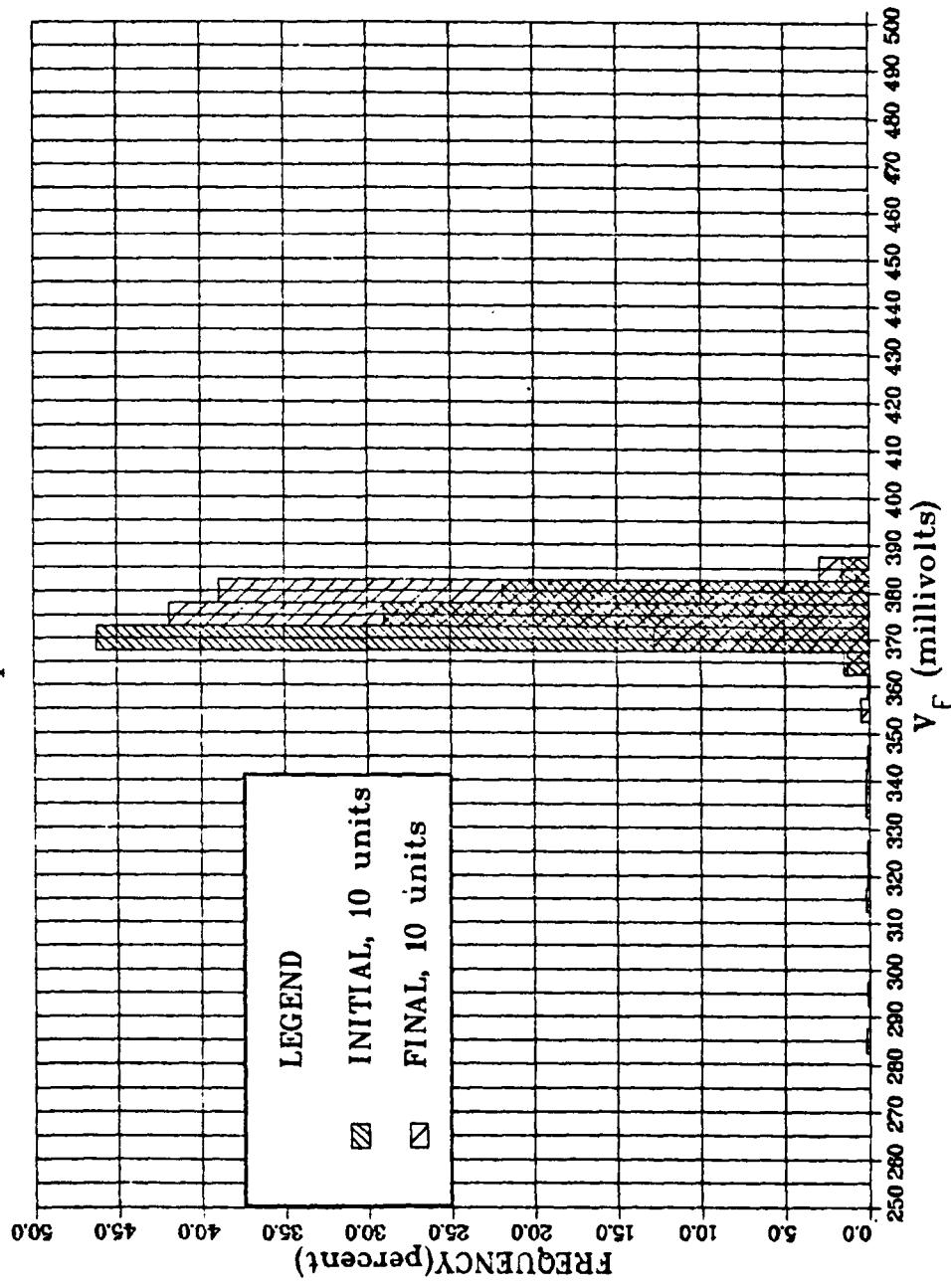
## Input Clamp Voltage Distribution

(18 millamps)  
Vendor B 54LS283  
All Inputs at +25°C



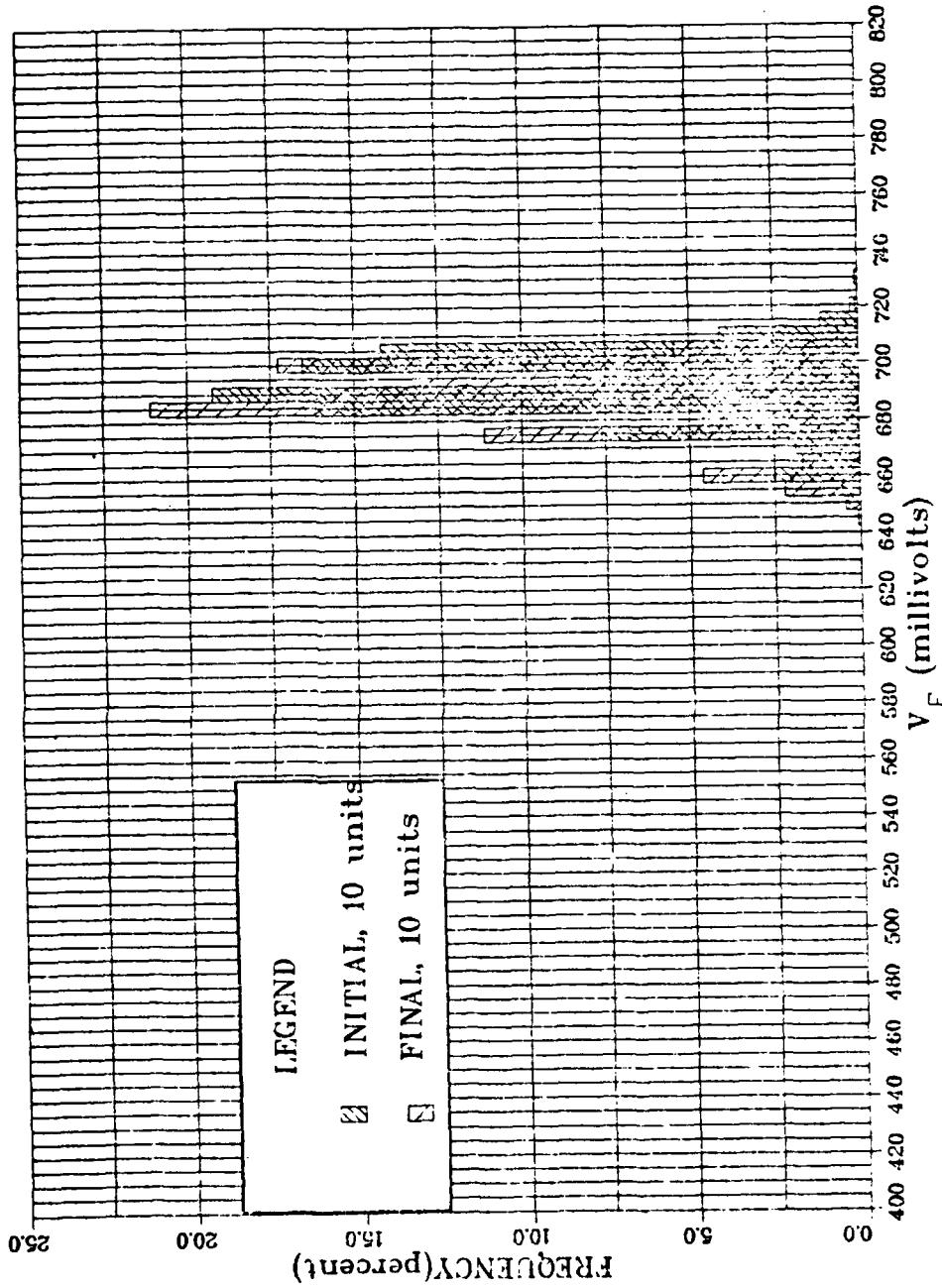
## Input Clamp Voltage Distribution

(10 microamps)  
Vendor B 54LS283  
All Inputs at +25°C



## Input Clamp Voltage Distribution

(18 millamps)  
Vendor C RAM  
All Inputs at +25°C

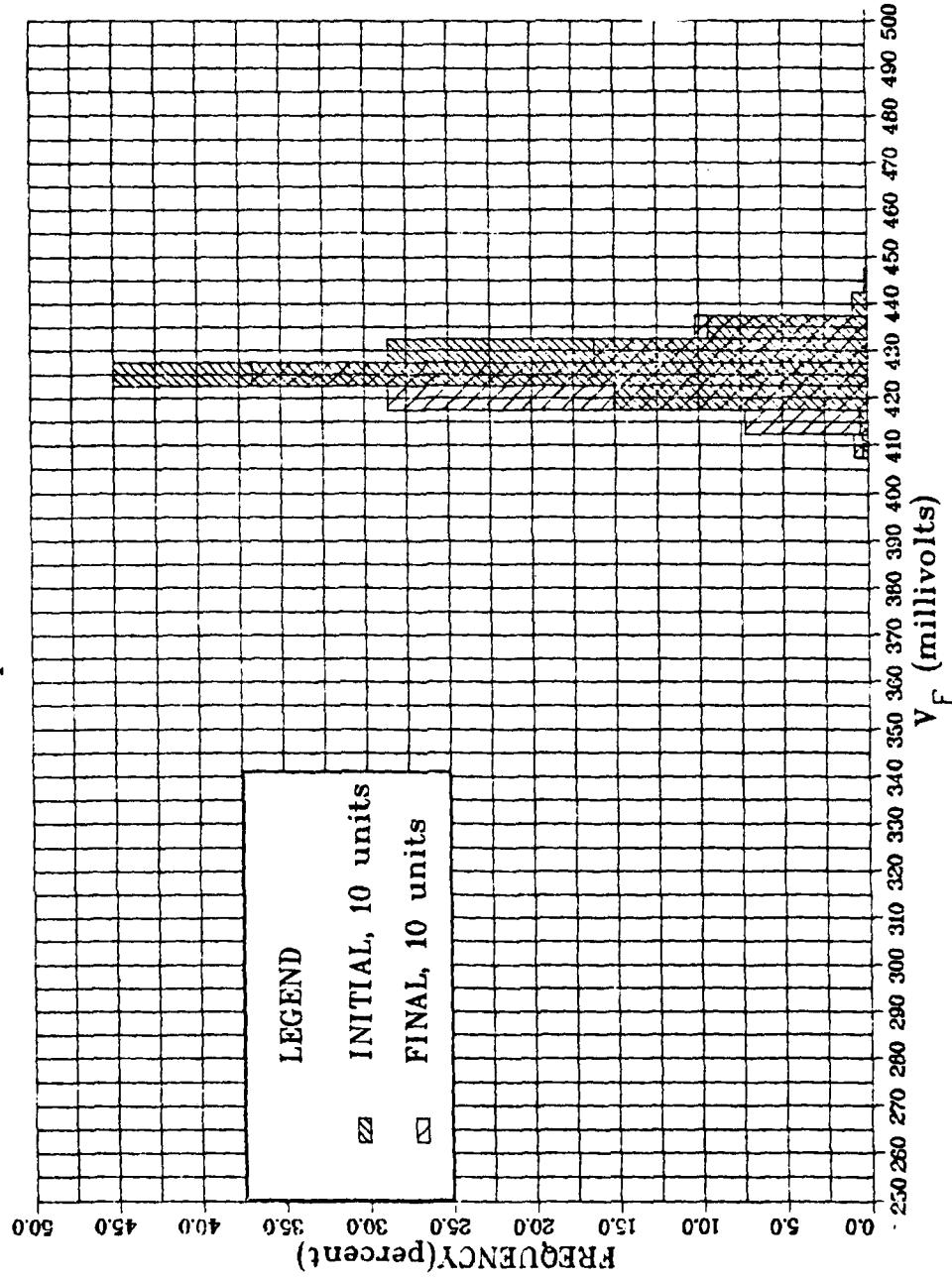


## Input Clamp Voltage Distribution

(10 microamps)

Vendor C RAM

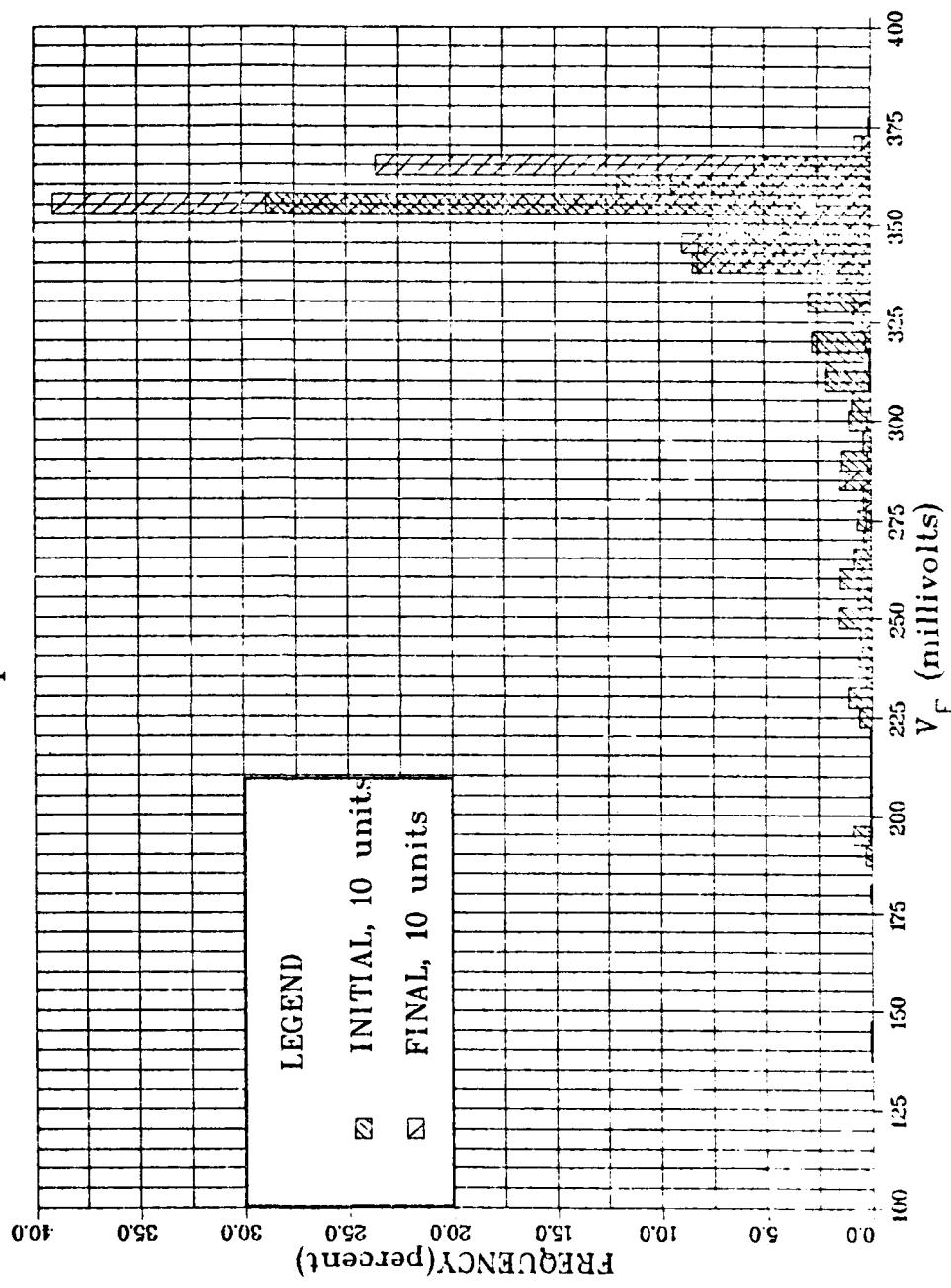
All Inputs at +25°C



## Input Clamp Voltage Distribution

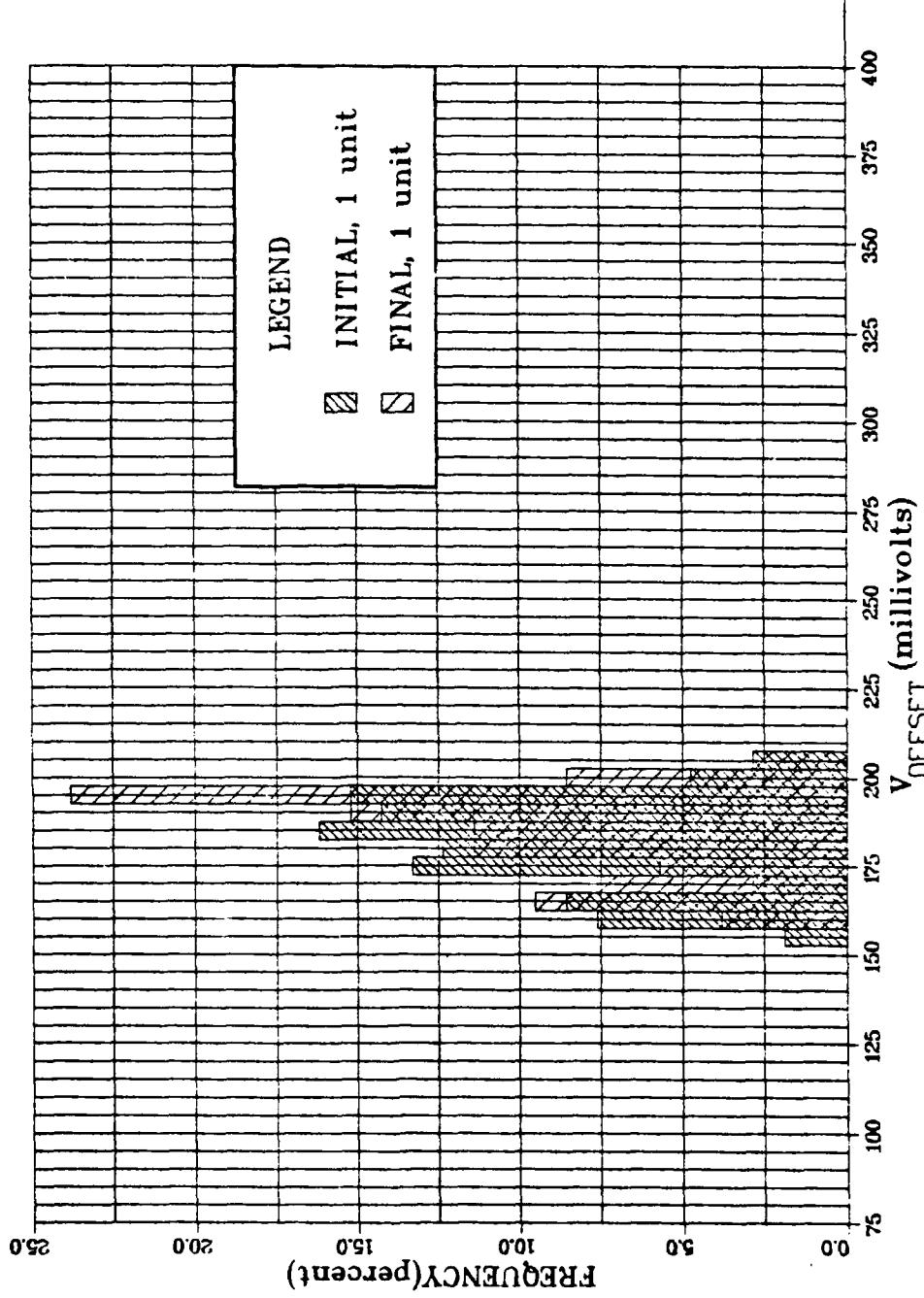
(1 microamp)

Vendor C RAM  
All Inputs at +25°C



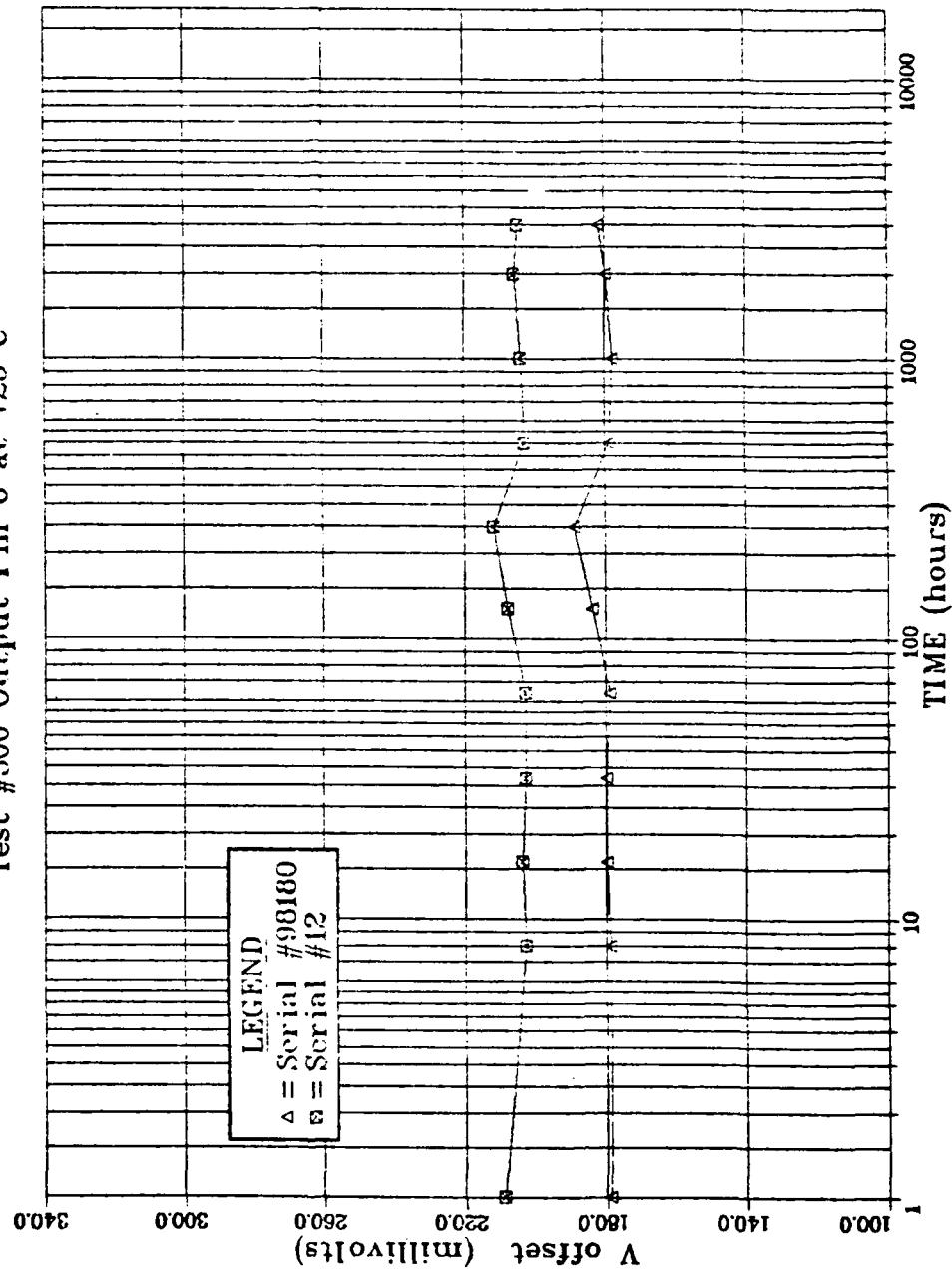
## Offset Voltage Distribution

Vendor C RAM  
Output Pin 6 at +25°C



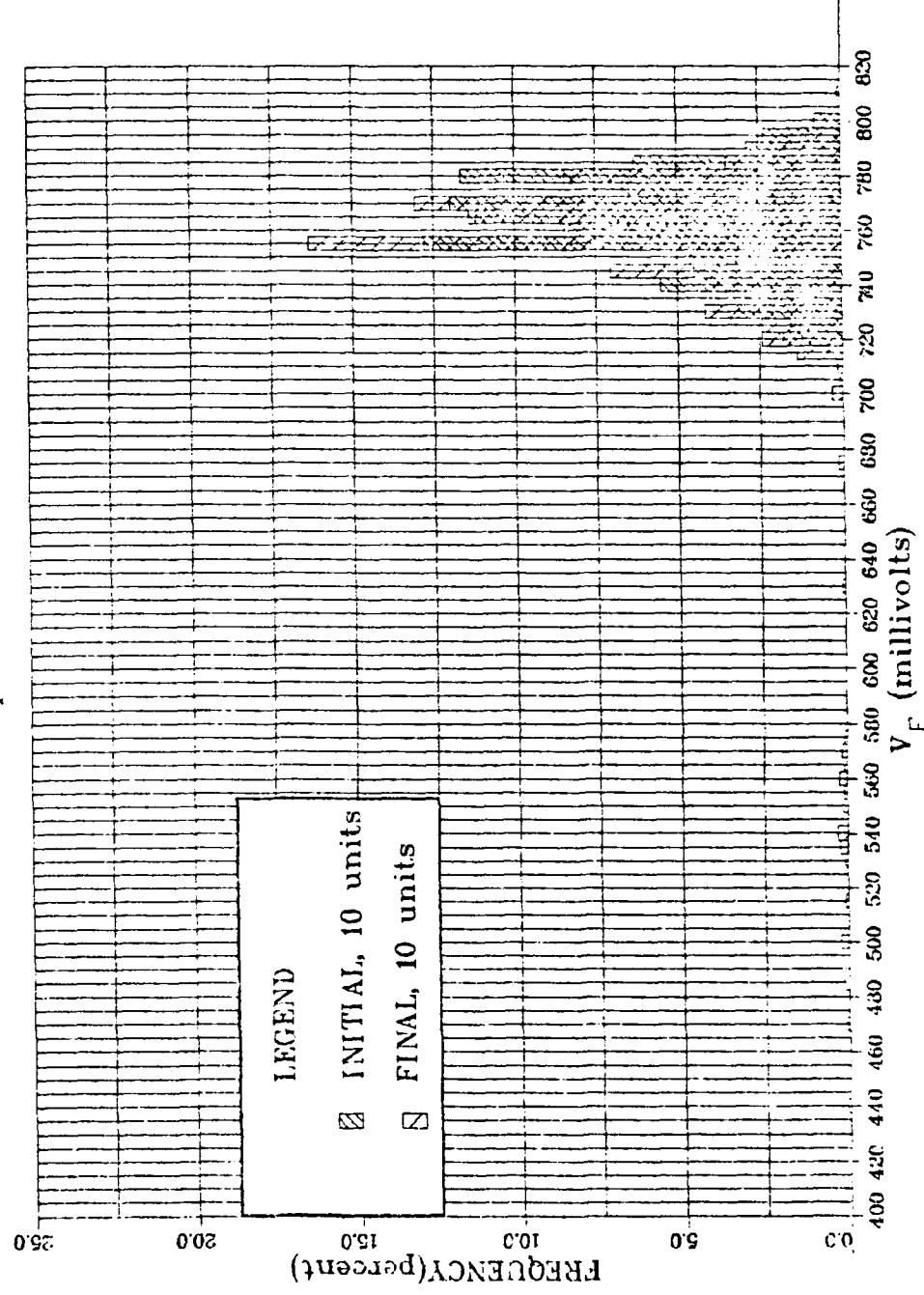
## Offset Voltage Stability

Vendor C RAM  
Stress Temperature +250°C  
Test #500 Output Pin 6 at +25°C



## Input Clamp Voltage Distribution

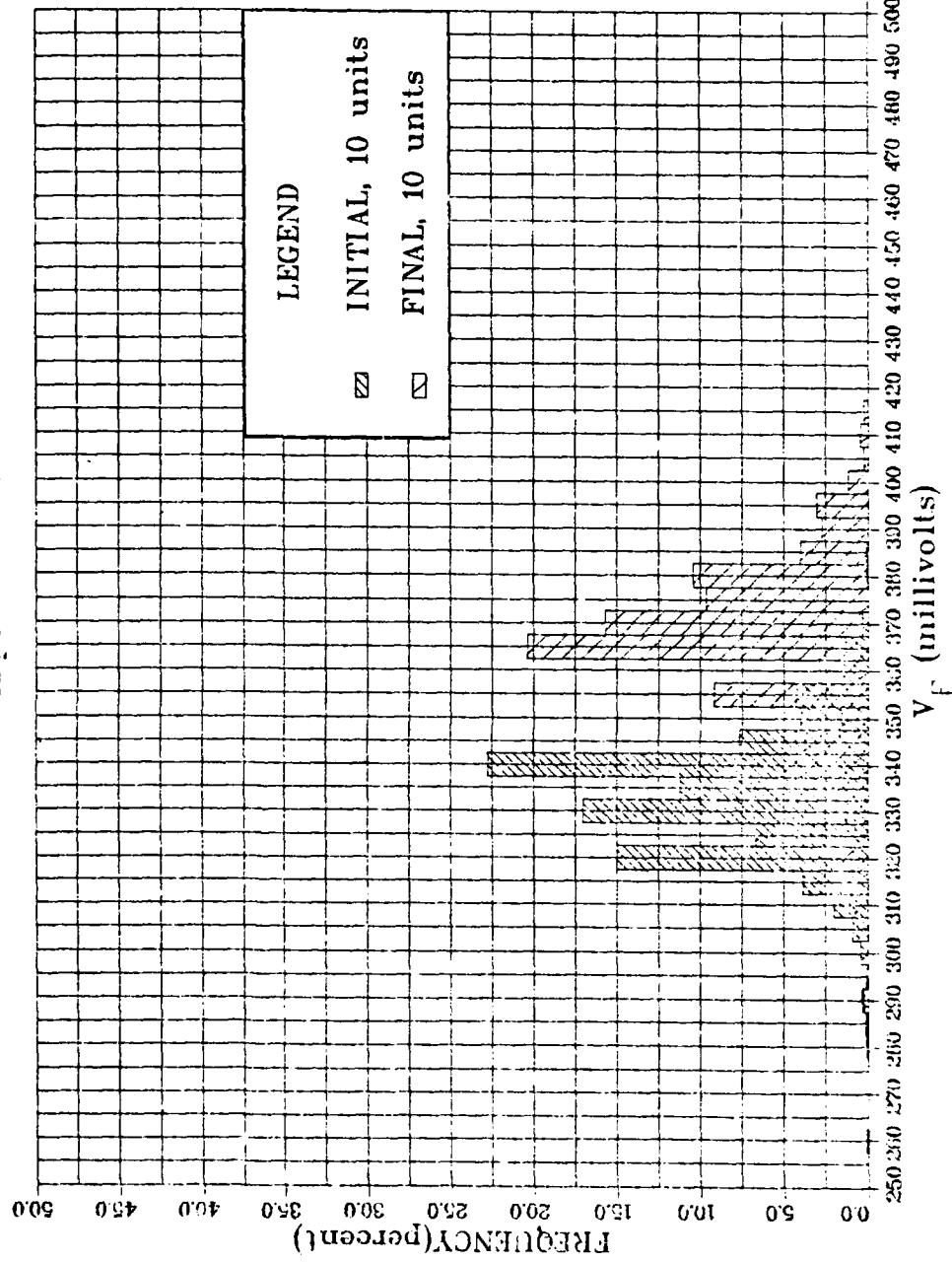
(18 milliamps)  
Vendor D RAM  
All Inputs at +25°C



## Input Clamp Voltage Distribution

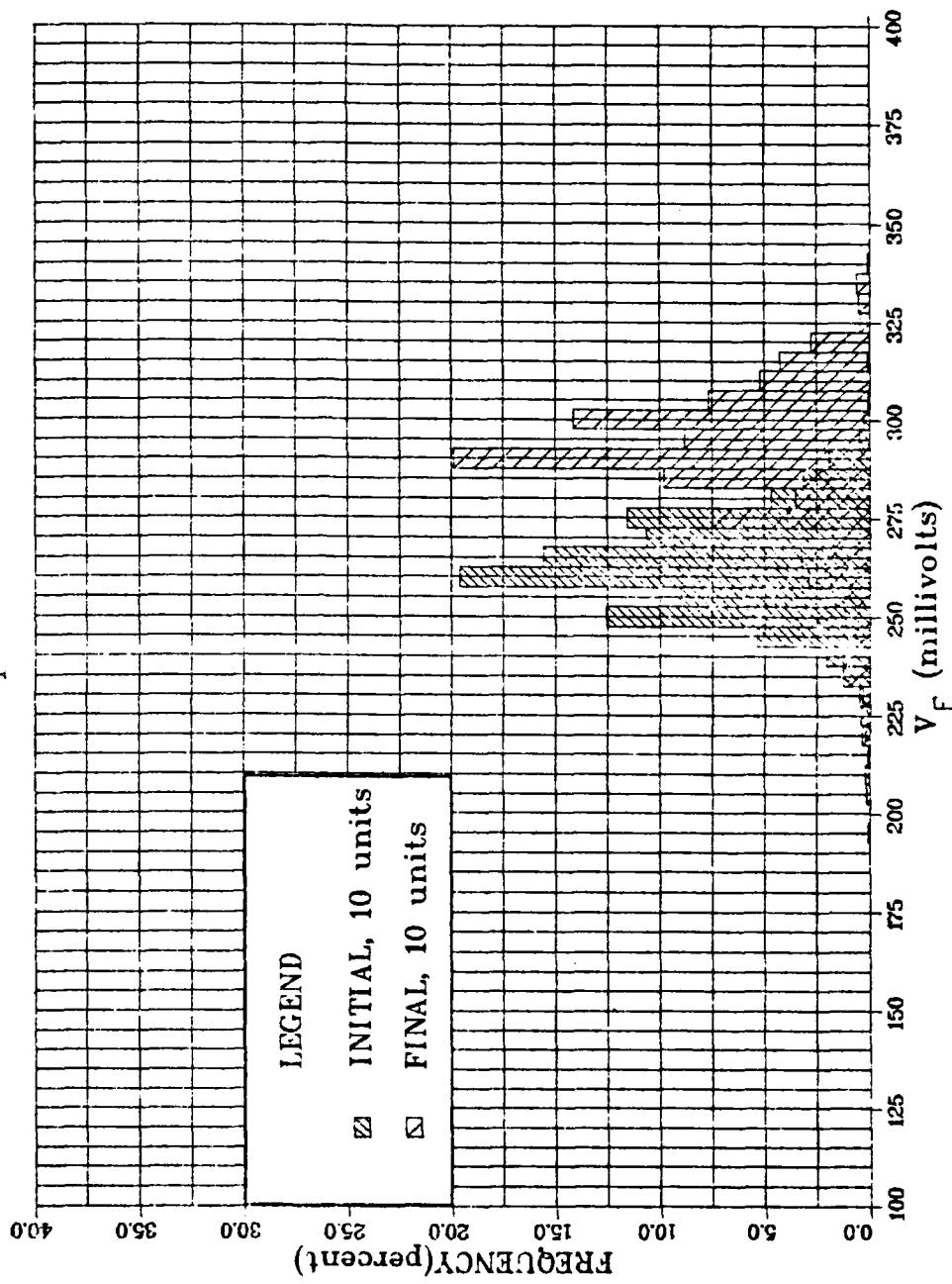
(10 microamps)

Vendor D RAM  
All Inputs at +25°C



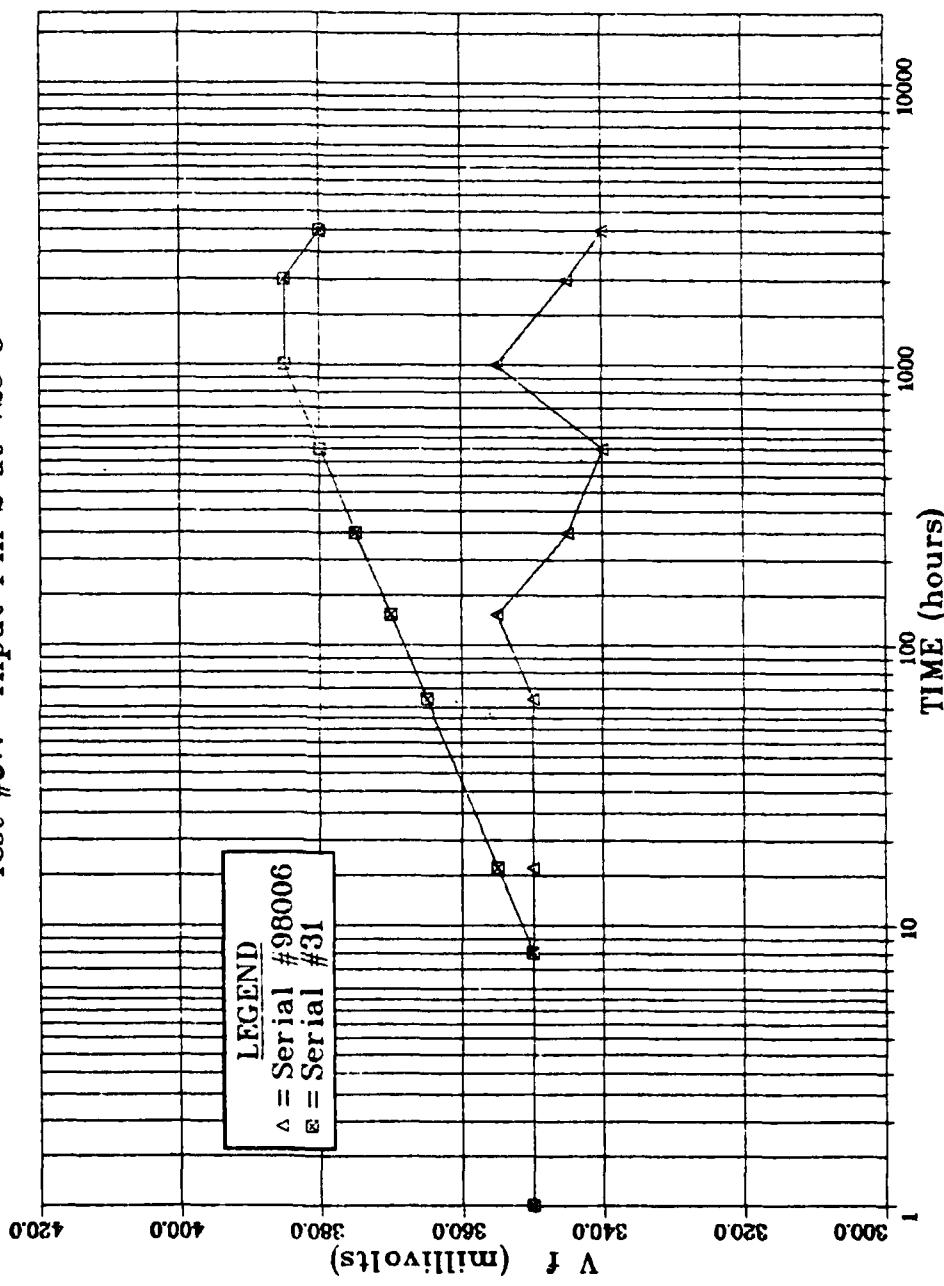
## Input Clamp Voltage Distribution

(1 microamp)  
Vendor D RAM  
All Inputs at +25°C



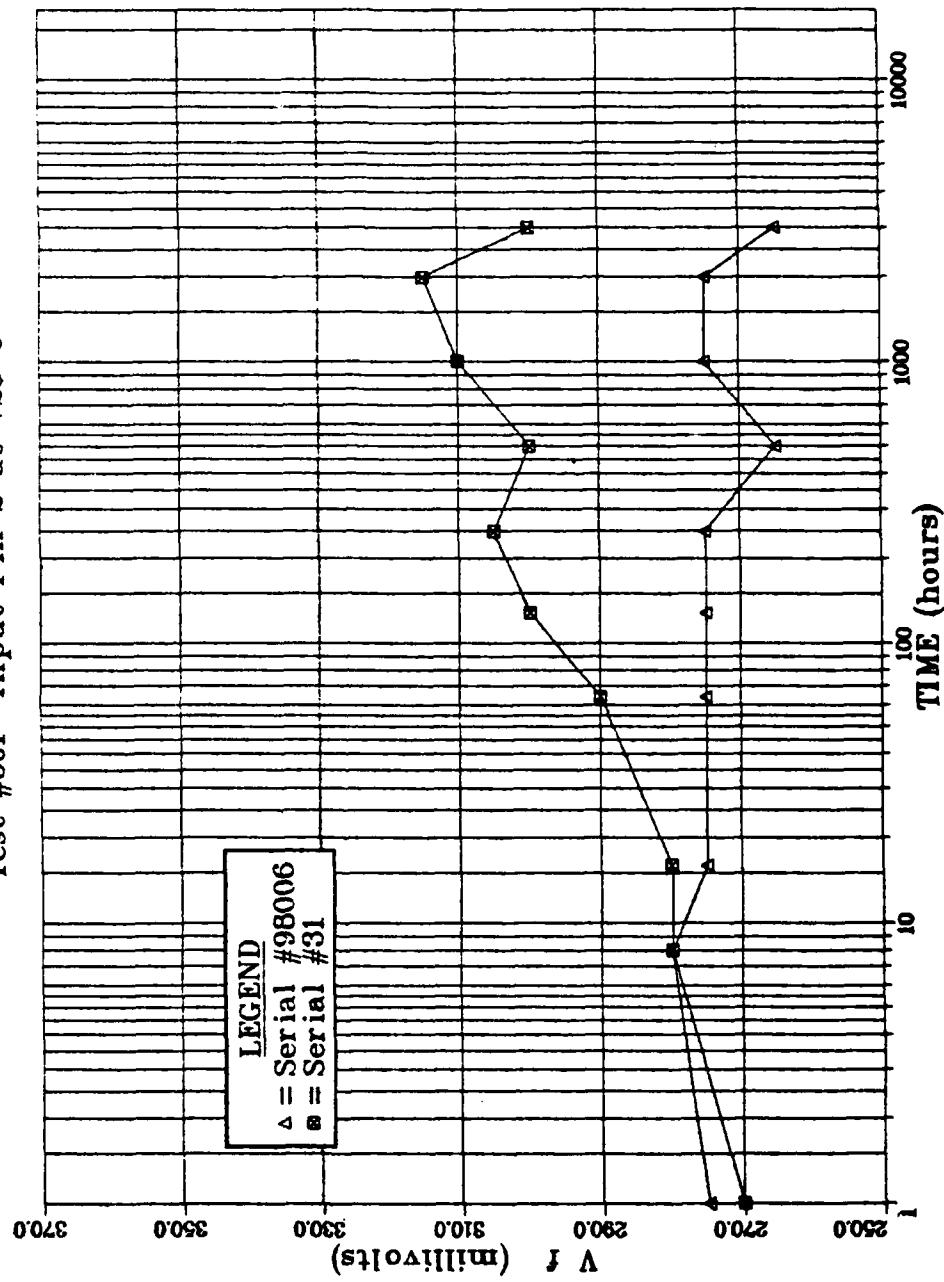
## Input Clamp Voltage Stability

Vendor D RAM (10 microamps)  
Stress Temperature +25°C  
Test #514 Input Pin 2 at +25°C



## Input Clamp Voltage Stability

Vendor D RAM (1 microamp)  
Stress Temperature +250°C  
Test #501 Input Pin 2 at +25°C



**MISSION**  
**of**  
**Rome Air Development Center**

RADC plans and executes research, development, test and selected acquisition programs in support of Command, Control Communications and Intelligence (C<sup>3</sup>I) activities. Technical and engineering support within areas of technical competence is provided to ESD Program Offices (POs) and other ESD elements. The principal technical mission areas are communications, electromagnetic guidance and control, surveillance of ground and aerospace objects, intelligence data collection and handling, information system technology, ionospheric propagation, solid state sciences, microwave physics and electronic reliability, maintainability and compatibility.

